# MN6153UC

## PLL LSI with Built-In Prescaler

### ■ Overview

The MN6153UC is a CMOS LSI for a phase-locked loop (PLL) frequency synthesizer with serial data input.

It consists of a two-coefficient prescaler, variable frequency divider, phase comparator, and charge pump.

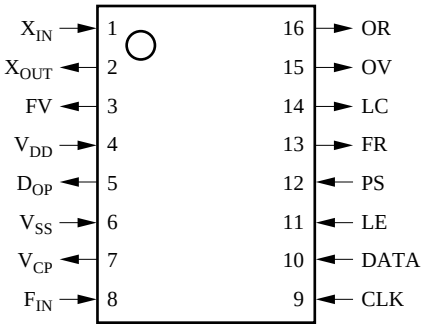
It offers high-speed operation on a low power supply voltage (1.0 to 1.4 V) and low power consumption (0.5 mW for $V_{DD}$=1.03 V, $F_{IN}$= 60 MHz).

Other features include intermittent operation by the power save (PS) control signal and high-speed pull-in that rapidly corrects the phase differences occurring at the start of operation.

### ■ Features

- Low power supply voltage: $V_{DD}$=1.0 to 1.4V
- Low power consumption: 0.5mW ($V_{DD}$=V1.03V, $F_{IN}$=60MHz)
- High-speed operation: $F_{IN}$=60MHz ($V_{DD}$=1.03V)
- Frequency dividing ratios in reference frequency dividing stage: 5 to 131,071
- Frequency dividing ratios in comparator stage: 272 to 262,143
- Lock detector output pin
- Two types of phase comparator output
  - Internal charge pump output
  - Output for external charge pump
- Output monitor pins for both comparator and reference frequency dividing stages

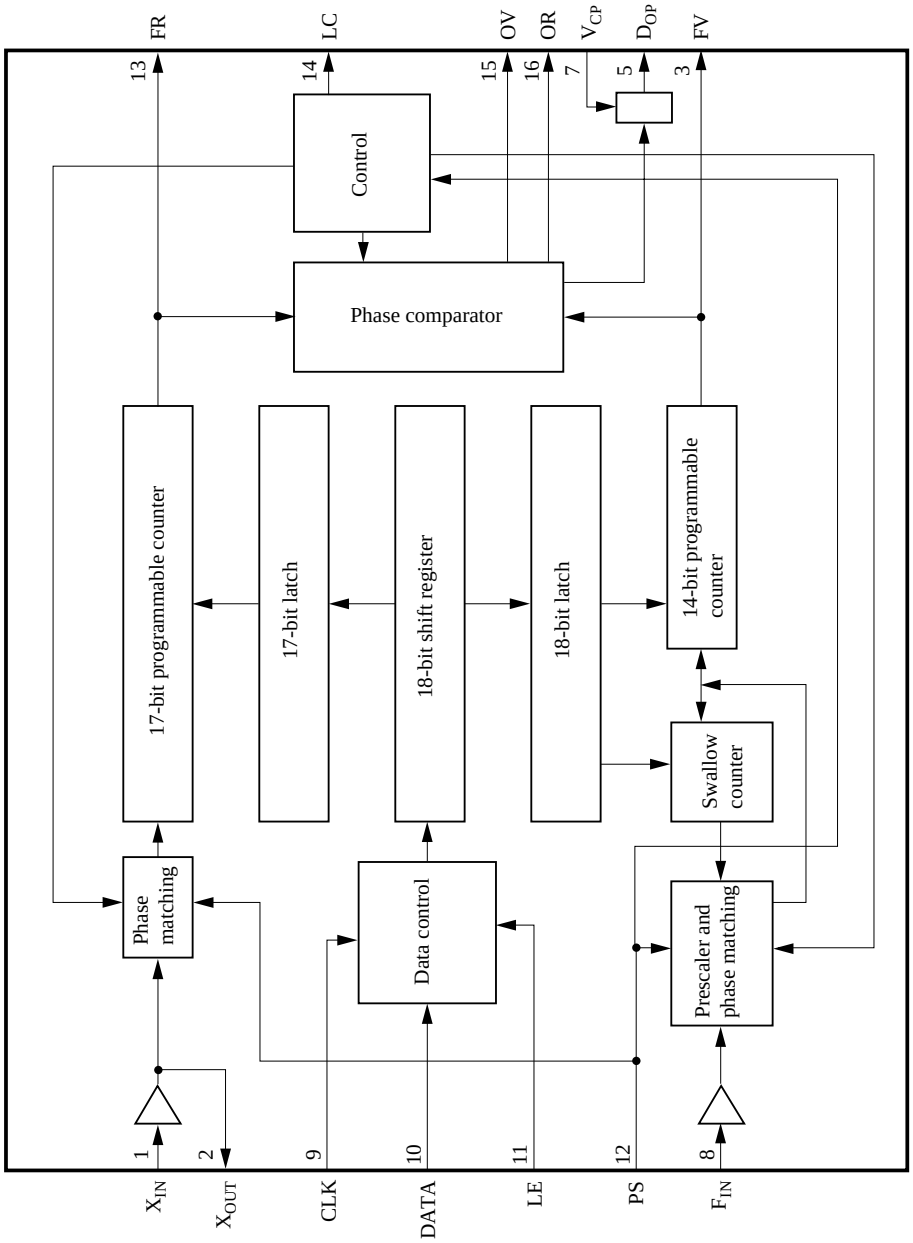
### ■ Pin Assignment




(TOP VIEW)

SSOP016-P-0225

■ Block Diagram



■ Pin Descriptions

| Pin No. | Symbol | Function Description |
|---|---|---|
| 1 | $X_{IN}$ | Crystal oscillator connection pins:<br>$X_{IN}$ =Oscillator circuit input pin;<br>$X_{OUT}$=Oscillator circuit output pin. |
| 2 | $X_{OUT}$ | |
| 3 | FV | Frequency divider output signal in comparator stage.<br>Phase comparator input monitor. |
| 4 | $V_{DD}$ | Power supply |
| 5 | $D_{OP}$ | Low-pass filter connection pin. Use a passive filter. |
| 6 | $V_{SS}$ | Ground |
| 7 | $V_{CP}$ | Power supply pin for built-in charge pump |
| 8 | $F_{IN}$ | Frequency divider input pin in comparator stage. |
| 9 | CLK | Shift register clock input pin.<br>The chip latches data at the rising edge of the CLK signal. |
| 10 | DATA | Shift register data input pin.<br>The final two bits in the data select the write latch:<br>"11" for R-latch; "01" for N-latch. |
| 11 | LE | Load enable signal input pin.<br>This is the latch-write-enable signal. It is at "H" level for write. |
| 12 | PS | Power save control signal input pin.<br>"H" level input starts the frequency divider and places the chip in operational mode.<br>"L" level input places the chip in standby mode, which saves power.<br>The chip switches the internal charge pump output to the H-z state and the loop is opened. |
| 13 | FR | Reference frequency divider output signal.<br>Phase comparator input monitor. |
| 14 | LC | Charge pump control signal output pin.<br>When frequency divider operation is stopped, this pin is at "L" level, the internal charge pump output is in the high-impedance state, and the loop is opened. |
| 15 | OV | Phase comparator output pin for external charge pump. |
| 16 | OR | (OR provides N-channel open drain output.) |

## ■ MN6153 Frequency Dividing Data Settings

The following formula shows frequency divider operation.

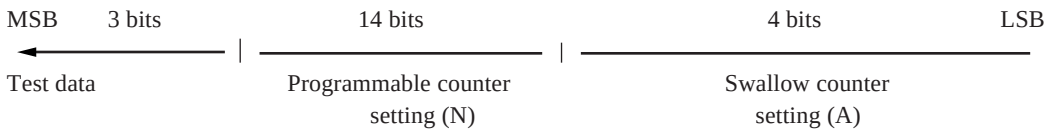
$F_{IN} = \{ (16 \times N) + A \} \times (X_{IN} \div R)$

where

- $F_{IN}$ : VCO output frequency
- N : Setting for 14-bit programmable counter on comparator side
- A : Setting for 4-bit swallow counter on comparator side
- $X_{IN}$ : Reference oscillator frequency
- R : Setting for 17-bit programmable counter on reference side

Note that N should be greater than A.

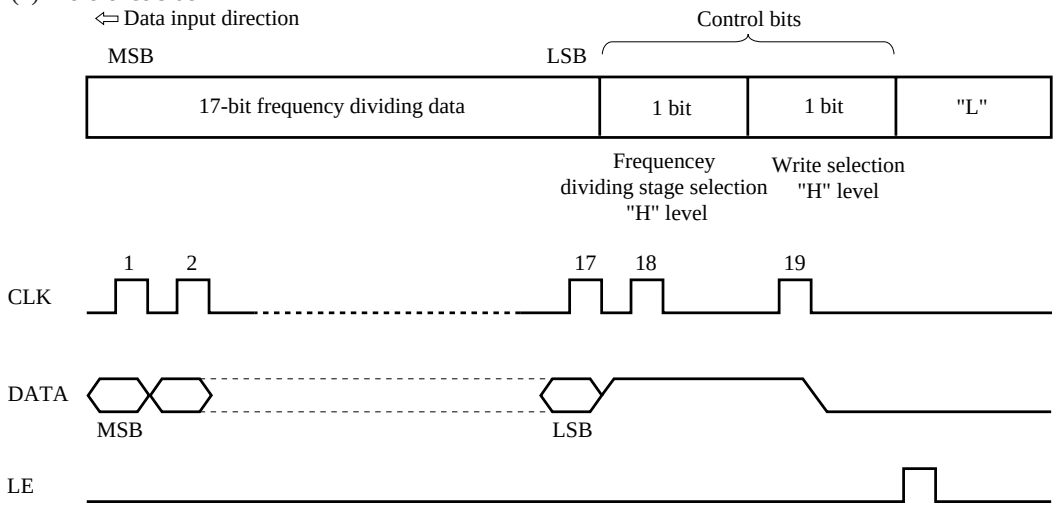
● N-Side Latch Data



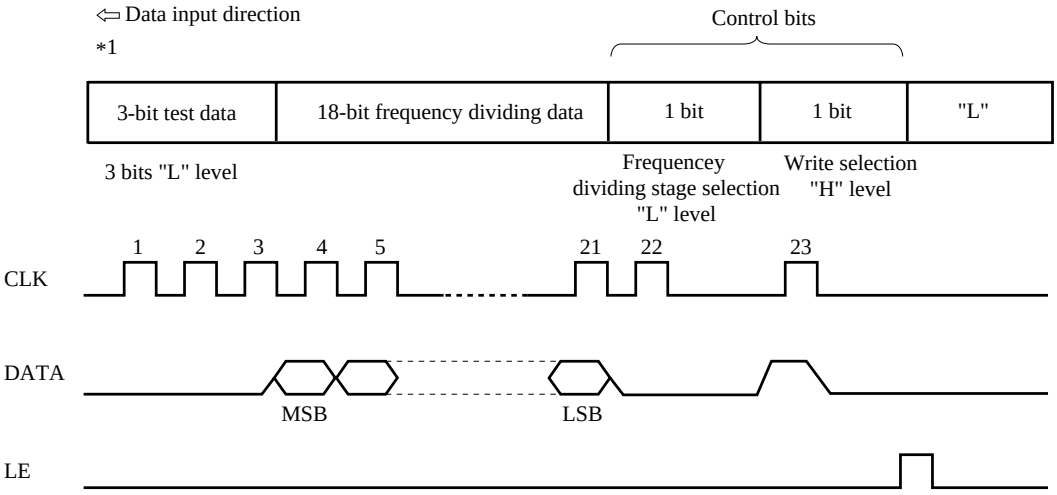
## ■ Note on Setting Frequency Dividing Data Input

1) Frequency dividing data input

(1) Reference side




(2) Comparating side




Notes

1. *1: Preceding the input of the frequency dividing data for the comparating side, input test data consisting of three "L" level bits to produce normal operation. Never use any other pattern.
2. When the power is first applied, internal operation remains in an unstable state until data is written. To eliminate the risk of excessive current consumption, keep the PS pin at "L" level.
3. When the power is first applied, the data settings are indeterminate. Always write data to the chip before starting operation.
4. Enter the data to fill the entire latch:
   Reference side: 19 bits (17 bits for the frequency divider setting and 2 control bits)
   Comparating side: 23 bits (3 bits for the test pattern, 18 bits for the frequency divider setting, and 2 control bits)
5. Drive the LE pin at "L" level while writing the data.
6. "H" level input from the LE pin causes the chip to read the data only when the CLK pin and the DATA pin are both at "L" level.
7. Writes are possible when the PS pin is either "H" or "L" level.
8. Input the data MSB first.
9. The data are inputted at the rising edge of the CLK signal.

## ■ Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Power supply voltage | $V_{DD}$ | – 0.3 to +3.0 | V |
| Power supply voltage | $V_{CP}$ | – 0.3 to +4.0 | |
| Input pin voltage | $V_I$ | $V_{SS}$ – 0.3 to $V_{DD}$ +0.3 | |
| Output pin voltage | $V_O$ | $V_{SS}$ – 0.3 to $V_{DD}$ +0.3 | |
| Power dissipation | $P_D$ | 20 | mW |
| Operating ambient temperature | $T_{opr}$ | –10 to +60 | ˚C |
| Storage temperature | $T_{stg}$ | –55 to +125 | |

## ■ Operating Conditions

$V_{SS}$=0V, Ta=–10 to +60˚C

| Parameter | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | | 1.0 | 1.1 | 1.4 | V |
| Power supply voltage | $V_{CP}$ | | 2.5 | 3.0 | 3.2 | V |

## ■ Electric Characteristics

$V_{CP}$=2.5V, Ta=–10 to +60˚C

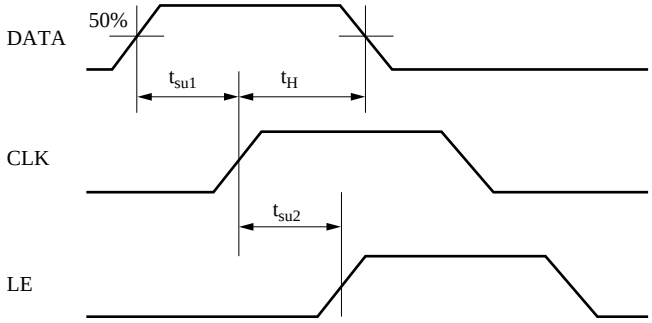
| Parameter | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Power supply pin | $V_{DD}$ | $V_{DD}$=1.03V | | | | |
| Power supply current | $I_{DD}$ | $F_{IN}$=100MHz, $X_{IN}$=20MHz, PS="H" | | | 0.5 | mA |
| | $I_{Dstop}$ | PS="L" (at power save operation) | | | 2.0 | µA |
| Input Pins CLK, DATA, LE, PS $V_{DD}$=1.0 to 1.4V | | | | | | |
| "H" level input voltage | $V_{IH}$ | | $V_{DD}$ – 0.2 | | $V_{DD}$ | V |
| "L" level input voltage | $V_{IL}$ | | $V_{SS}$ | | 0.2 | |
| Input leakage current | $I_{LI}$ | | | | ±1.0 | µA |
| Input Pin $F_{IN}$ $V_{DD}$=1.03 to 1.4V | | | | | | |
| Input voltage | $V_{IN}$ | | 0.4 | | | $V_{p-p}$ |
| Input current | $I_{IF}$ | Pull-up resistor is present (PS="L") | –10 | | –100 | µA |
| Input leakage current | $I_{LIF}$ | $V_{IN}$=0 or $V_{DD}$ (PS="H") | | | ±20 | µA |
| Maximum operating frequency | $F_{INMAX}$ | $V_{IN}$=0.4 $V_{p-p}$ | 60 | | | MHz |
| Minimum operating frequency | $F_{INMIN}$ | $V_{IN}$=0.4 $V_{p-p}$ | | | 10 | MHz |
| Input Pin $X_{IN}$ $V_{DD}$=1.0 to 1.4V | | | | | | |
| Input voltage | $V_{IN}$ | | 0.4 | | | $V_{p-p}$ |
| Input current | $I_{IX}$ | Pull-up resistor is present (PS="L") | – 0.2 | | –1.5 | mA |
| Input leakage current | $I_{LIX}$ | VIN=0 or $V_{DD}$ | | | 2.0 | µA |

## ■ Electrical Characteristics (continued)

$V_{CP}$=2.5V, Ta=–10 to +60˚C

| Parameter | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Crystal Oscillator Pins $X_{IN}$, $X_{OUT}$ $V_{DD}$=1.03 to 1.4V | | | | | | |
| Crystal oscillator frequency | $f_{Xtal}$ | | | 12.8 | | MHz |
| Output Pins FV, FR, LC, OV $V_{DD}$=1.0 to 1.4V | | | | | | |
| "H"level output voltage | $V_{OH}$ | $I_{OH}$= –60µA | $V_{DD}$– 0.3 | | $V_{DD}$ | V |
| "L"level output voltage | $V_{OL}$ | $I_{OL}$=30µA | $V_{SS}$ | | 0.3 | |
| Output Pin $X_{OUT}$ $V_{DD}$=1.0 to 1.4V | | | | | | |
| "H"level output voltage | $V_{XOH}$ | $I_{XOH}$= –100µA | $V_{DD}$– 0.3 | | $V_{DD}$ | V |
| "L"level output voltage | $V_{XOL}$ | $I_{XOL}$=100µA | $V_{SS}$ | | 0.3 | |
| Output Pin $D_{OP}$ $V_{DD}$=1.0 to 1.4V | | | | | | |
| "H"level output voltage | $I_{DOH}$ | $V_{Dop}$=$V_{CP}$ – 0.3V | –250 | | | µA |
| "L"level output voltage | $I_{DOL}$ | $V_{Dop}$=0.3V | 250 | | | |
| Output leak current | $I_{LOH}$ | $V_{Dop}$=$V_{CP}$ | | | 2.0 | |
| Output leak current | $I_{LOL}$ | $V_{Dop}$=0.0V | | | –2.0 | |
| Output Pin OR $V_{DD}$=1.0 to 1.4V | | | | | | |
| "L"level output voltage | $I_{ORL}$ | $V_{OR}$=0.3V | 45 | | | µA |
| $V_{DD}$=1.0 to 1.4V | | | | | | |
| Setup time *1 | $t_{sul}$ | | 500 | | | ns |
| | $t_{su2}$ | | 500 | | | ns |
| Hold time *1 | $t_H$ | | 500 | | | ns |

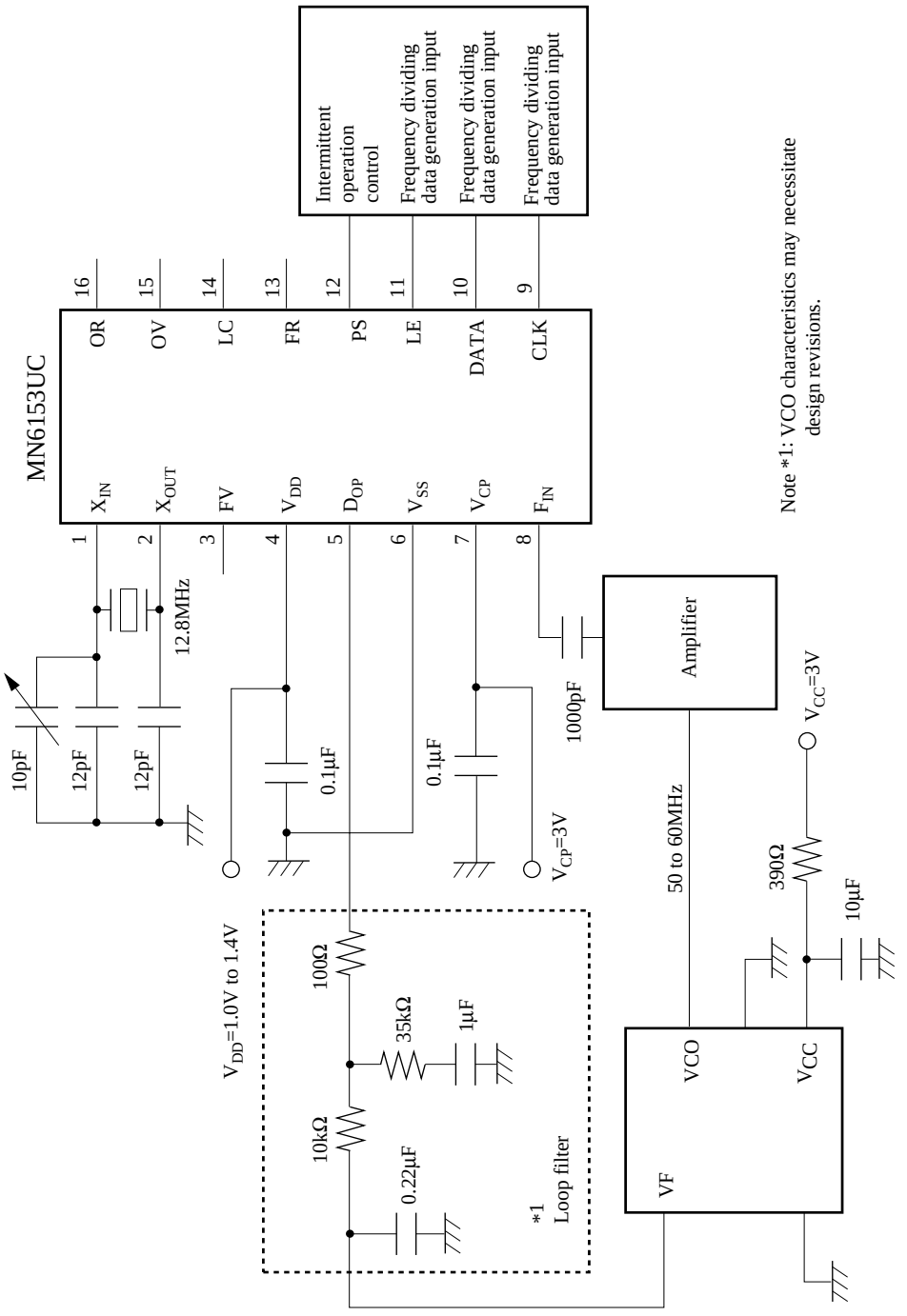
Note*1: The following timing chart shows the setup and hold times.




Usage Note

Be particularly careful with this product as it is more sensitive on the static electricity damage than most of our other products.

■ Application Circuit Example



■ Package Dimensions (Unit: mm)

SSOP016-P-0225