DATA SHEET

PTN3310/PTN3311
High-speed serial logic translators

Product data

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Philips
Semiconductors

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High-speed serial logic translators PTN3310/PTN3311

FEATURES

- Meets LVDS EIA-644 and PECL standards
- 2 pin-for-pin replacement input/output choices:
  - LVDS in, PECL out (PTN3310)
  - PECL in, LVDS out (PTN3311)
- Single +3.3 V supply voltage operation
- Available in 8-pin SO package
- Maximum throughput data rate of 800 Mbps typical

APPLICATIONS

- High-speed networking and telecom applications
  - ATM
  - SONET/SDH
  - Switches
  - Routers
  - Add-drop multiplexers

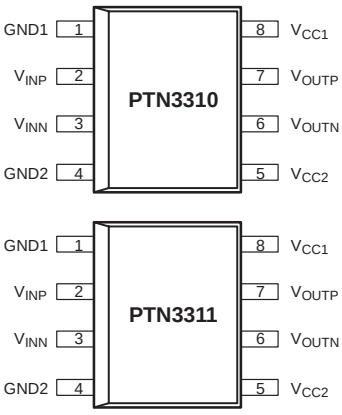
GENERAL DESCRIPTION

The High-Speed Serial Logic Translator provides a point solution that addresses the various interface logic requirements of Optical Transceiver Modules. The product offers a compact translation between LVDS and PECL high speed serial data lines. This provides the end users a simple way to mix or match Optical Transceiver ICs from various vendors to maximize desired performance and reduces the need to redesign interfaces to accommodate new Optical Transceiver ICs.

The High-Speed Serial Logic Translator comes in two translation choices to allow mixing LVDS and PECL input/outputs. The product is offered in a small, convenient, 8-pin package.

Figure 1 shows the High-Speed Serial Logic Translator Device in a typical high speed optical module application. Figure 2 shows the circuit block diagrams.

PIN CONFIGURATIONS



8-pin SO package

ST00014

PIN DESCRIPTIONS

8-pin SO package

Pin #	Symbol	Name and function
1, 4	GND1, GND2	Ground
2, 3	V_{INP}, V_{INN}	Differential inputs
5, 8	V_{CC1}, V_{CC2}	Supply voltage
6, 7	V_{OUTN}, V_{OUTP}	Differential outputs

ORDERING INFORMATION

Type number	Package		
	Name	Description	Version
PTN3310D	SO8	Plastic small-outline package; 8 leads; body width 3.9 mm	SOT96-1
PTN3311D	SO8	Plastic small-outline package; 8 leads; body width 3.9 mm	SOT96-1

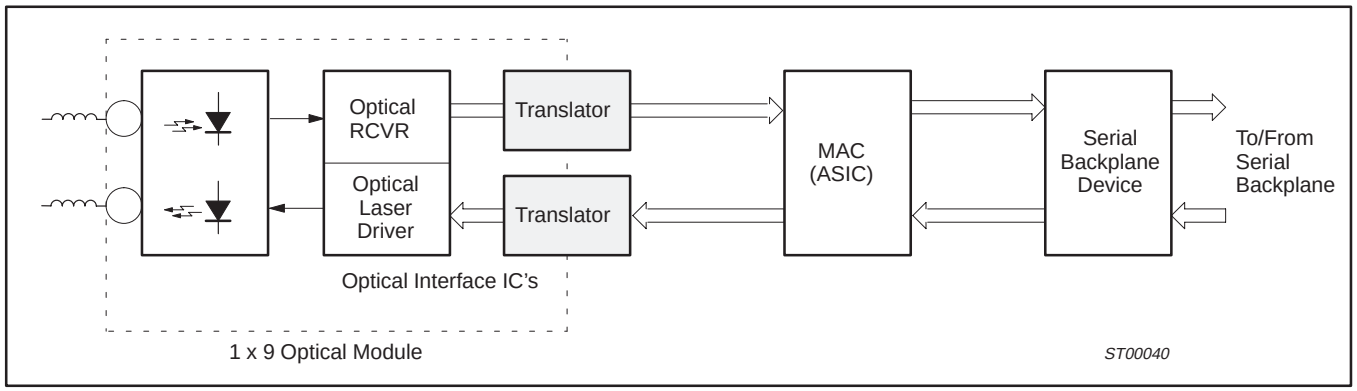


Figure 1. High-Speed Serial Logic Translators in Optical Module Application

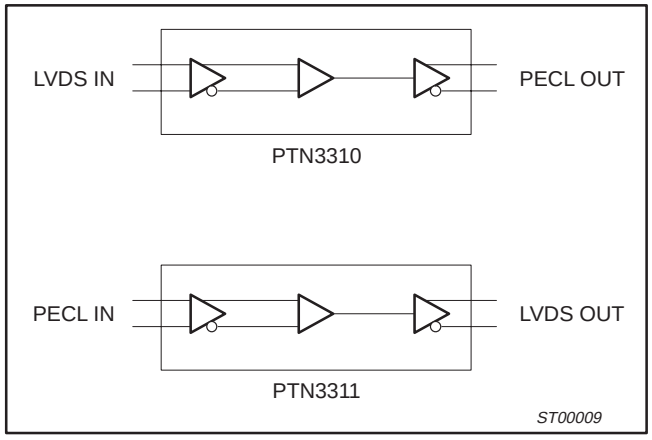


Figure 2. High-Speed Serial Logic Translator Block Diagrams

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Limits	Unit
V_{CC}	Supply voltage	–0.3 to +4.0	V
V_I	LVDS receiver input voltage	–0.3 to +5.5	V
V_O	LVDS driver output voltage	–0.3 to +5.5	V
t_{SC}	LVDS output short circuit duration	continuous	
T_j	Maximum junction temperature	+150	°C
T_{stg}	Storage temperature range	–65 to +150	°C
ESD_{HBM}	Electrostatic discharge (Human Body Model, 1.5 kΩ, 100 pF)	>2	kV
ESD_{MM}	Electrostatic discharge (Machine Model, 0 kΩ, 200 pF)	>200	V

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	3.0	3.6	V
T_{amb}	Operating ambient temperature range in free air	–40	+85	°C
V_{CCN}	Power supply noise voltage	–	100	mV_{PP}

DC ELECTRICAL CHARACTERISTICS

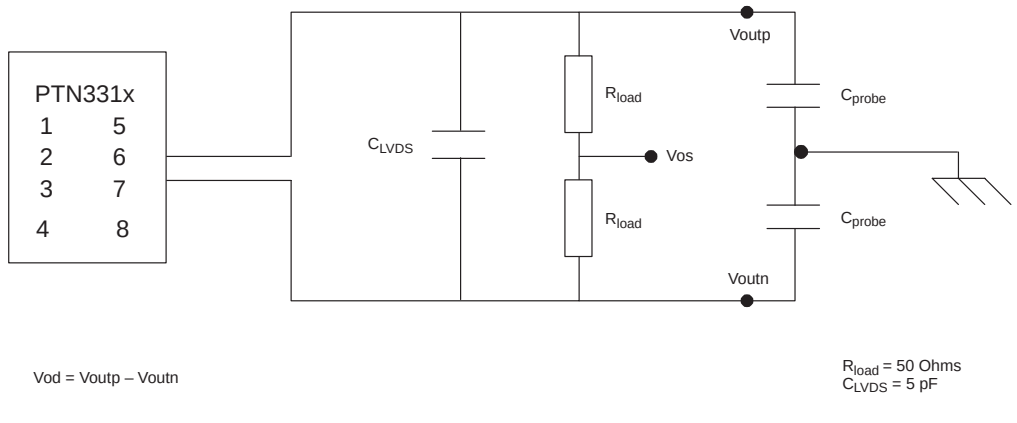
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General						
V_{CC}	Supply voltage		3.0	3.3	3.6	V
I_{CC}	Power supply current	PTN3311	–	12	20	mA
I_{EE}	Power supply current	PTN3310	–	13	20	mA
PECL inputs (PTN3311)						
V_{IH}	Input HIGH voltage[1]		2.135	–	2.420	V
V_{IL}	Input LOW voltage[1]		1.490	–	1.825	V
I_I	Input current	$V_{IN} = V_{CC}$ or GND	–	–	±10	μA
LVDS inputs (PTN3310)						
V_{ID}	Minimum differential input signal amplitude		100	–	–	mV
I_{IN}	Input current[2]	V_{IN} = 0 V	–	–	20	μA
		$V_{IN} = V_{CC}$	–	–	20	μA
PECL outputs (PTN3310)						
V_{OH}	Output HIGH voltage[1]		2.275	2.345	2.420	V
V_{OL}	Output LOW voltage[1]		1.490	1.595	1.680	V
C_L	Output load capacitance		–	5	–	pF
LVDS outputs (PTN3311); R_L = 100 Ω						
V_{OD}	Output differential voltage		250	350	450	mV
ΔV_{OD}	Steady-state difference in output differential voltage between complementary output states		–	–	50	mV
V_{OS}	Offset voltage		1.125	1.250	1.375	V
ΔV_{OS}	Steady-state difference in offset voltage between complementary output states		–	–	50	mV
I_{OS}	Output short-circuit current	outputs mutually shorted	–	–	12	mA
		output shorted to GND	–	–	24	mA
C_L	Output load capacitance		–	5	–	pF

NOTES:
1. These values are for V_{CC} = 3.3 V; PECL level specifications are referenced to V_{CC} and will track 1:1 with variation of V_{CC}.
2. Power supply either on or off.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General						
f_{MAX}	Maximum throughput data rate		655	800	–	Mbps
t_{SKEW}	Clock output skew, part-to-part		–	100	–	ps
	Clock output pulse skew		–	50	–	ps
t_{PLH}/t_{PHL}	Propagation delay input (differential) to output		–	1	3	ns
	Propagation delay input (single-ended) to output		–	1	3	ns
PECL outputs (PTN3310)						
t_r/t_f	Output rise and fall times at 20% and 80% intersects		–	200	300	ps
LVDS outputs (PTN3311); R_L = 100 Ω; C_L = 5 pF						
t_{TLH}	Transition time LOW to HIGH	R_L = 100 Ω; C_L = 5 pF	–	500	650	ps
t_{THL}	Transition time HIGH to LOW	R_L = 100 Ω; C_L = 5 pF	–	500	650	ps
V_{OSS}	Peak-to-peak switching offset voltage	Measured between two matched 49.9 Ω load resistors; 5 pF load capacitance	–	–	150	mV

LVDS REFERENCE MEASUREMENT CONFIGURATION



The above diagram shows the test set-up used when evaluating LVDS outputs. According to the TIA-EIA-644 Standard, the maximum lumped capacitance test load should be 5 pF. However, by using probes or cables to observe the signal, additional capacitance is added, which has an effect on the rise and fall times. C_{probe} represents any capacitance caused by the use of probes or cables. Assuming balanced loading and balanced output drivers, the total effective capacitance seen by the part is:

$$C_{Eff} = C_{LVDS} + {}^1/_2\, C_{probe}$$

To correctly account for the effects of C_{probe}, the following formula should be used:

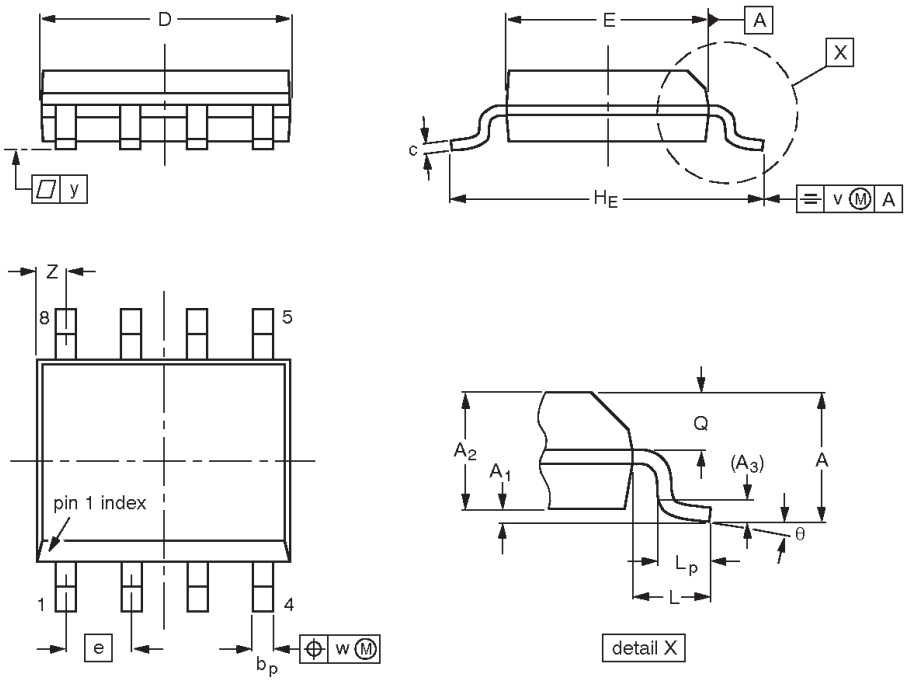
$$\Delta t = \frac{5\ pF}{C_{Eff}}\ \Delta t_{\ measured,}$$

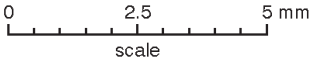
Where Δt is the 20%–80% rise/fall time.

To avoid the use of additional calculation of the measured results, a different approach could be taken; however, the value of C_{probe} has to be known in advance. In that case, the value of C_{LVDS} can be chosen such that the sum of the capacitances equals 5 pF, i.e.:

$$C_{LVDS} + {}^1/_2\, C_{probe} = 5\ pF$$

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

Data sheet status

Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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