1 PRODUCT OVERVIEW

SAM87 RC PRODUCT FAMILY

Samsung's new SAM87RC family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Timer/counters with selectable operating modes are included to support real-time operations. Many SAM87RC microcontrollers have an external interface that provides access to external memory and other peripheral devices. The sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum six CPU clocks) can be assigned to specific interrupt levels.

S3C8454 MICROCONTROLLER

The S3C8454 single-chip microcontroller is fabricated using a highly advanced CMOS process. Its design is based on the powerful SAM87RC CPU core. Stop and Idle power-down modes were implemented to reduce power consumption. The size of the internal register file is logically expanded, increasing the addressable on-chip register space to 1040 bytes. A flexible yet sophisticated external interface is used to access up to 64-Kbytes of program and data memory. The S3C8454 is a versatile microcontroller that is ideal for use in a wide range of general-purpose applications such as CD-ROM/DVD-ROM drives.

Using the SAM87RC modular design approach, the following peripherals were integrated with the SAM87RC CPU core:

— Five configurable 8-bit general I/O ports
— One 2-bit general I/O ports
— Full-duplex serial data port with one synchronous operating modes
— Two 8-bit timers with interval timer
— Two 16-bit timers/counters with PWM operating modes or capture modes
— One voltage level detector pin
— Four embedded chip selection pins (CS0–CS4) or normal I/O ports
— Two programmable 8-bit PWM modules with corresponding output pins
— A/D converter with 4 selectable input pins

OTP

The S3C8454 microcontroller is also available in OTP(One Time Programmable) version, S3P8454
The S3P8454 microcontroller has an on-chip 4K-byte one-time-programmable EPROM instead of masked ROM. The S3P8454 is comparable to S3C8454, both in function and in pin configuration.

FEATURES

CPU

- SAM87RC CPU core

Memory

- 1040-byte internal register file
- 4-Kbyte internal program memory

External Interface

- 64 Kbyte external data memory
- 64 Kbyte external program memory area (ROMless)
- 60 Kbyte external program memory and 4 Kbyte internal program memory

ADC

- Can be used as a general input/output port
- 8-bit resolution four channels

SIO

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable
- Internal or external clock mode

8-bit Timers

- Two 8-bit timers with interval timer mode (Timer A and B)

16-bit Timer/Counters

- Two programmable 16-bit timer/counters
- Interval, or event counter mode operation
- 16-bit capture and 16-bit PWM mode
- Internal or external clock source

Basic Timer (Watchdog Timer)

- Overflow signal makes a system reset
- 8-bit timer with interval timer mode

General I/O Ports

- Five 8-bit general I/O ports (port 0, 1, 2, 3, 4)
- One 2-bit general I/O port (port 5)
- Port 2 can drive LED directly

Interrupts

- Six edge-driven external interrupts
- Two level-driven external interrupts
- Fast interrupt mode processing

PWM

- Four output channels (PWM0, PWM1, TCPWM, TDPWM)
- 8-bit resolution with a 4-bit prescaler (PWM0, PWM1)
- From 16-bit counter (Timer C/D) (TCPWM, TDPWM)

Embedded chip selection

- To reduce interface glue logic, chip selection logic is bold

Voltage level detector

- To prevent MCU from malfunctioning in an unstable power level, a voltage level detector circuit is inserted

Operating Voltage Range

- 2.7 V to 5.5 volts (@12 MHz)

Operating Temperature Range

- – 40 °C to + 85 °C

Package Types

- 80-pin QFP or TQFP

Operating frequency

- 25 MHz (4.5 V to 5.5 V)

BLOCK DIAGRAM

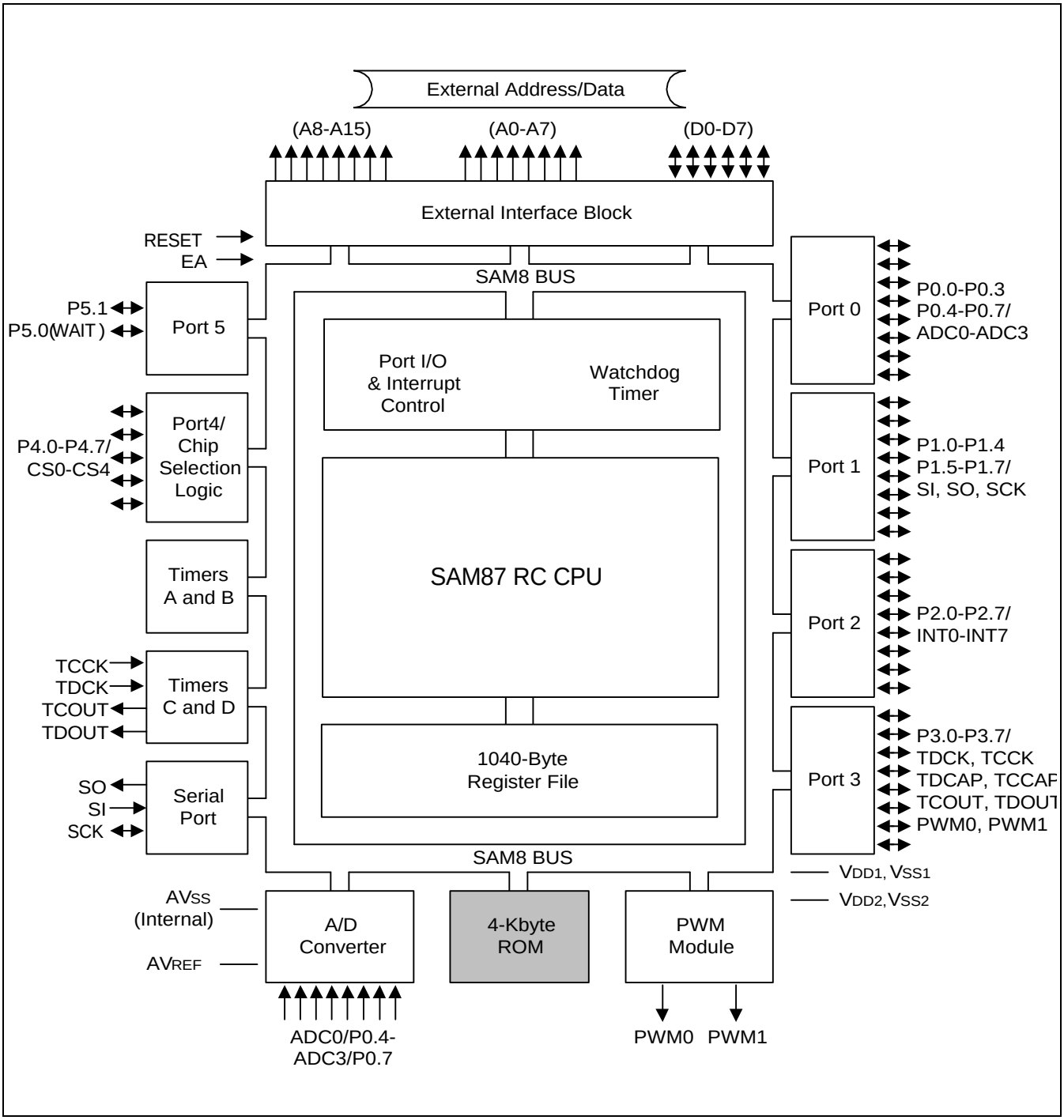


Figure 1-1. S3C8454 Block Diagram

PIN ASSIGNMENT

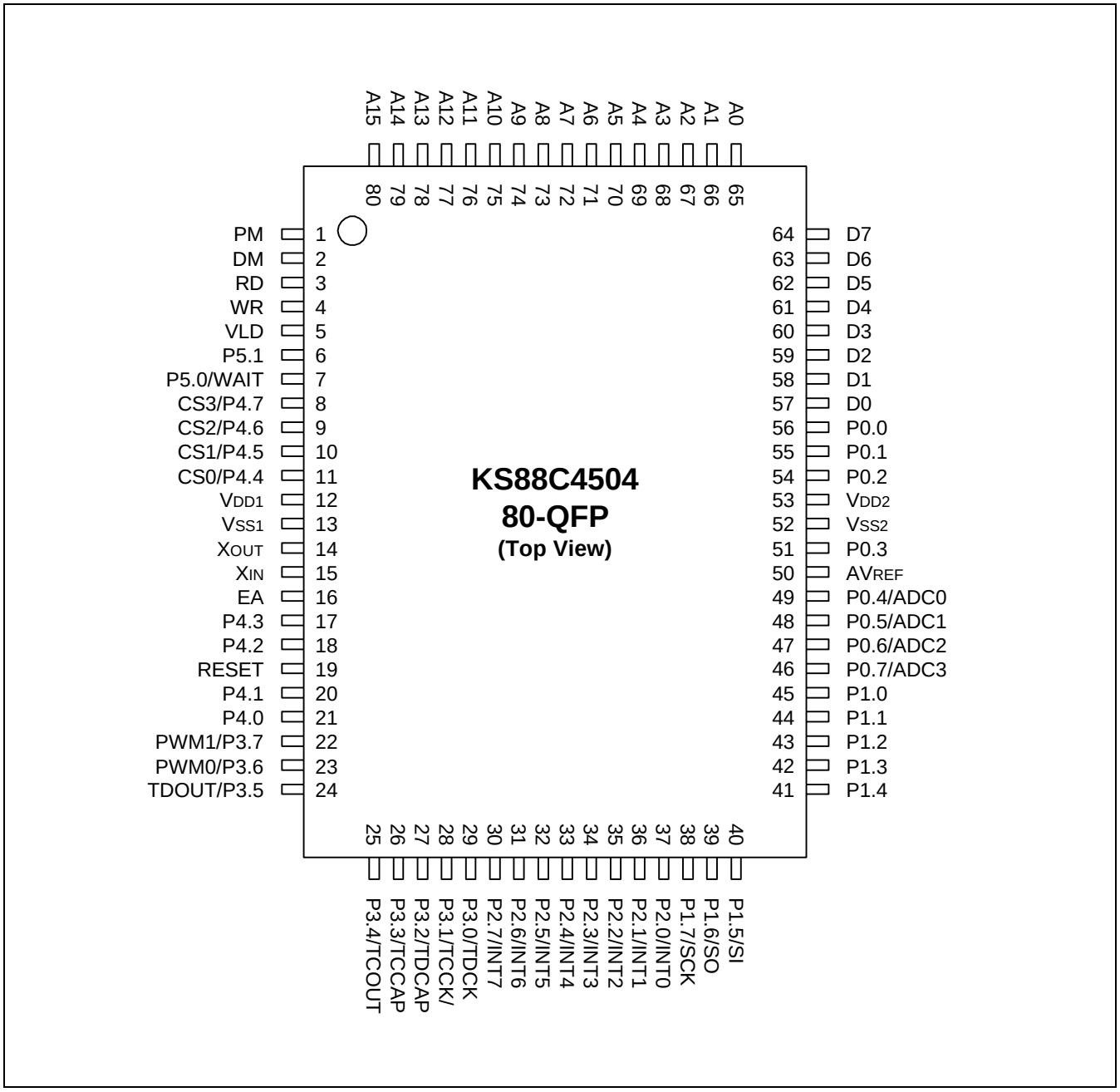


Figure 1-2. S3C8454 Pin Assignments

PIN ASSIGNMENTS (Continued)

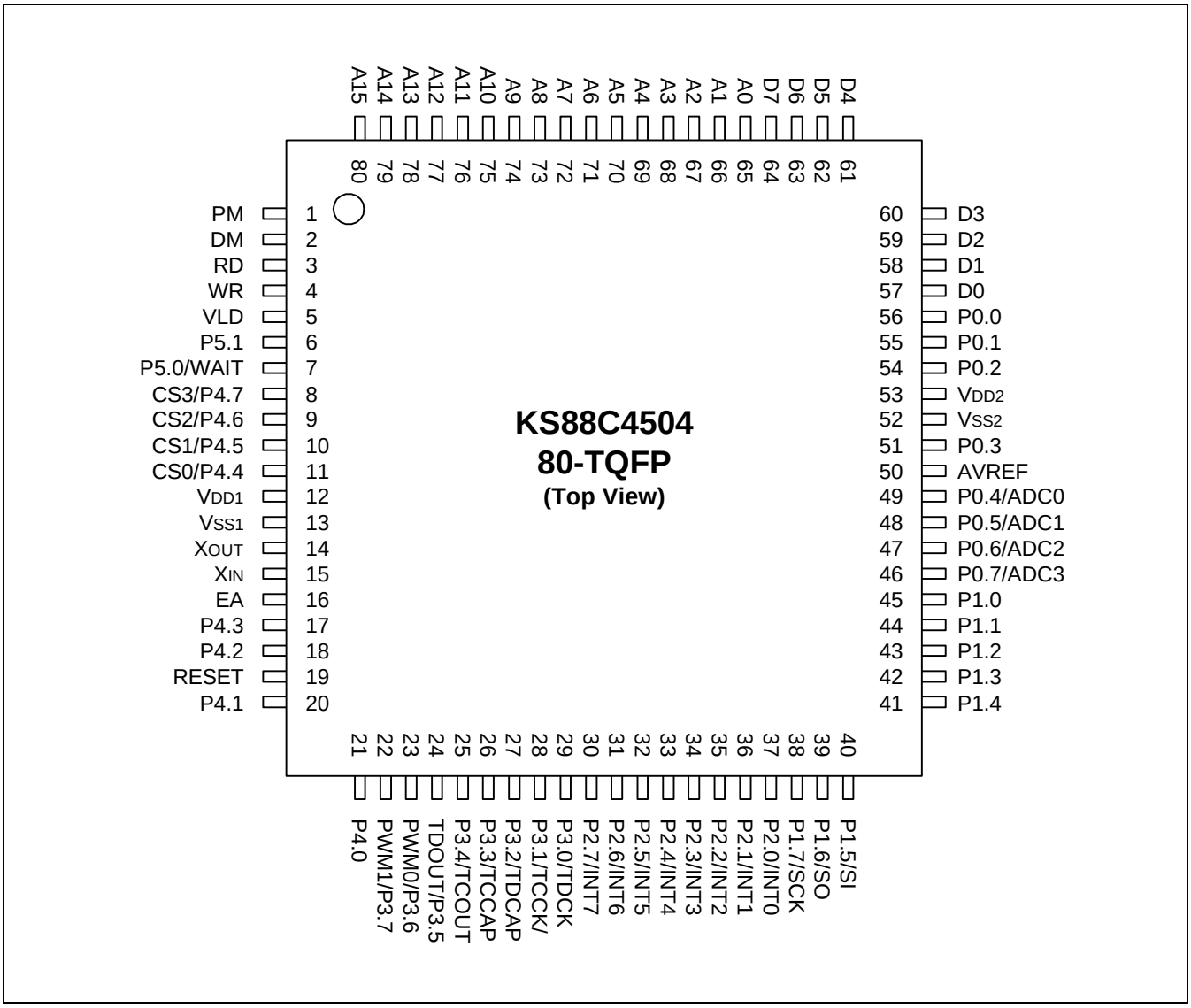


Figure 1-3. S3C8454 Pin Assignments

PIN DESCRIPTIONS

Table 1-1. S3C8454/P8454 Pin Descriptions

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
P0.0–P0.7	I/O	Bit programmable port; input or output mode selected by software; normal input or push-pull output with software assignable pull-up (P0.0–P0.3) or pull-down (P0.4–P0.7). Alternately, P0.4–P0.7 can be use as a ADC input port with 8-bit resolution.	2, 3	56–54, 51, 49–46	ADC0–ADC3
P1.0–P1.7	I/O	Bit programmable port; input or output mode selected by software; normal input or push-pull output with software assignable pull-up. P1.5–P1.7 can be used as a synchronous SIO port P1.5/SI P1.6/SO P1.7/SCK	3	45–38	SI, SO, SCK
P2.0–P2.7	I/O	General I/O port with normal input or push-pull output with software; assignable pull-up. Bit programmable. Alternately, P2.0–P2.7 can be used as inputs for external interrupts, INT0–INT7 (with noise filter and interrupt control). INT0/INT1 is level interrupts.	4	37–30	INT0–INT7
P3.0–P3.7	I/O	General I/O port with bit programmable pins. Normal input or push-pull output with software assignable pull-up. Input or output mode is selectable by software. Respectively, each pin can serve as (with noise filters): P3.0/timer D clock input (TDCK) P3.1/timer C clock input (TCCK) P3.2/timer D capture input (TDCAP) P3.3/timer C capture input (TCCAP) P3.4/timer C out (TCOUT)/PWM out (TCPWM) P3.5/timer D out (TDOUT)/PWM out (TDPWM) P3.6/PWM0 output port P3.7/PWM1 output port	3, 5	29–22	TDCK TCCK TDCAP TCCAP TDOUT/ TDPWM TCOUT/ TCPWM PWM0 PWM1
P4.0–P4.7	I/O	General I/O port with bit programmable pins. Normal input or push-pull output with software assignable pull-up. Input or output mode is selectable by software. P4.0–P4.7 can alternately be used as inputs for embedded chip selection output. P4.4/CS0 P4.5/CS1 P4.6/CS2 P4.7/CS3	3, 5	21, 20, 18, 17, 11–8	CS0–CS3

Table 1-1. S3C8454/P8454 Pin Descriptions (Continued)

Pin Name	Pin Type	Pin Description	Circuit Type	QFP Pin Number	Share Pins
P5.0–P5.1	I/O	General I/O port with bit programmable pins. Normal input or push-pull, output mode. Alternately It can use as external interface control signal P5.0/WAIT signal	5	7	WAIT
ADC0–ADC3	I	Analog input pins for A/D converter module. Alternatively used as general-purpose I/O	2	49–46	P0.4–P0.7
AV_{REF}	–	A/D converter reference voltage AV_{SS} is connected to ground internally		50	–
PWM0, PWM1	O	Pulse width modulation output pins	5	23,22	P3.6, P3.7
INT0–INT7	I	External interrupt input pins	4	37–30	P2.0–P2.7
TCCK, TDCK	I	External clock input for timer C and timer D	3	28,29	P3.1/P3.0
TCCAP,TDCAP	I	Timer C/ timer D capture input	3	26,27	P3.3/P3.2
WAIT	I	Input pin for the slow memory timing signal from the external interface	5	7	P5.0
RESET	I	System reset pin (pull-up resistor: 240 kΩ)	1	19	–
EA	I	5V: ROMless operating 0V: internal 4 K and external 60 K addressing mode	–	16	–
V_{DD1}, V_{SS1}	–	Power input pins for CPU operation (internal) and Power input for OTP writing	–	12,13	–
V_{DD2}, V_{SS2}	–	Power input pins for port output (external)	–	53, 52	–
X_{IN}, X_{OUT}	–	Main oscillator pins	–	15, 14	–
SI, SO, SCK	I/O	synchronous SIO communication port	3	40,39,38	P1.5/P1.6 P1.7
A0–A15	O	Address output for external device	6	65–80	–
D0–D7	I/O	Data I/O for external device	7	57–64	–
PM,DM	O	External memory selection output	–	1, 2	–
RD,WR	O	Memory read/write output	–	3, 4	–
CS0–CS3	O	Embedded chip selection output	5	11–8	P4.4–P4.7
TCOUT,TDOUT	O	16-bit timer PWM mode output	5	25, 24	P3.4, P3.5
VLD	–	Voltage Level Detect Pin	–	5	–

NOTE: V_{DD1} must be connected to V_{DD2} in users application circuit, V_{SS1} & V_{SS2} also.

PIN CIRCUITS

Table 1-2. Pin Circuit Assignments for the S3C8454/P8454

Circuit Number	Circuit Type	S3C8454 Assignments
1	Input	RESET pin
2	I/O	A/D converter input pins, ADC0–ADC3, P0.4–P0.7
3	I/O	Port 0, 1, 3, 4, and 5
4	I/O	P2 (INT0–INT7)
5	I/O	P3 (TDCK, TCCK, TDCAP, TCCAP, TCOUT, TDOUT, TCPWM, TDPWM, PWM0, PWM1)
6	Output	A0–A15,PM, DM, RD, WR
7	I/O	D0–D7

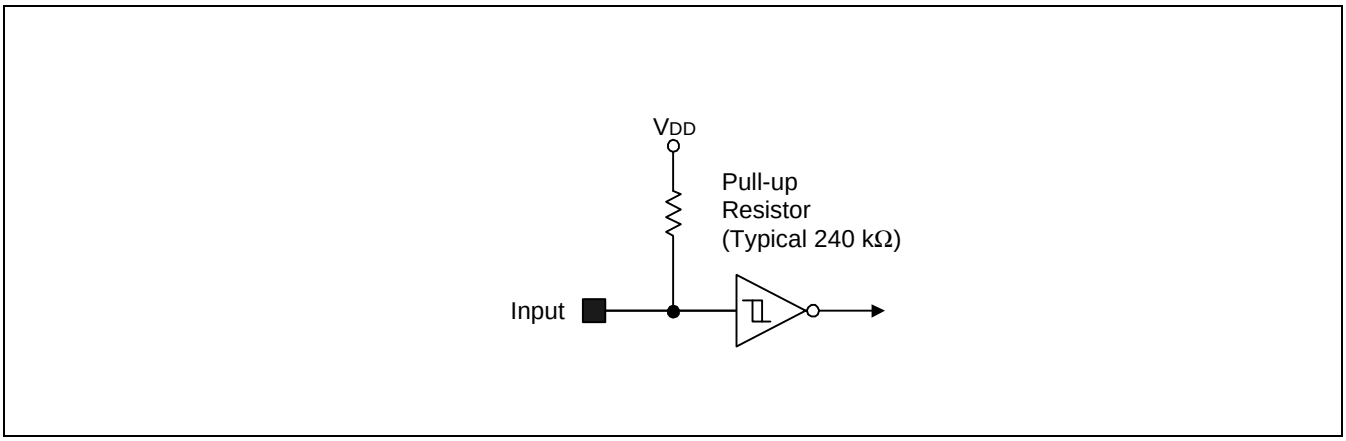


Figure 1-4. Pin Circuit Type 1 (RESET)

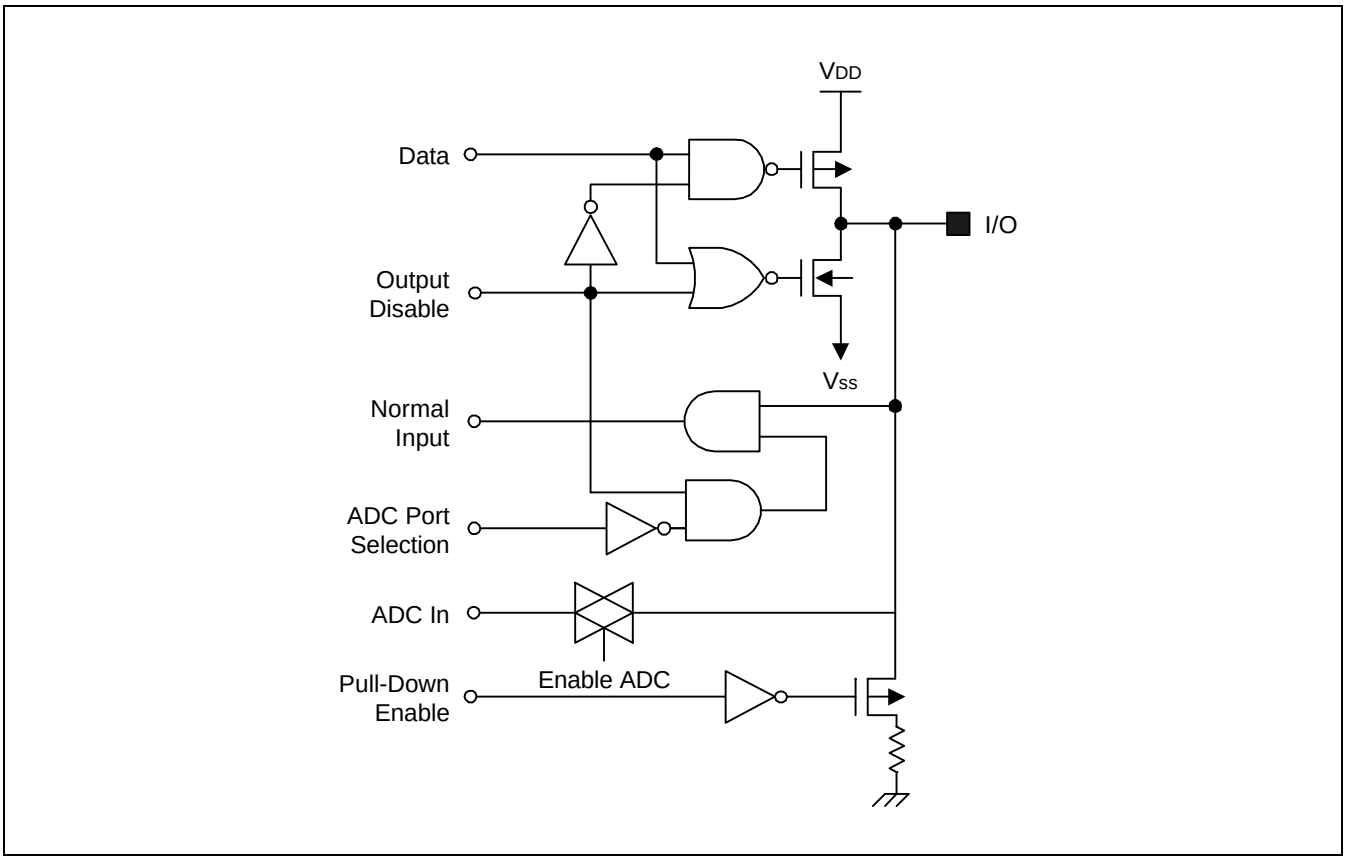


Figure 1-5. Pin Circuit Type 2 (ADC0–ADC3)

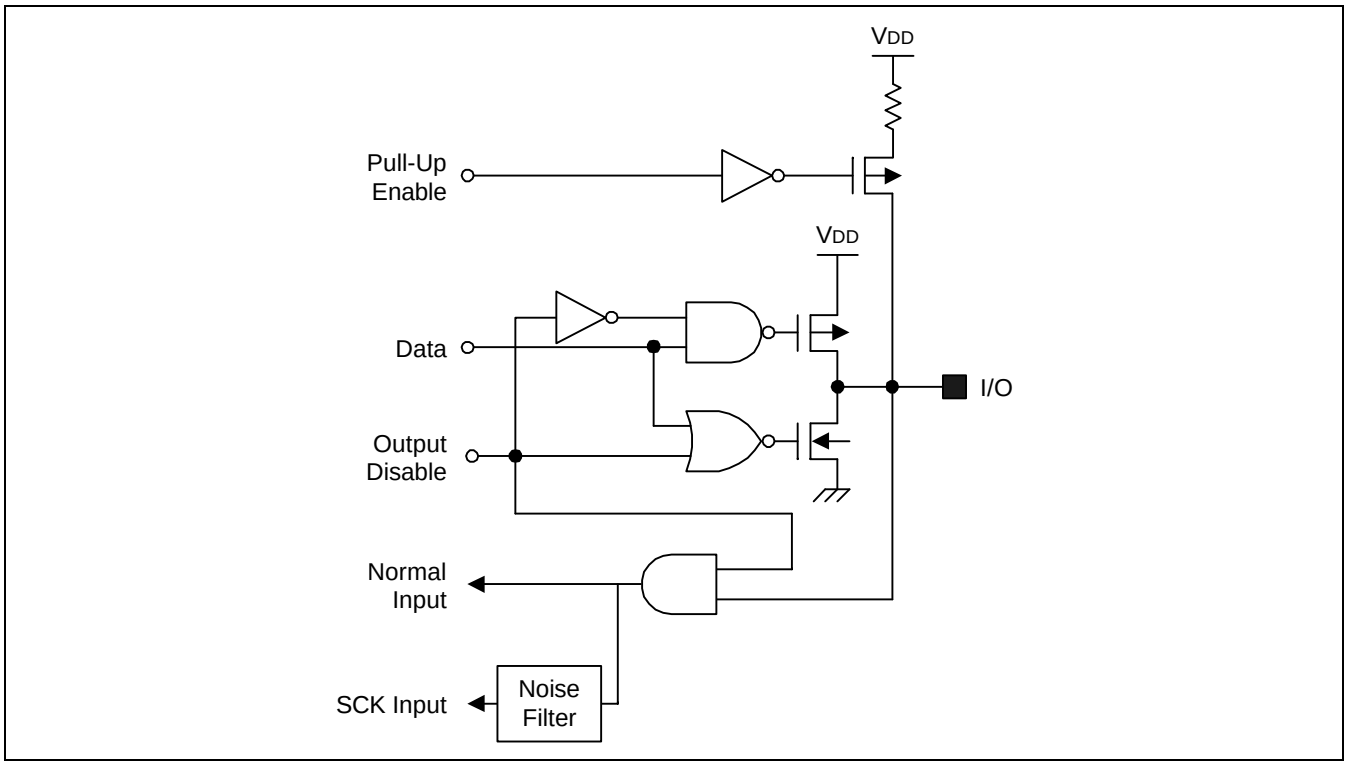


Figure 1-6. Pin Circuit Type 3

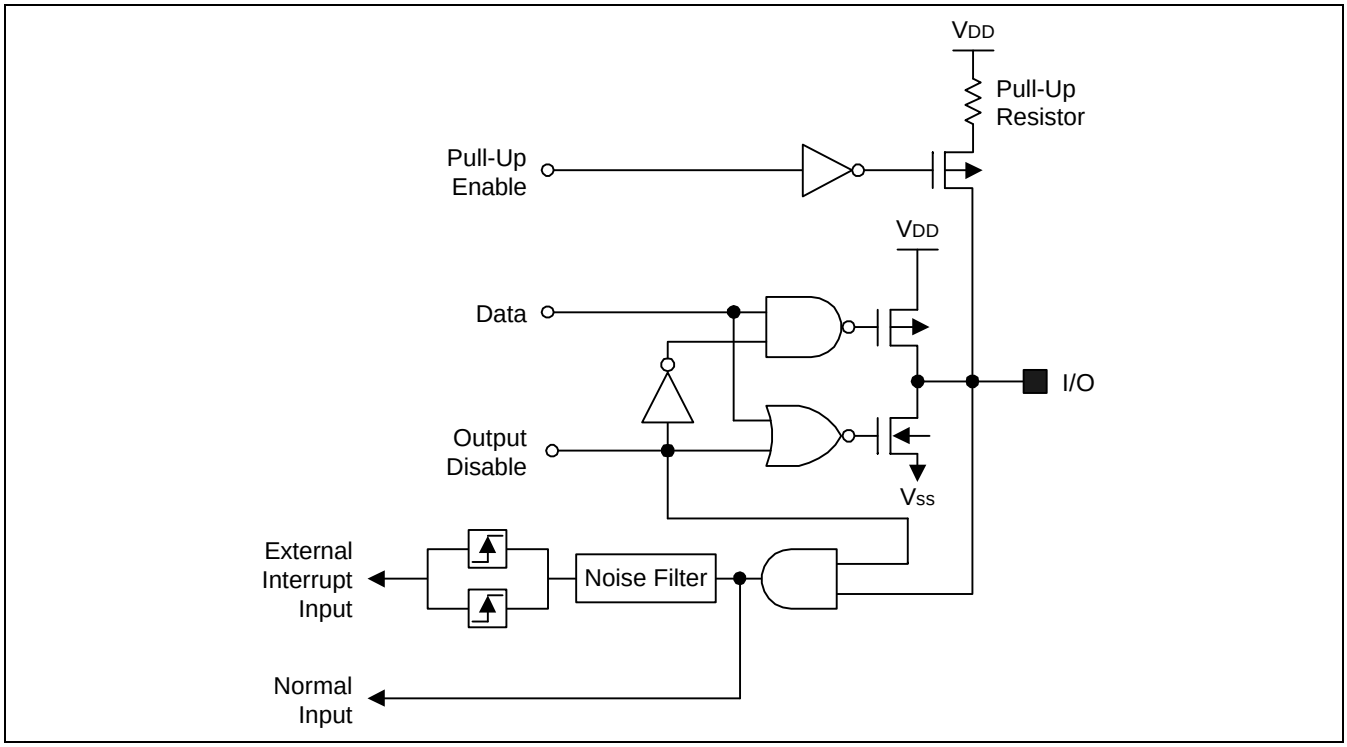


Figure 1-7. Pin Circuit Type 4

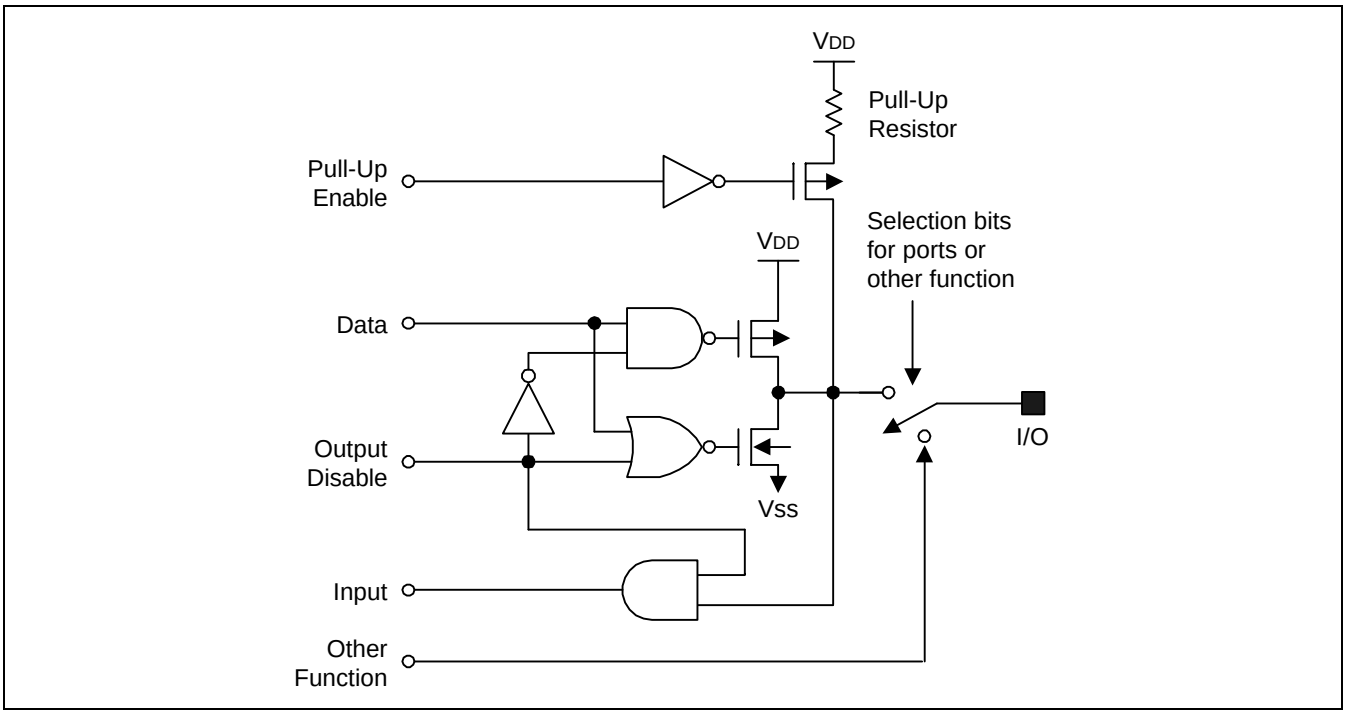


Figure 1-8. Pin Circuit Type 5

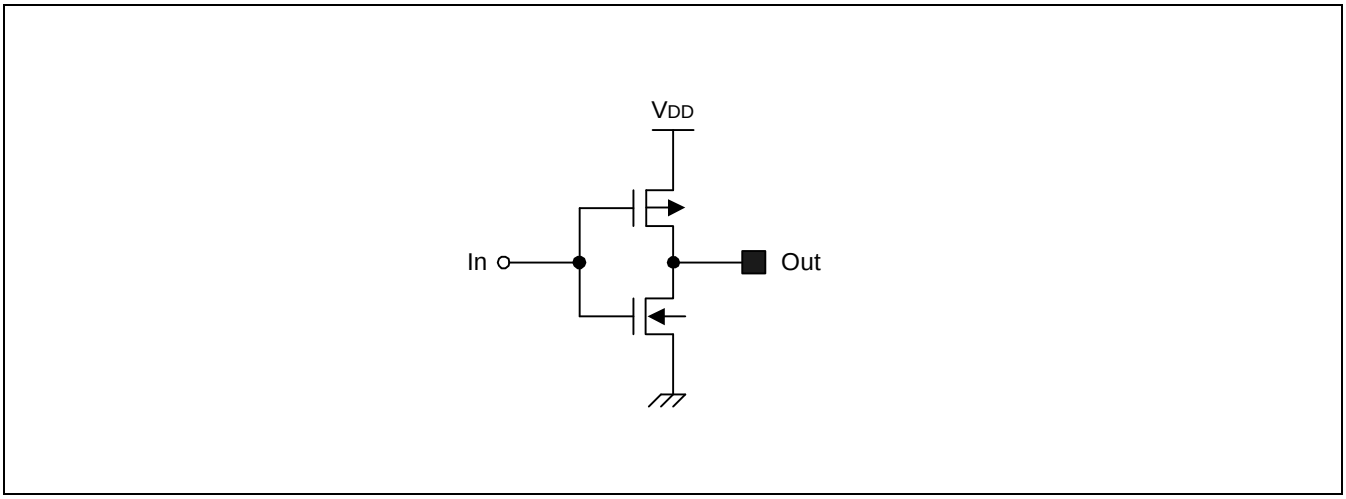


Figure 1-9. Pin Circuit Type 6

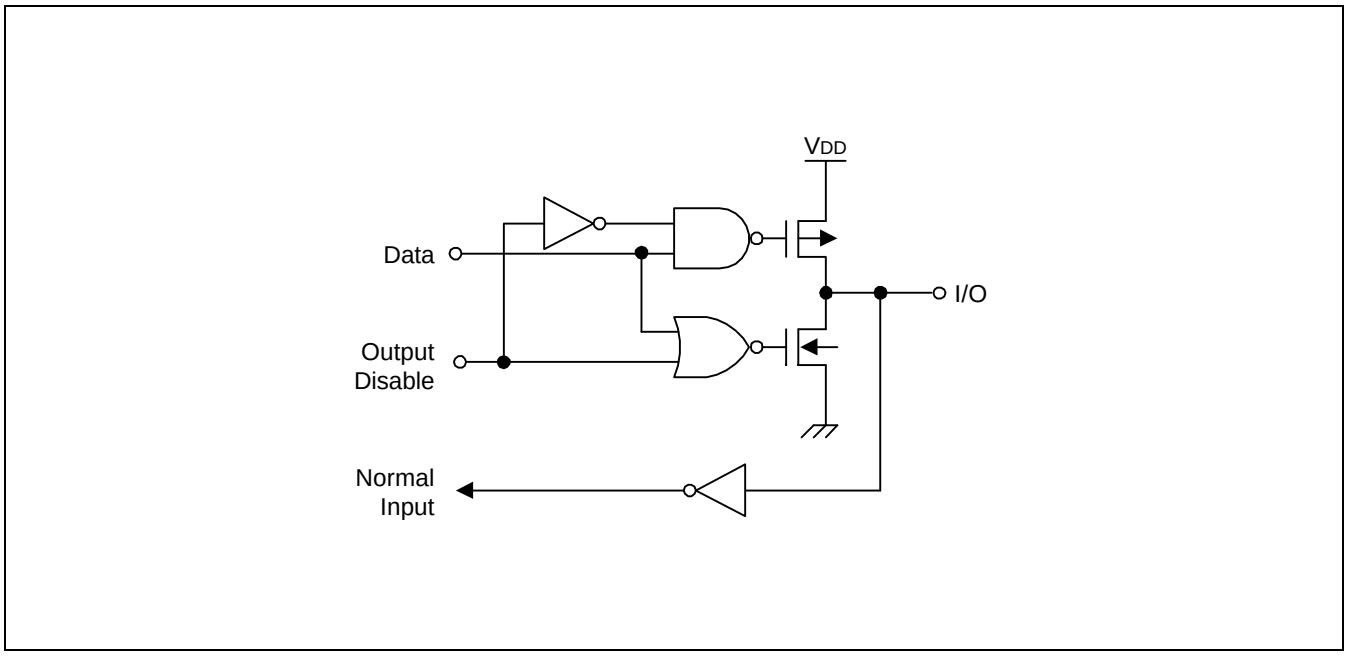


Figure 1-10. Pin Circuit Type 7

18 ELECTRICAL DATA

OVERVIEW

In this section, S3C8454 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

— Absolute maximum ratings
— D.C. electrical characteristics
— A.C. electrical characteristics
— I/O capacitance
— Oscillation characteristics
— Oscillation stabilization time

Table 18-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}		– 0.3 to + 6.5	V
Input voltage	V_I	All ports (in input mode)	– 0.3 to V_{DD} + 0.3	
Output voltage	V_O	All ports (in output mode)	– 0.3 to V_{DD} + 0.3	V
Output current high	I_{OH}	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output current low	I_{OL}	One I/O pin active	+ 30	mA
		Total pin current for port	+ 100	
Operating temperature	T_A		– 40 to +85	°C
Storage temperature	T_{STG}		– 65 to +150	°C

Table 18-2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating voltage	V_{DD}	f_{OSC} = 25 MHz (instruction clock = 6.25 MHz)	4.5	–	5.5	V
		f_{OSC} = 12 MHz (instruction clock = 3 MHz)	2.7	–	5.5	
Input high voltage	V_{IH1}	All input pins except V_{IH2}, V_{IH3}	0.51 V_{DD}	–	V_{DD}	V
	V_{IH2}	X_{IN}	V_{DD} – 0.5			
	V_{IH3}	Test, RESET	0.8V_{DD}			
Input low voltage	V_{IL1}	All input pins except V_{IL2}, V_{IL3}	–	–	0.2 V_{DD}	V
	V_{IL2}	X_{IN}			0.4	
	V_{IL3}	Test, RESET	0.2V_{DD}		–	
Output high voltage	V_{OH}	V_{DD}= 5 V I_{OH} = – 1 mA	V_{DD} – 1.0	–	–	V
		I_{OH} = – 100 uA	V_{DD} – 0.5	–	–	
Output low voltage	V_{OL1}	V_{DD} = 5 V I_{OL} = 2 mA All output pins except port 2	–	–	0.4	V
	V_{OL2}	V_{DD} = 5 V I_{OL} = 15 mA, port 2	–	0.5	1.0	
Input high leakage current	I_{LIH1}	V_{IN} = V_{DD} All input pins except X_{IN}	–	–	3	µA
	I_{LIH2}	V_{IN} = V_{DD} X_{IN}			20	
Input low leakage current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{IN} and RESET	–	–	– 3	
	I_{LIL2}	V_{IN} = 0 V, $X_{IN,}$ RESET			– 20	
Output high leakage current	I_{LOH}	V_{OUT} = V_{DD} All I/O pins and output pins	–	–	5	
Output low leakage current	I_{LOL}	V_{OUT} = 0 V All I/O pins and output pins	–	– 0	– 5	
Pull-up and pull-down resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% Ports 0-5, T_A = 25 °C	30	46	80	kΩ
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% T_A = 25 °C, RESET only	120	240	320	

Table 18-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current (note)	I_{DD1}	V_{DD} = 5 V ± 10 % 20 MHz oscillation		20	40	mA
		V_{DD} = 2.7 V 12 MHz oscillation		7	14	
	I_{DD2}	Idle mode; V_{DD} = 5 V ± 10 % 20 MHz oscillation		8	16	
		Idle mode; V_{DD} = 2.7 V 12 MHz oscillation		3	6	
	I_{DD3}	Stop mode; V_{DD} = 5 V ± 10 % LVD enable, T_A = 25 °C		110	220	µA

NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.

Table 18-3. A.C. Electrical Characteristics

(T_A = -40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt input high, low width (P2.0–P2.7)	t_{INTH}, t_{INTL}	V_{DD} = 5 V	180	–	–	nS
RESET input low width	t_{RSL}	V_{DD} = 5 V	1000	–	–	nS

NOTES:
1. The unit t_{CPU} means one CPU clock period.
2. The oscillator frequency is the same as the CPU clock frequency.

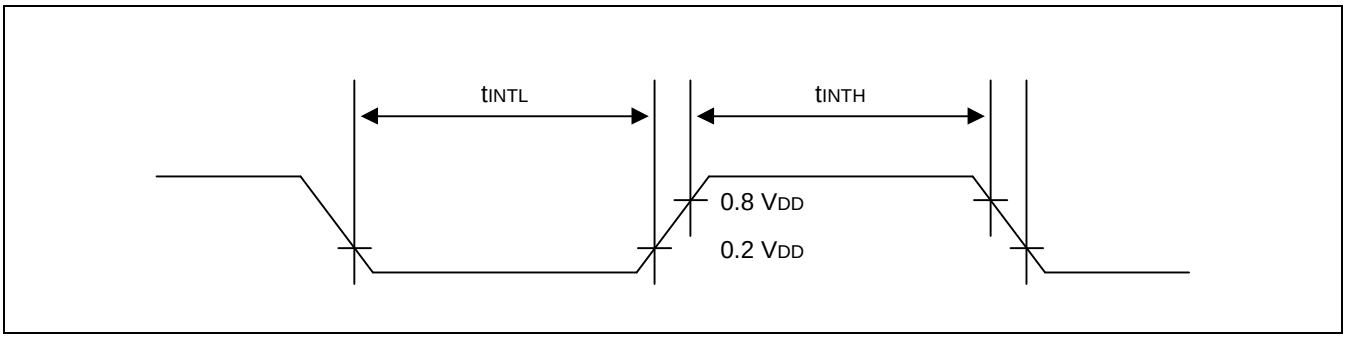


Figure 18-1. Input Timing for External Interrupts (Ports 2)

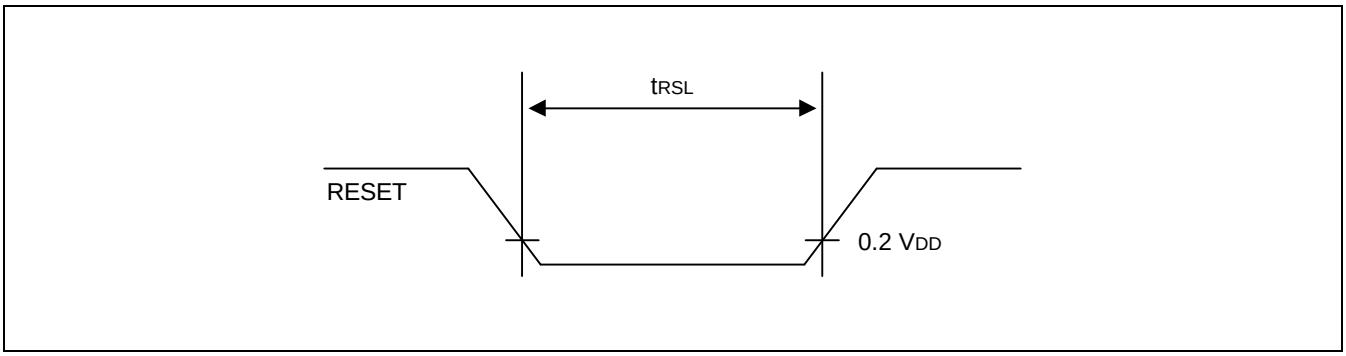


Figure 18-2. Input Timing for RESET

Table 18-4. Input/Output Capacitance

(T_A = – 40 °C to + 85 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	f = 1 MHz; unmeasured pins are connected to V_{SS}	–	–	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

Table 18-5. Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}		2	–	5.5	V
Data retention supply current	I_{DDDR}	Stop mode, V_{DDDR} = 2.0 V	–	–	50	µA

NOTES:
1. During the oscillator stabilization wait time (t_{WAIT}), all CPU operations must be stopped.
2. Supply current does not include drawn through internal pull–up resistors and external output current loads.

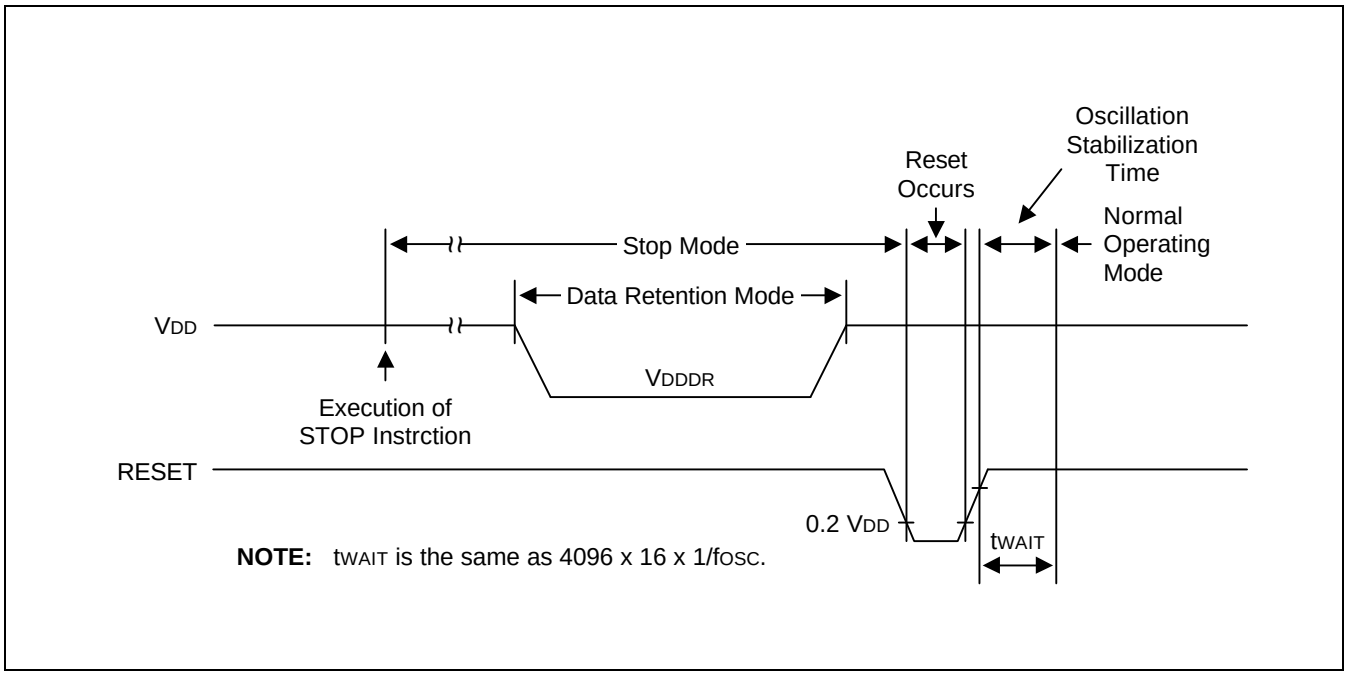


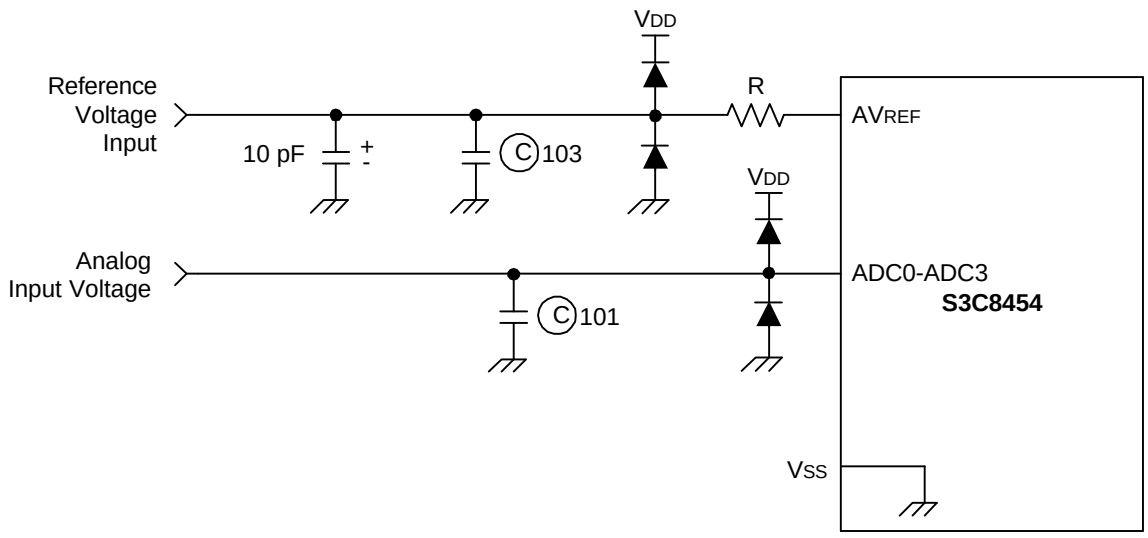
Figure 18-3. Stop Mode Release Timing Initiated by RESET

Table 18-6. A/D Converter Electrical Characteristics

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resolution			–	8	–	bit
Total accuracy		V_{DD} = 5 V	–	–	± 2	LSB
Integral linearity error	ILE	Conversion time = 5 us		–	± 1	
Integral linearity error	DLE	AV_{REF} = 5 V		–	± 1	
Offset error of top	EOT	AV_{SS} = 0 V		± 1	± 2	
Offset error of bottom	EOB			± 0.5	± 2	
Conversion time (1)	t_{CON}		17	–	170	µs
Analog input voltage	V_{IAN}		AVss	–	AV_{REF}	V
Analog input impedance	R_{AN}	–	2	1000	–	MΩ
Analog reference voltage	AV_{REF}	–	2.5	–	V_{DD}	V
Analog ground	AV_{SS}	–	V_{SS}	–	V_{SS}+ 0.3	V
Analog input current	I_{ADIN}	AV_{REF} = V_{DD} = 5 V	–	–	10	uA
Analog block current (2)	I_{ADC}	AV_{REF} = V_{DD} = 5 V		1	3	mA
		AV_{REF} = V_{DD} = 3 V		0.5	1.5	mA
		AV_{REF} = V_{DD} = 5 V When power down mode		100	500	nA

NOTES:
1. 'Conversion time' is the time required from the moment a conversion operation starts until it ends.
2. I_{ADC} is an operating current during A/D conversion.



NOTE: The symbol 'R' signifies an offset resistor with a value of from 50 to 100.
If this resistor is omitted, the absolute accuracy will be maximum of 3 LSBs.

Figure 18-4. Recommended A/D Converter Circuit for Highest Absolute Accuracy

Table 18-7. Synchronous SIO Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 4.5 V to 5.5 V, V_{SS} = 0 V, f_{OSC} = 10 MHz oscillator)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SCK cycle time	t_{CYC}	–	200	–	–	nS
Serial clock high width	t_{SCKH}	–	60	–	–	
Serial clock low width	T_{SCKL}	–	60	–	–	
Serial output data delay time	T_{OD}	–	–	–	50	
Serial input data set up time	T_{ID}	–	40	–	–	
Serial input data hold time	T_{IH}	–	100	–	–	

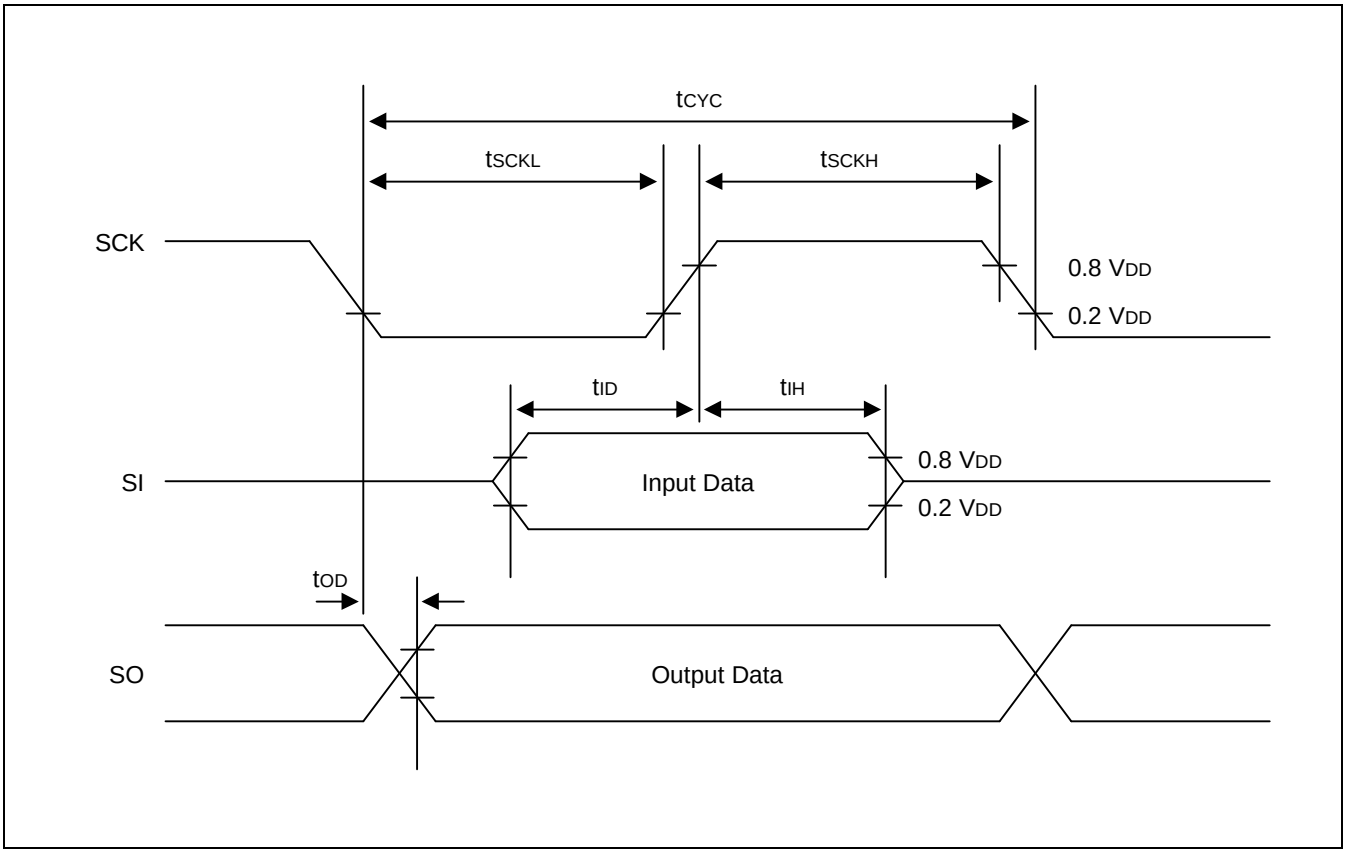


Figure 18-5. Serial Data Transfer Timing

Table 18-8. Main Oscillator Frequency (f_{OSC1})

(T_A = – 40 °C + 85 °C, V_{DD} = 4.5 V to 5.5 V)

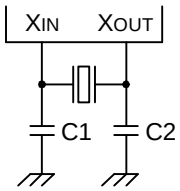
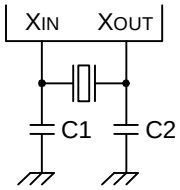
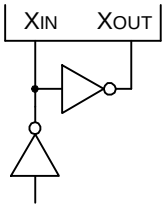
Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
Crystal		CPU clock oscillation frequency	4	–	25	MHz
Ceramic		CPU clock oscillation frequency	4	–	25	MHz
External clock		X_{IN} input frequency	4	–	25	MHz

Table 18-9. Main Oscillator Clock Stabilization Time (t_{ST1})

(T_A = -40 °C + 85 °C, V_{DD} = 4.5 V to 5.5 V)

Oscillator	Test Condition	Min	Typ	Max	Unit
Crystal	V_{DD} = 4.5 V to 5.5 V	–	–	10	ms
Ceramic	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	4	ms
External clock	X_{IN} input high and low level width (t_{XH}, t_{XL})	50	–	–	ns

NOTE: Oscillation stabilization time (tST1) is the time required for the CPU clock to return to its normal oscillation frequency after a power-on occurs, or when Stop mode is ended by a RESET signal. The RESET should therefore be held at low level until the t_{ST1} time has elapsed.

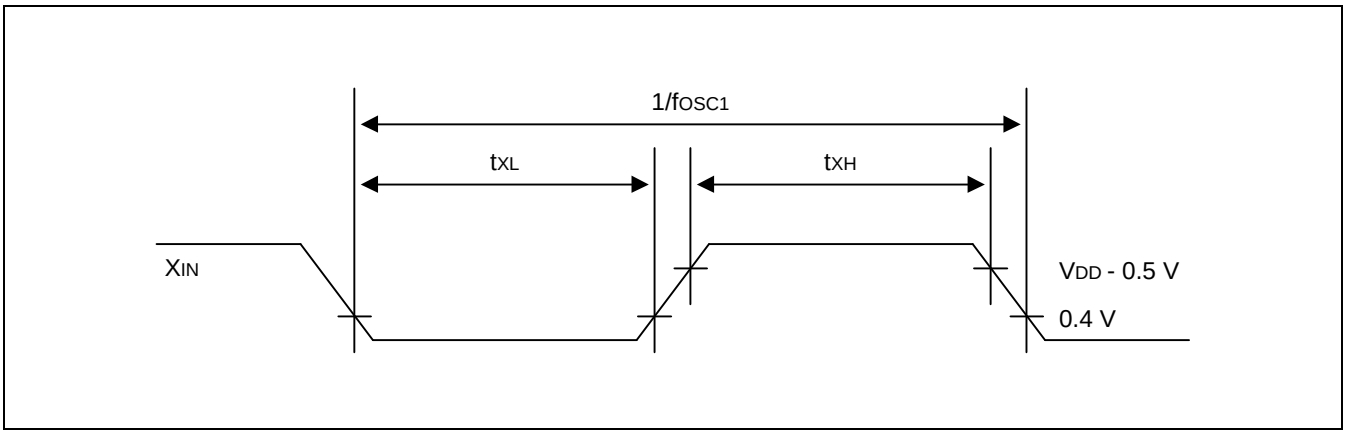
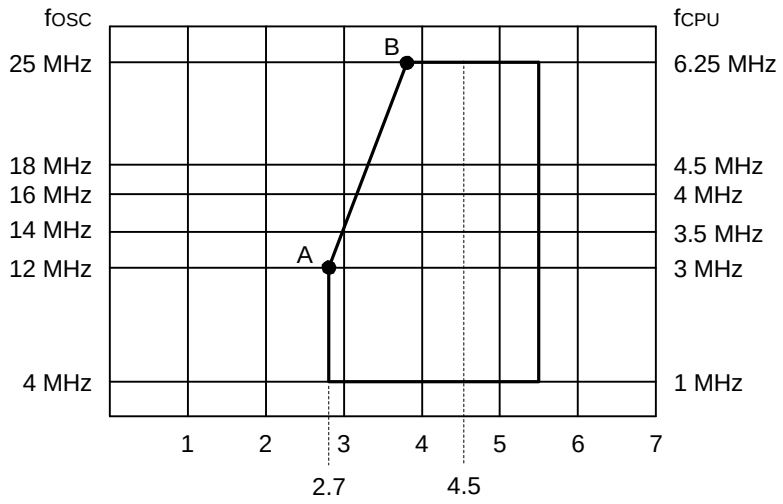


Figure 18-6. Clock Timing Measurement at X_{IN}

Table 18-10. Characteristics of Voltage Level Detect circuit

(T_A = – 40 °C + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage of VLD	V_{DDVLD}	–	2.7	–	5.5	V
Detect Voltage	V_{VLD}	–	1.15	1.40	1.51	V
Current consumption	I_{VLD}	V_{DD} = 5.5 V	–	100	200	uA



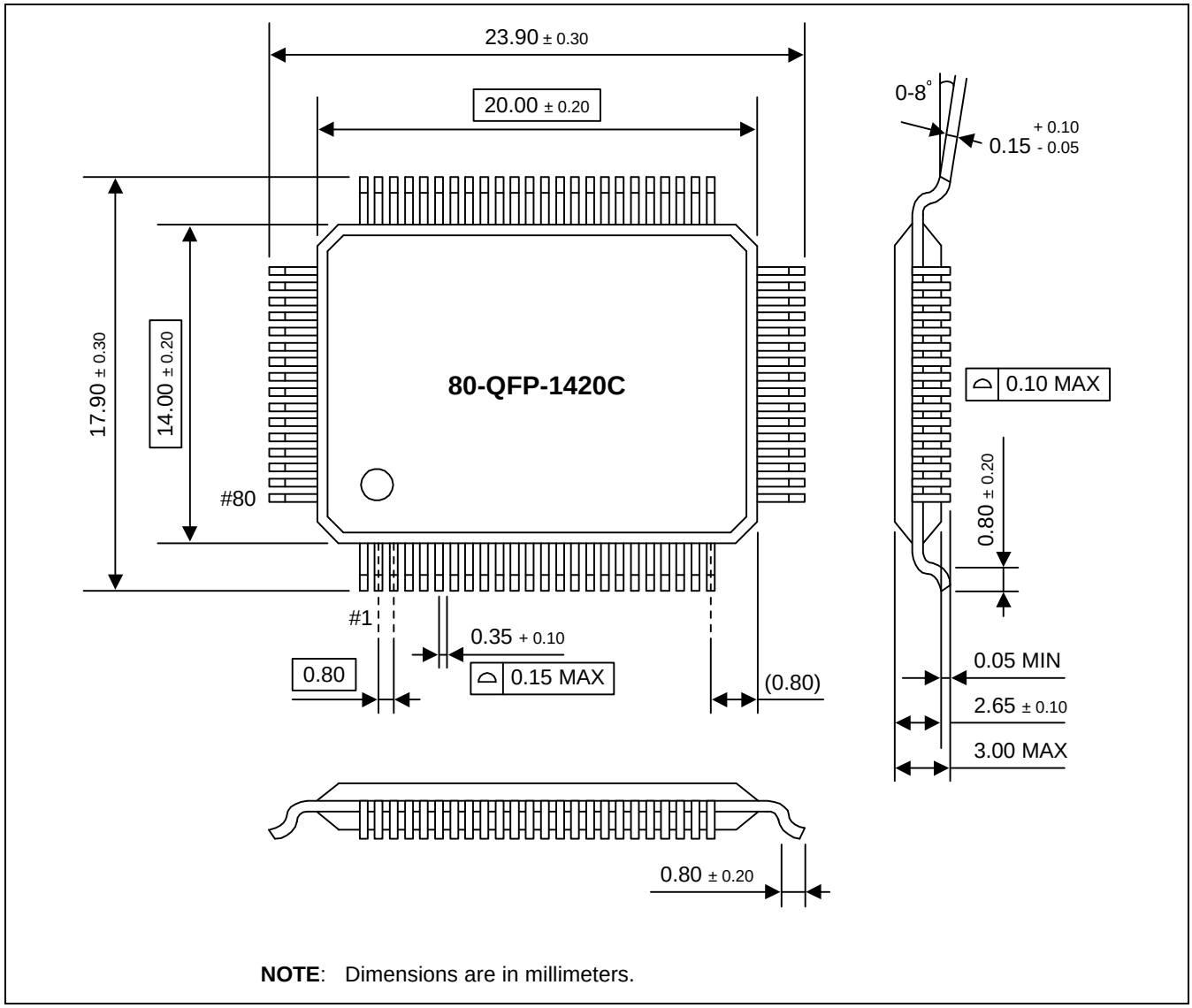
Instruction Clock = 1/4n x oscillator frequency (n = 1, 2, 8, 16)

Figure 18-7. Operating Voltage Range

19 MECHANICAL DATA

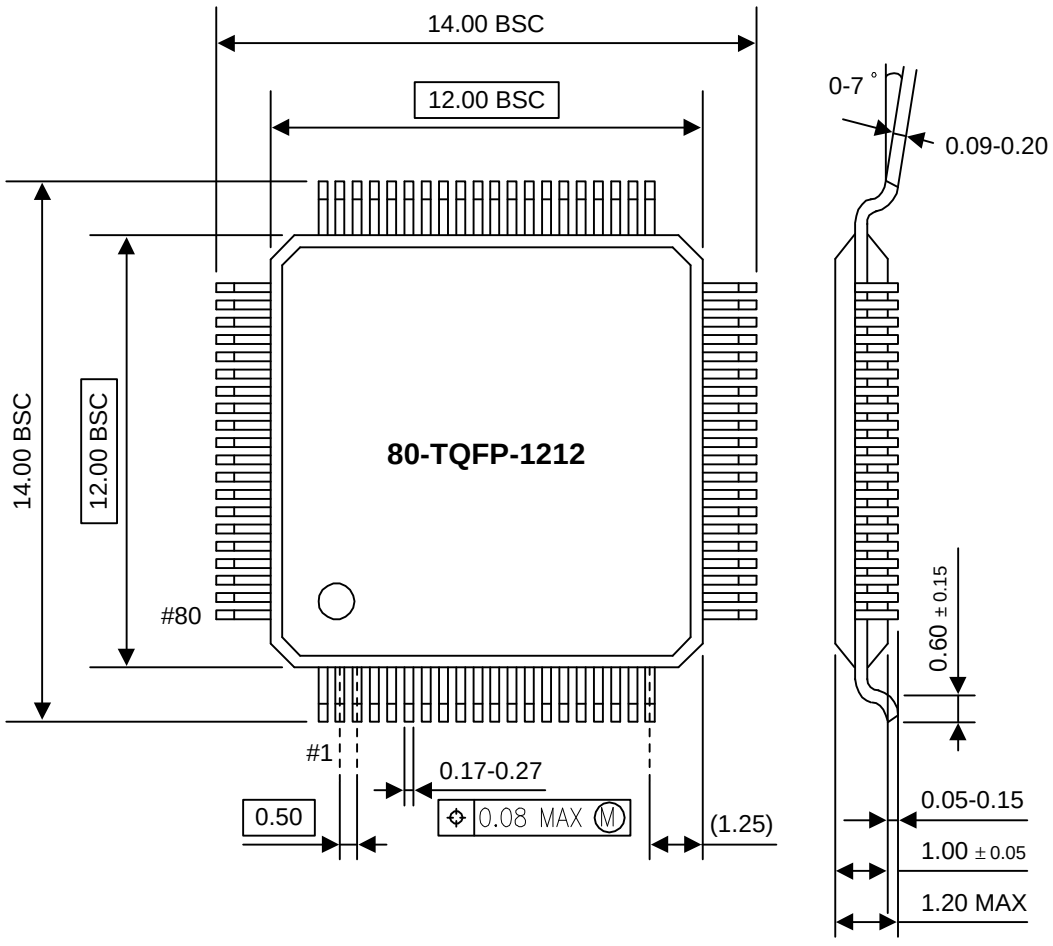
OVERVIEW

The S3C8454 microcontroller is available in a 80-pin QFP package (80-QFP-1420C) and a 80-pin TQFP package (80-TQFP-1212AN).



NOTE: Dimensions are in millimeters.

Figure 19-1. 80-QFP-1420C Package Dimensions



NOTE: Dimensions are in millimeters.

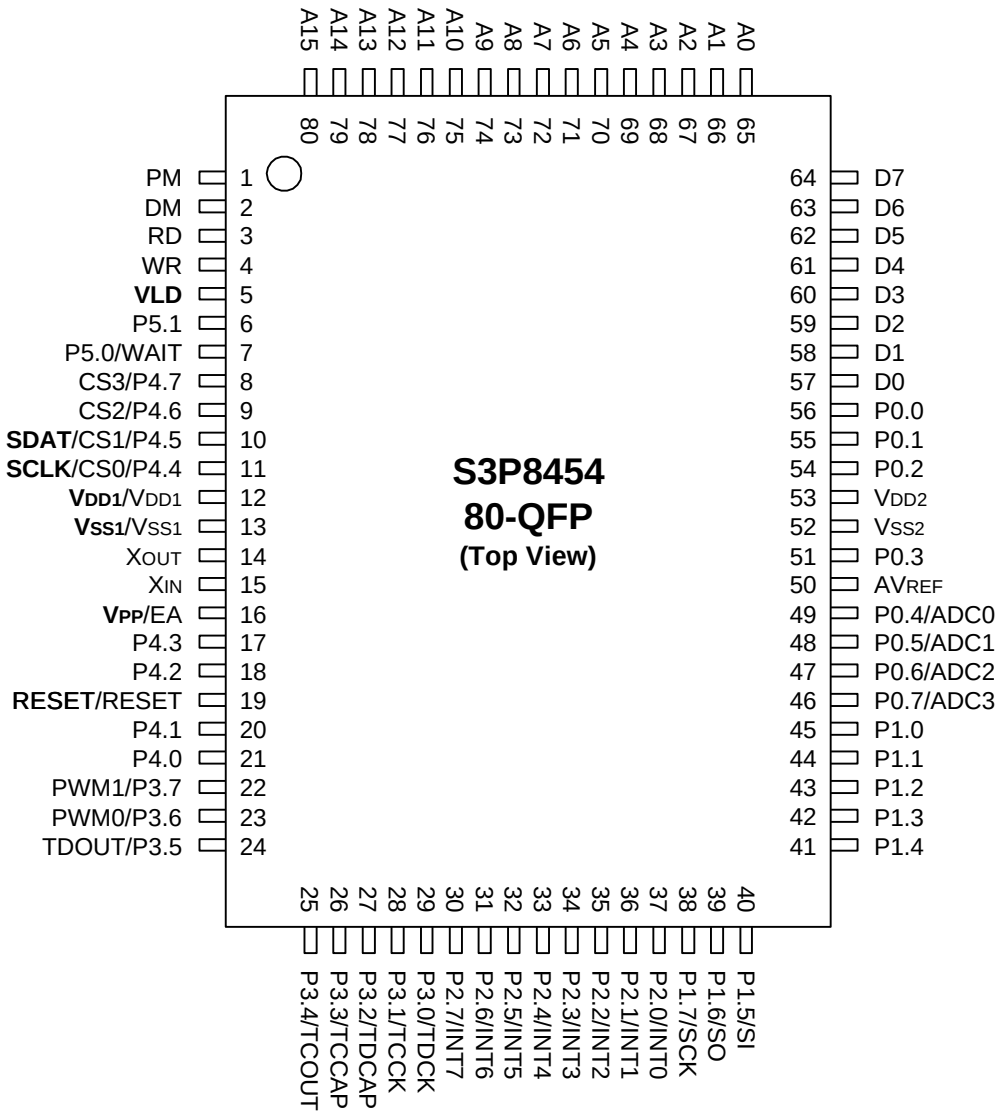
Figure 19-2. 80-TQFP-1212AN Package Dimensions

20 S3P8454 OTP

OVERVIEW

The S3P8454 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C8454 microcontrollers. It has an on-chip EPROM instead of masked ROM. The EPROM is accessed by serial data format.

S3P8454 is fully compatible with S3C8454, both in function and in pin configuration. As it has simple programming requirements, S3P8454 is ideal for use as an evaluation chip for the S3C8454.



NOTE: The bolds indicates OTP pin name.

Figure 20-1. S3P8454 Pin Assignments (80-QFP Package)

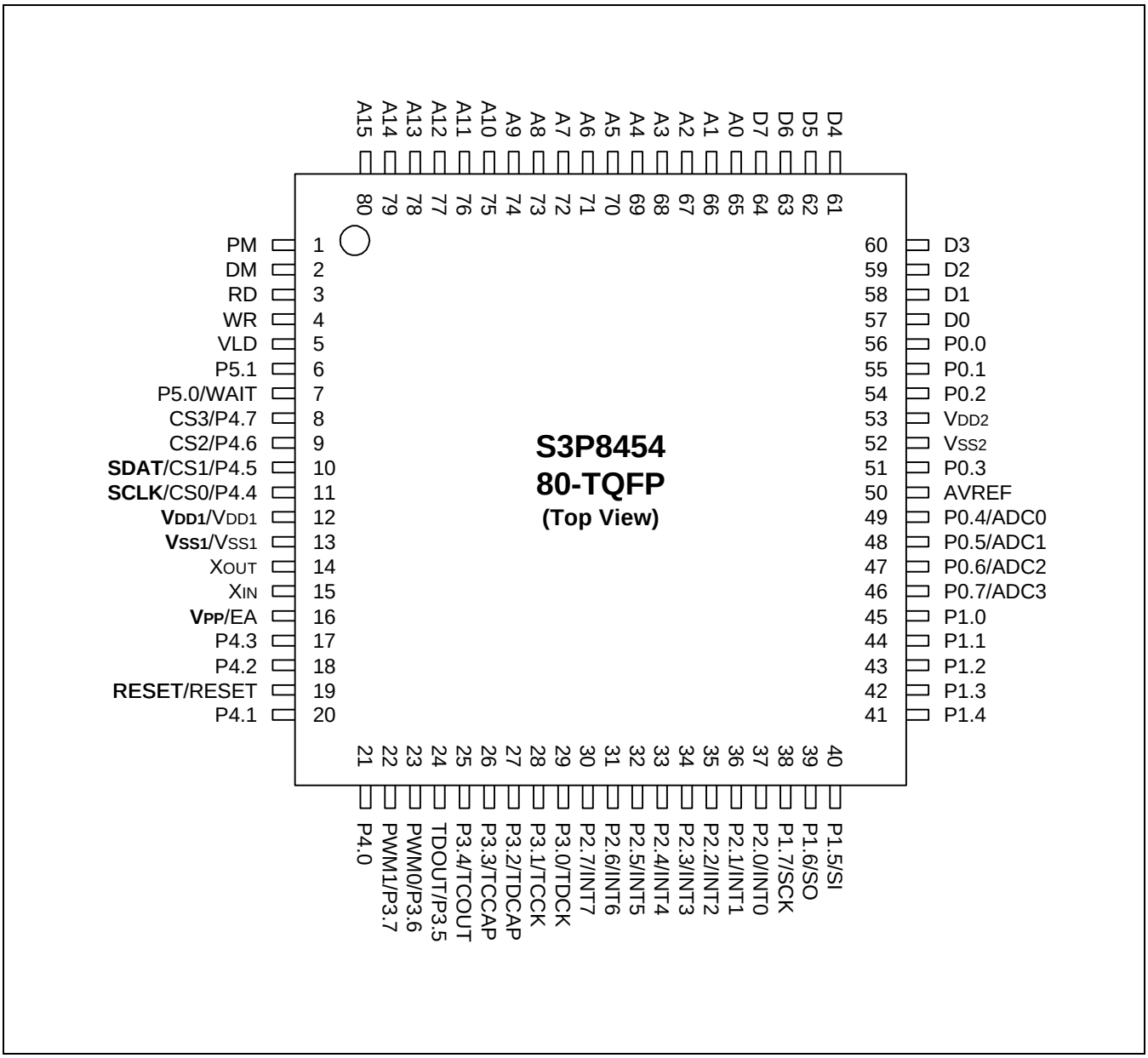


Figure 20-2. S3P8454 Pin Assignments (80-TQFP Package)

Table 20-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	Pin Name	Pin No.	I/O	Function
P4.5	SDAT	10	I/O	Serial data pin (Output when reading, Input when writing) Input and push-pull output port can be assigned.
P4.4	SCLK	11	I	Serial clock pin (Input only pin)
EA	V_{PP}	16	I	EPROM cell writing power supply pin (Indicates OTP mode entering) When writing 12.5 V is applied and when reading 5 V is applied (Option).
RESET	RESET	19	I	Chip Initialization
V_{DD1}/V_{SS1}	V_{DD}/V_{SS}	12/13	I	Logic Power Supply Pin. V_{DD} should be tied to 5 V during programming.

Table 20-2. Comparison of S3P8454 and S3C8454 Features

Characteristic	S3P8454	S3C8454
Program Memory	4 Kbyte EPROM	4 Kbytes mask ROM
Operating Voltage (V_{DD})	2.7 V to 5.5 V	2.7 V to 5.5V
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (TEST) = 12.5V	
Pin Configuration	80 QFP, 80 TQFP	80 QFP, 80 TQFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP} (TEST) pin of S3P8454, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 20-3 below.

Table 20-3. Operating Mode Selection Criteria

V_{DD}	V_{PP} (TEST)	REG /MEM	Address (A15–A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

D.C. ELECTRICAL CHARACTERISTICS

Table 20-4. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating voltage	V_{DD}	f_{OSC} = 25 MHz (instruction clock = 6.25 MHz)	4.5	–	5.5	V
		f_{OSC} = 12 MHz (instruction clock = 3 MHz)	2.7	–	5.5	
Input high voltage	V_{IH1}	All input pins except V_{IH2}, V_{IH3}	0.51 VDD	–	V_{DD}	V
	V_{IH2}	X_{IN}	V_{DD} – 0.5			
	V_{IH3}	Test, RESET	0.8V_{DD}			
Input low voltage	V_{IL1}	All input pins except V_{IL2}, V_{IL3}	–	–	0.2 V_{DD}	V
	V_{IL2}	X_{IN}			0.4	
	V_{IL3}	Test, RESET	0.2V_{DD}		–	
Output high voltage	V_{OH}	V_{DD}= 5 V I_{OH} = – 1 mA	V_{DD} – 1.0	–	–	V
		I_{OH} = – 100 uA	V_{DD} – 0.5	–	–	
Output low voltage	V_{OL1}	V_{DD} = 5 V, I_{OL} = 2 mA All output pins except port 2	–	–	0.4	V
	V_{OL2}	V_{DD} = 5 V, I_{OL} = 15 mA, port 2	–	0.5	1.0	
Input high leakage current	I_{LIH1}	V_{IN} = V_{DD} All input pins except X_{IN}	–	–	3	µA
	I_{LIH2}	V_{IN} = V_{DD}, X_{IN}			20	
Input low leakage current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{IN} and RESET	–	–	– 3	
	I_{LIL2}	V_{IN} = 0 V, X_{IN}, RESET			– 20	
Output high leakage current	I_{LOH}	V_{OUT} = V_{DD} All I/O pins and output pins	–	–	5	
Output low leakage current	I_{LOL}	V_{OUT} = 0 V All I/O pins and output pins	–	– 0	– 5	
Pull-up and pull-down resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% Ports 0-5, T_A = 25 °C	30	46	80	kΩ
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V ± 10% T_A = 25 °C, RESET only	120	240	320	

Table 20-4. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output high leakage current	I_{LOH}	$V_{OUT} = V_{DD}$ All I/O pins and output pins	–	–	5	µA
Output low leakage current	ILOL	V_{OUT} = 0 V All I/O pins and output pins	–	– 0	– 5	
Pull-up and pull-down resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V ± 10 % Ports 0-5, T_A = 25 °C	30	46	80	kΩ
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V ± 10 % T_A = 25 °C, RESET only	120	240	320	
Supply current (note)	I_{DD1}	V_{DD} = 5 V ± 10 % 20 MHz oscillation	–	20	40	mA
		V_{DD} = 2.7 V 12 MHz oscillation		7	14	
	I_{DD2}	Idle mode; V_{DD} = 5 V ± 10 % 20 MHz oscillation		8	16	
		Idle mode; V_{DD} = 2.7 V 12 MHz oscillation		3	6	
	I_{DD3}	Stop mode; V_{DD} = 5 V ± 10%, LVD enable		110	220	µA

NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.