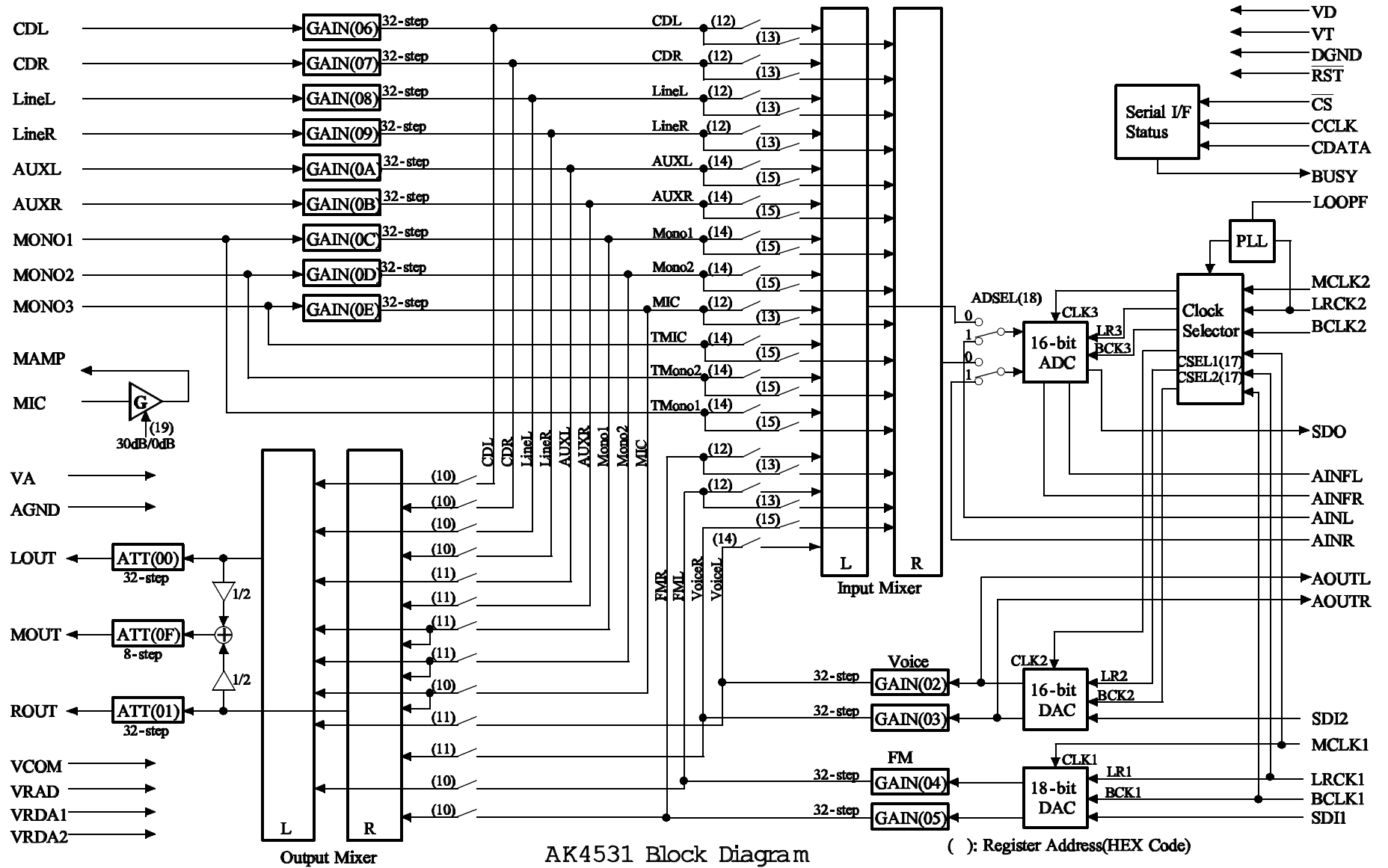


General Description

The AK4531A is a two channel 16bit AUDIO Hi-Fi CODEC (ADC and DAC) with a sampling rate of 4kHz to 50kHz and includes a 2 channel 18bit DAC designed to work together with an extra sound source. Each converter can also operate by independent sampling rates. Its internal recording and playback mixer has 5 channel stereo and 3 channel mono with L/R, R/L, L/L and R/R switching. The AK4531A also has an internal 30dB microphone amplifier. Its master clock is 256 times of f_s and an internal PLL can also automatically generates 256 f_s for master clock from f_s . The sampling ADC has an enhanced dual bit delta sigma modulator. Both the 16bit and 18bit DAC have low outband noise and high jitter tolerance due to a switched capacitor filter(SCF) and a continuous time filter(CTF). The AK4531A corresponds to a 3.3V digital interface, performing with a low power dissipation of 315mW. The package is a low profile 44pin LQFP.

Features

- 2ch Audio CODEC with low outband noise DAC
- 2ch 18bit Extra Audio DAC
- Standard Serial Interface for CODEC & DAC
- CODEC & DAC Dynamic Range: 87dB
- High Jitter Tolerance
- 5ch stereo & 3ch mono recording mixer
with L/R, R/L, L/L and R/R switching
- 5ch stereo & 3ch mono playback mixer
- Input PGA with 32levels & 2dB step
- 30dB microphone amplifier
- 3-wire Serial Interface for Mixer Control
- Sampling Rate: 4kHz ~ 50kHz
- Independent Sampling Rates for Each Converter
- Master Clock: 256 f_s
- On chip PLL for deriving 256 f_s master clock from f_s clock
- Corresponding to a 3.3V digital interface
- Low Power Dissipation: 315mW
- Low Profile Package: 44pin LQFP
- AK4531 Pin Compatible



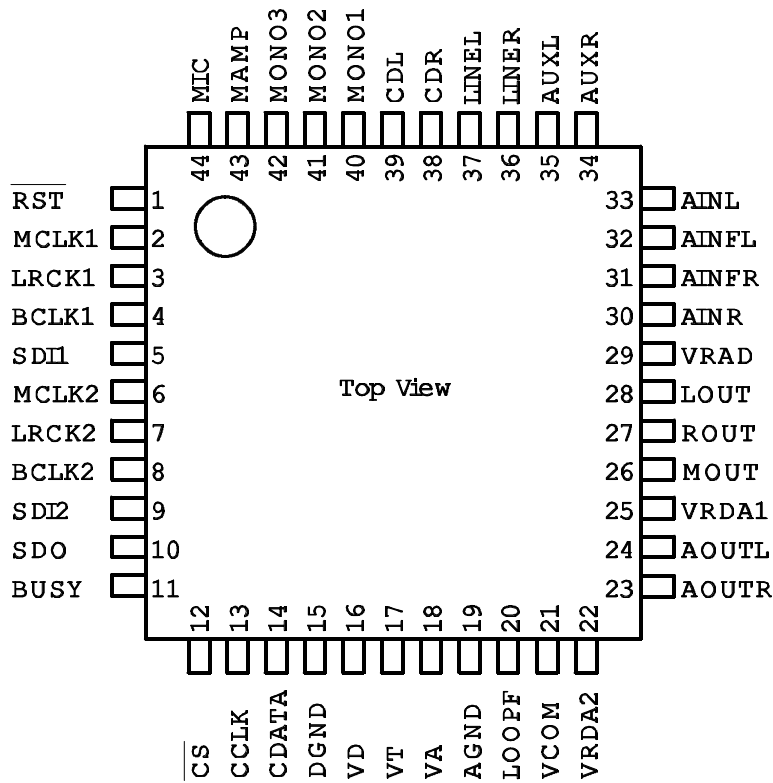
AK4531 Block Diagram

(): Register Address(HEX Code)

Ordering Guide

| | | |
|------------|------------------|-------------------------|
| AK4531A-VQ | -10 ~ +70 | 44pin LQFP(0.8mm pitch) |
| AKD4531 | Evaluation Board | |

Pin Layout



| PIN/FUNCTION | | | |
|--------------------------------------|----------|-----|-----------------------------|
| No. | Pin Name | I/O | Function |
| Analog Inputs/Outputs : 16pin | | | |
| 39 | CDL | I | Lch #1 Line Level Input Pin |
| 38 | CDR | I | Rch #1 Line Level Input Pin |
| 37 | LineL | I | Lch #2 Line Level Input Pin |
| 36 | LineR | I | Rch #2 Line Level Input Pin |
| 35 | AUXL | I | Lch #3 Line Level Input Pin |
| 34 | AUXR | I | Rch #3 Line Level Input Pin |
| 40 | MONO1 | I | Mono #1 Input Pin |
| 41 | MONO2 | I | Mono #2 Input Pin |
| 44 | MIC | I | MIC Input Pin |
| 28 | LOUT | O | Lch Line Level Output Pin |
| 27 | ROUT | O | Rch Line Level Output Pin |
| 26 | MOUT | O | Mono Output Pin |
| 33 | AINL | I | Lch ADC Input Pin |
| 30 | AINR | I | Rch ADC Input Pin |
| 24 | AOUTL | O | Lch DAC Output Pin |
| 23 | AOUTR | O | Rch DAC Output Pin |
| Serial Audio Interface : 9pin | | | |
| 2 | MCLK1 | I | Extra DAC Master Clock |
| 3 | LRCK1 | I | Extra DAC L/R Clock |
| 4 | BCLK1 | I | Extra DAC Bit Clock |
| 5 | SDI1 | I | Extra Data Input |
| 6 | MCLK2 | I | CODEC Master Clock |
| 7 | LRCK2 | I | CODEC L/R Clock |
| 8 | BCLK2 | I | CODEC Bit Clock |
| 9 | SDI2 | I | CODEC-DAC Data Input |
| 10 | SDO | O | CODEC-ADC Data Output |
| Serial Control Data Interface : 3pin | | | |
| 12 | CS | I | Chip Select |
| 13 | CCLK | I | Control Interface Clock |
| 14 | CDATA | I | Control Data |

| No. | Pin Name | I/O | Function |
|-----------------------|-------------------------|-----|---|
| Miscellaneous : 11pin | | | |
| 1 | $\overline{\text{RST}}$ | I | Reset Pin |
| 11 | BUSY | O | Status Output |
| 29 | VRAD | O | ADC Voltage Reference Pin Connected to AGND with 0.1uF and 4.7uF capacitors. |
| 25 | VRDA1 | O | CODEC-DAC Voltage Reference Pin Connected to AGND with 0.1uF and 4.7uF capacitors. |
| 22 | VRDA2 | O | Extra-DAC Voltage Reference Pin Connected to AGND with 0.1uF and 4.7uF capacitors. |
| 21 | VCOM | O | Voltage Common Output Pin Connected to AGND with 0.1uF and 4.7uF capacitors. |
| 43 | MAMP | O | MIC Amp Output Pin Connected to MONO3 with 1uF capacitor. |
| 42 | MONO3 | I | MONO #3 Input Pin |
| 32 | AINFL | O | Lch Antialias Filter Pin Connected to AGND with 1.0nF capacitor. |
| 31 | AINFR | O | Rch Antialias Filter Pin Connected to AGND with 1.0nF capacitor. |
| 20 | LOOPF | O | Loop Filter Pin Connected to AGND with 0.1uF capacitor. |
| Power Supplies : 5pin | | | |
| 18 | VA | - | Analog Power Supply Pin, 5V |
| 19 | AGND | - | Analog Ground Pin |
| 16 | VD | - | Digital Power Supply Pin, 5V |
| 17 | VT | - | Output Buffer Power Supply Pin, 3.3V |
| 15 | DGND | - | Digital Ground Pin |

Note:

No load current may be taken from the VCOM, VRAD, VRDA1, VRDA2 pins for the external circuits.
All digital input pins except pull-down pins should not be left floating.

| |
|---------------------------------|
| ABSOLUTE MAXIMUM RATINGS |
|---------------------------------|

(AGND,DGND=0V; Note 1)

| Parameter | Symbol | min | max | Units |
|--|--------|------|------------|-------|
| Power Supplies: Analog | VA | -0.3 | 6.0 | V |
| Digital (Note 2) | VD | -0.3 | 6.0/VA+0.3 | V |
| Output Buffer | VT | -0.3 | VD | V |
| Input Current, Any Pin Except Supplies | IIN | - | ± 10 | mA |
| Analog Input Voltage (Note 2) | VINA | -0.3 | 6.0/VA+0.3 | V |
| Digital Input Voltage (Note 2) | VIND | -0.3 | 6.0/VA+0.3 | V |
| Ambient Temperature (power applied) | Ta | -10 | 70 | |
| Storage Temperature | Tstg | -65 | 150 | |

Note: 1. All voltages with respect to ground.

2. Max value is higher voltage of 6.0V or VA+0.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

| |
|---|
| RECOMMENDED OPERATING CONDITIONS |
|---|

(AGND,DGND=0V; Note 1)

| Parameter | Symbol | min | typ | max | Units |
|------------------------|--------|-----|-----|-----|-------|
| Power Supplies: Analog | VA | 4.5 | 5.0 | 5.5 | V |
| Digital | VD | 4.5 | 5.0 | VA | V |
| Output Buffer | VT | 3.0 | 3.3 | VD | V |

Note: 1. All voltages with respect to ground.

| |
|-------------------------------|
| ANALOG CHARACTERISTICS |
|-------------------------------|

(Ta=25 ; VA,VD=5.0V; VT=3.3V; fs=44.1kHz; Signal Frequency=1kHz;

CSEL2,1="1,1", MCLK=256fs, BCLK=64fs, LRCK=fs

The same clocks are supplied to CODEC-ADC, CODEC-DAC & Extra-DAC.

Measurement frequency=10Hz ~ 20kHz; unless otherwise specified)

| Parameter | min | typ | max | Units |
|--|------|------|------|-------|
| CODEC-ADC: Measured via AINL/AINR | | | | |
| Resolution | | | 16 | Bits |
| S/(N+D) (-0.5dB Input) | 74 | 82 | | dB |
| S/N (A-Weighted) | 83 | 88 | | dB |
| Dynamic Range (-60dB Input, A-Weighted) | 83 | 88 | | dB |
| Interchannel Isolation (Note 3) | 70 | 78 | | dB |
| Interchannel Gain Mismatch | | 0.1 | 0.3 | dB |
| Gain Drift | | 100 | | ppm/ |
| Offset Error (Note 4) | | ± 1 | - | LSB |
| Input Voltage | 2.60 | 2.88 | 3.16 | Vpp |
| Input Resistance | 45 | 75 | 105 | k |
| Power Supply Rejection | | 50 | | dB |
| CODEC-DAC: Measured via AOUTL/AOUTR | | | | |
| Resolution | | | 16 | Bits |
| S/(N+D) | 74 | 83 | | dB |
| S/N (A-Weighted) | 83 | 88 | | dB |
| Dynamic Range (-60dB Input, A-Weighted) | 83 | 88 | | dB |
| Interchannel Isolation (Note 3) | 80 | 90 | | dB |
| Interchannel Gain Mismatch | | 0.1 | 0.5 | dB |
| Gain Drift | | 100 | | ppm/ |
| Output Voltage | 2.60 | 2.88 | 3.16 | Vpp |
| Load Resistance | 10 | | | k |
| Out-of-Band Noise (BW 100kHz) | | -83 | | dB |
| Power Supply Rejection | | 50 | | dB |
| Extra-DAC: Reference data | | | | |
| Resolution | | | 18 | Bits |
| S/(N+D) | | 83 | | dB |
| S/N (A-Weighted) | | 88 | | dB |
| Dynamic Range (-60dB Input, A-Weighted) | | 88 | | dB |
| Interchannel Isolation (Note 3) | | 90 | | dB |
| Interchannel Gain Mismatch | | 0.1 | | dB |
| Gain Drift | | 100 | | ppm/ |
| Output Voltage | | 2.88 | | Vpp |
| Power Supply Rejection | | 50 | | dB |

Note: 3. Crosstalk between channels on the same A/D or D/A.

4. Internal HPF removes offset.

| Parameter | min | typ | max | Units |
|--|-----|-----|-----|-------|
| Mic Amp | | | | |
| Gain | 28 | 30 | 32 | dB |
| Input Resistance | 30 | 50 | 80 | k |
| Mixer Input | | | | |
| Input Resistance (CD,Line,AUX) | 30 | 50 | 80 | k |
| Input Resistance (MONO1,MONO2,MONO3) | 10 | - | 80 | k |
| Mixer Gain Control: 32 steps | | | | |
| Step Size | 0 | 2 | | dB |
| Gain Control Range | -50 | | 12 | dB |
| Line Output: LOUT/ROUT/MOUT | | | | |
| Load Resistance | 5 | | | k |
| Master Volume: 32 steps | | | | |
| Step Size | 0 | 2 | | dB |
| Attenuation Control Range | -62 | | 0 | dB |
| Mono Volume: 8 steps | | | | |
| Step Size | 0 | 4 | | dB |
| Attenuation Control Range | -28 | | 0 | dB |
| Power Supplies | | | | |
| Power Supply Current | | | | |
| Normal Operation ($\overline{\text{PD}}$ bit="1") | | | | |
| VA | | 50 | 75 | mA |
| VD+VT | | 13 | 20 | mA |
| Power-Down-Mode ($\overline{\text{PD}}$ bit="0") | | | | |
| VA | | 10 | | uA |
| VD+VT | | 10 | | uA |
| Power Dissipation | | | | |
| Normal Operation | | | | |
| | | 315 | 475 | mW |
| Power-Down-Mode | | | | |
| | | 100 | | uW |

| |
|-------------------------------|
| FILTER CHARACTERISTICS |
|-------------------------------|

(Ta=25 ; VA,VD=5.0V ± 10%; VT=3.0 ~ 5.5V; fs=44.1kHz)

| Parameter | Symbol | min | typ | max | Units |
|--|--------|------|-------|--------|-------|
| CODEC-ADC Digital Filter(Decimation LPF): | | | | | |
| Passband ± 0.1dB (Note 5) | PB | 0 | | 16.5 | kHz |
| -0.5dB | | 0 | | 19.0 | kHz |
| -1.2dB | | 0 | | 20.0 | kHz |
| -6.7dB | | 0 | | 22.05 | kHz |
| Stopband | SB | 26.0 | | | kHz |
| Passband Ripple | PR | | | ± 0.1 | dB |
| Stopband Attenuation | SA | 68 | | | dB |
| Group Delay Distortion | GD | | | 0 | us |
| Group Delay (Note 6) | GD | | 16.1 | | 1/fs |
| CODEC-ADC Digital Filter(HPF): | | | | | |
| Frequency Response -3dB (Note 5) | FR | | 6.85 | | Hz |
| -0.5dB | | | 19.6 | | Hz |
| -0.1dB | | | 44.9 | | Hz |
| CODEC-DAC Digital Filter: | | | | | |
| Passband ± 0.1dB (Note 5) | PB | 0 | | 18.0 | kHz |
| -6.0dB | | 0 | | 22.05 | kHz |
| Stopband | SB | 26.1 | | | kHz |
| Passband Ripple | PR | | | ± 0.1 | dB |
| Stopband Attenuation | SA | 65 | | | dB |
| Group Delay (Note 6) | GD | | 14.4 | | 1/fs |
| CODEC-DAC Digital Filter+Analog Filter: | | | | | |
| Frequency Response 0 ~ 20.0kHz | FR | | ± 1.0 | | dB |
| Extra-DAC Digital Filter: | | | | | |
| Passband ± 0.1dB (Note 5) | PB | 0 | | 18.0 | kHz |
| -6.0dB | | 0 | | 22.05 | kHz |
| Stopband | SB | 26.0 | | | kHz |
| Passband Ripple | PR | | | ± 0.02 | dB |
| Stopband Attenuation | SA | 57 | | | dB |
| Group Delay (Note 6) | GD | | 14.4 | | 1/fs |
| Extra-DAC Digital Filter+Analog Filter: | | | | | |
| Frequency Response 0 ~ 20.0kHz | FR | | ± 1.0 | | dB |

Notes: 5. The Passband and stopband frequencies scale with fs.

6. The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 16bit data of both channels to the output register for ADC.

For DAC, this time is from setting the 16/18bit data of both channels on input register to the output of analog signal.

| |
|--------------------------------|
| DIGITAL CHARACTERISTICS |
|--------------------------------|

(Ta=25 ; VA,VD=5.0V ± 10%; VT=3.0 ~ 5.5V)

| Parameter | Symbol | min | typ | max | Units |
|--|--------|--------|-----|------|-------|
| High-Level Input Voltage | VIH | 2.0 | - | - | V |
| Low-Level Input Voltage | VIL | - | - | 0.8 | V |
| High-Level Output Voltage (Iout=-80uA) | VOH | VT-0.4 | - | - | V |
| Low-Level Output Voltage (Iout=80uA) | VOL | - | - | 0.4 | V |
| Input Leakage Current | Iin | - | - | ± 10 | uA |

| |
|----------------------------------|
| SWITCHING CHARACTERISTICS |
|----------------------------------|

(Ta=25 ; VA,VD=5.0V ± 10%; VT=3.0 ~ 5.5V; CL = 20pF)

| Parameter | Symbol | min | typ | max | Unit |
|----------------------------------|--------|-------|---------|--------|------|
| Master Clock Timing (Note 7) | fCLK | 1.024 | 11.2896 | 12.800 | MHz |
| Pulse Width Low | tCLKL | 31.25 | | | ns |
| Pulse Width High | tCLKH | 31.25 | | | ns |
| LRCK Frequency (Note 8) | fs | 4 | 44.1 | 50 | kHz |
| Duty Cycle | | 45 | | 55 | % |
| Serial Interface Timing (Note 9) | | | | | |
| BCLK Period | tBCK | 312.5 | | | ns |
| BCLK Pulse Width Low | tBCKL | 100 | | | ns |
| Pulse Width High | tBCKH | 100 | | | ns |
| LRCK Edge to BCLK " " (Note 10) | tLRB | 50 | | | ns |
| BCLK " " to LRCK Edge (Note 10) | tBLR | 50 | | | ns |
| SDI Hold Time | tSDH | 50 | | | ns |
| SDI Setup Time | tSDS | 50 | | | ns |
| LRCK to SDO(MSB) | tLRS | | | 70 | ns |
| BCLK " " to SDO | tBSD | | | 70 | ns |
| Control Interface Timing | | | | | |
| CCLK Period | tCCK | 200 | | | ns |
| CCLK Pulse Width Low | tCCKL | 80 | | | ns |
| Pulse Width High | tCCKH | 80 | | | ns |
| CDATA Hold Time | tCDS | 50 | | | ns |
| CDATA Setup Time | tCDH | 50 | | | ns |
| CS High Level Time | tCSW | 150 | | | ns |
| CS " " to CCLK " " | tCSS | 50 | | | ns |
| CCLK " " to CS " " | tCSH | 50 | | | ns |
| Reset Timing | | | | | |
| RST Pulse Width | tRTW | 150 | | | ns |
| RST " " to SDO delay (Note 11) | tRSD | | 516 | | 1/fs |

Notes: 7. Master clock means MCLK1 and MCLK2.

8. LRCK means LRCK1 and LRCK2.

If the duty of LRCK changes larger than 5% from 50%, the AK4531A is reset by the internal phase detecting circuit automatically. Extra-DAC should operate at fs 16kHz for practical use.

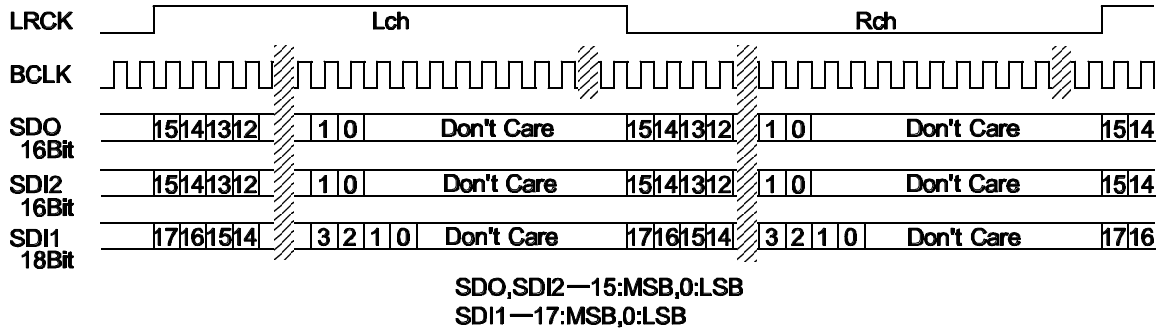
9. Timing relation is specified between LRCK1 and BCLK1, or LRCK2 and BCLK2.

10. BCLK rising edge must not occur at the same time as LRCK edge.

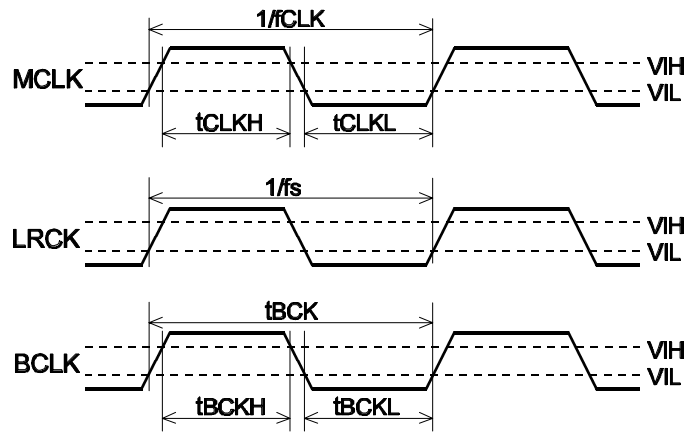
11. These cycles are the number of LRCK rising from RST rising.

Audio Data Formats

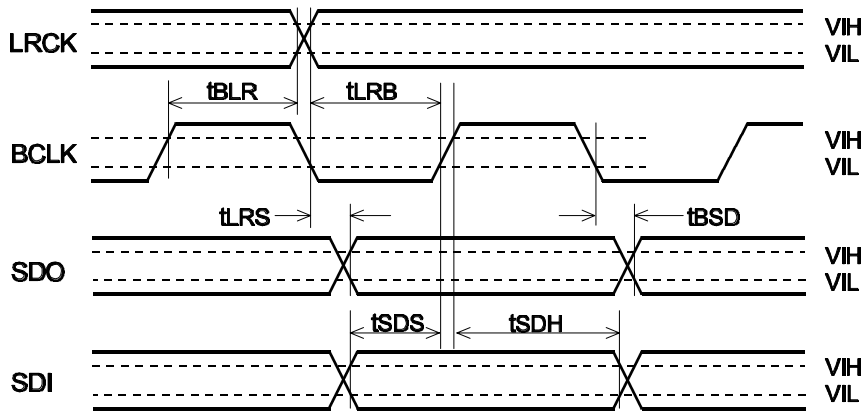
The data format of CODEC-ADC/DAC is MSB first & MSB justified with 16bit. The BCLK needs 32fs or more than 32fs cycles. The data format of Extra-DAC is MSB first & MSB justified with 18bit. In this case, BCLK needs 36fs or more than 36fs cycles.



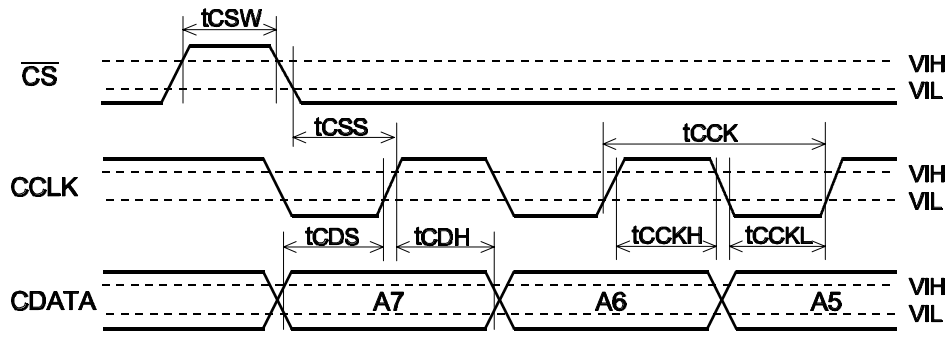
Timing Diagram



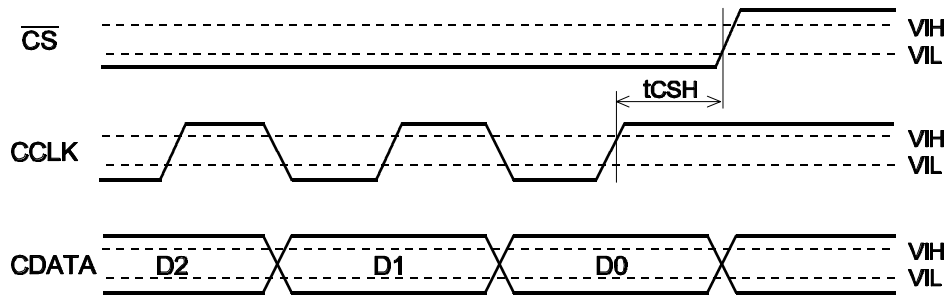
Clock Timing



Serial Audio Interface Timing



Control Data Interface Timing 1



Control Data Interface Timing 2



Reset Timing

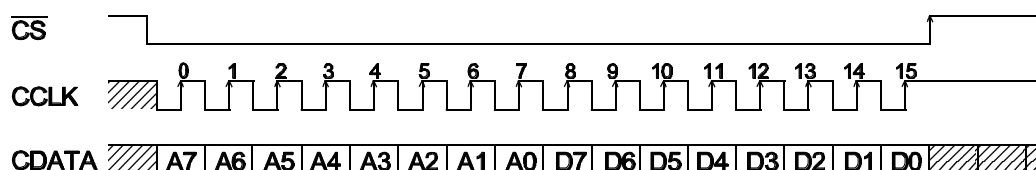
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|---------------------------|
| OPERATION OVERVIEW |
|---------------------------|

1. Control Register Map

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------------|------|--------|--------|-------|--------|--------|-------|-------|
| 00 | Master Volume Lch | MUTE | | | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 01 | Master Volume Rch | MUTE | | | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 02 | Voice Volume Lch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 03 | Voice Volume Rch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 04 | FM Volume Lch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 05 | FM Volume Rch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 06 | CD Audio Volume Lch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 07 | CD Audio Volume Rch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 08 | Line Volume Lch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 09 | Line Volume Rch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 0A | AUX Volume Lch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 0B | AUX Volume Rch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 0C | Mono1 volume | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 0D | Mono2 volume | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 0E | MIC volume | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 0F | Mono-out Volume | MUTE | | | | | ATT2 | ATT1 | ATT0 |
| 10 | Output Mixer SW 1 | | FML | FMR | LineL | LineR | CDL | CDR | MIC |
| 11 | Output Mixer SW 2 | | | AUXL | AUXR | VoiceL | VoiceR | Mono2 | Mono1 |
| 12 | Lch Input Mixer SW 1 | | FML | FMR | LineL | LineR | CDL | CDR | MIC |
| 13 | Rch Input Mixer SW 1 | | FML | FMR | LineL | LineR | CDL | CDR | MIC |
| 14 | Lch Input Mixer SW 2 | TMIC | TMono1 | TMono2 | AUXL | AUXR | VoiceL | Mono2 | Mono1 |
| 15 | Rch Input Mixer SW 2 | TMIC | TMono1 | TMono2 | AUXL | AUXR | VoiceR | Mono2 | Mono1 |
| 16 | Reset & Power Down | | | | | | | PD | RST |
| 17 | Clock Select | | | | | | | CSEL2 | CSEL1 |
| 18 | AD Input Select | | | | | | | | ADSEL |
| 19 | MIC Amp Gain | | | | | | | | MGAIN |

Notes. ATT* is data bits for the attenuation level.

GAI* is data bits for the gain level.

2. WRITE Timing of Control Register

A7-A0: Address

D7-D0: Control Data

3. Control Register Definitions

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------------|------|----|----|------|------|------|------|------|
| 00 | Master Volume Lch | MUTE | | | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |
| 01 | Master Volume Rch | MUTE | | | ATT4 | ATT3 | ATT2 | ATT1 | ATT0 |

MUTE 1:Mute.

ATT4:0 32 levels with 2dB step
 00000: 0dB
 11111: -62dB

Initial "1000 0000" (Mute & 0dB).

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------------|------|----|----|------|------|------|------|------|
| 02 | Voice Volume Lch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 03 | Voice Volume Rch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 04 | FM Volume Lch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 05 | FM Volume Rch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 06 | CD Audio Volume Lch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 07 | CD Audio Volume Rch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 08 | Line Volume Lch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 09 | Line Volume Rch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 0A | AUX Volume Lch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 0B | AUX Volume Rch | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 0C | Mono1 volume | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 0D | Mono2 volume | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |
| 0E | MIC volume | MUTE | | | GAI4 | GAI3 | GAI2 | GAI1 | GAI0 |

MUTE 1: Mute.

GAI4:0 32 levels with 2dB step
 00000: +12dB
 00110: 0dB
 11111: -50dB

Initial "1000 0110" (Mute & 0dB).

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------|------|----|----|----|----|------|------|------|
| 0F | Mono-out Volume | MUTE | | | | | ATT2 | ATT1 | ATT0 |

MUTE 1:Mute.

ATT2:0 8 levels with 4dB step
 000: 0dB
 111: -28dB

Initial "1000 0000" (Mute & 0dB).

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------------|------|--------|--------|-------|--------|--------|-------|-------|
| 10 | Output Mixer SW 1 | | FML | FMR | LineL | LineR | CDL | CDR | MIC |
| 11 | Output Mixer SW 2 | | | AUXL | AUXR | VoiceL | VoiceR | Mono2 | Mono1 |
| 12 | Lch Input Mixer SW 1 | | FML | FMR | LineL | LineR | CDL | CDR | MIC |
| 13 | Rch Input Mixer SW 1 | | FML | FMR | LineL | LineR | CDL | CDR | MIC |
| 14 | Lch Input Mixer SW 2 | TMIC | TMono1 | TMono2 | AUXL | AUXR | VoiceL | Mono2 | Mono1 |
| 15 | Rch Input Mixer SW 2 | TMIC | TMono1 | TMono2 | AUXL | AUXR | VoiceR | Mono2 | Mono1 |

ON/OFF of Mixer Switches

- 0: OFF
- 1: ON

Initial "0000 0000" (All OFF).

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------|----|----|----|----|----|----|-----------------|------------------|
| 16 | Reset & Power Down | | | | | | | \overline{PD} | \overline{RST} |
| 17 | Clock Select | | | | | | | CSEL2 | CSEL1 |
| 18 | AD Input Select | | | | | | | | ADSEL |
| 19 | MIC Amp Gain | | | | | | | | MGAIN |

\overline{RST} initializes the contents of all registers. When \overline{RST} pin goes "L", this register becomes "1".
 1: Normal Operation
 0: Initialize

\overline{PD} Enables the power down. When \overline{RST} pin goes "L", this register becomes "1".
 1: Normal Operation
 0: Power down

CSEL2,1 Selects the clocks for codec in two systems (-MCLK1,LRCK1,BCLK1; -MCLK2,LRCK2,BCLK2). The clocks for Extra-DAC always connect to system . The following is the clock select table. Please refer to the block diagram about each signal name. The initial state is "1,1".

| Clock Select | | CODEC-ADC | | | CODEC-DAC | | |
|--------------|-------|-----------|-------|-------|-----------|-------|-------|
| CSEL2 | CSEL1 | CLK3 | LR3 | BCK3 | CLK2 | LR2 | BCK2 |
| 0 | 0 | PLL | LRCK2 | BCLK2 | PLL | LRCK2 | BCLK2 |
| 0 | 1 | MCLK1 | LRCK1 | BCLK1 | PLL | LRCK2 | BCLK2 |
| 1 | 0 | MCLK2 | LRCK2 | BCLK2 | MCLK2 | LRCK2 | BCLK2 |
| 1 | 1 | MCLK1 | LRCK1 | BCLK1 | MCLK1 | LRCK1 | BCLK1 |

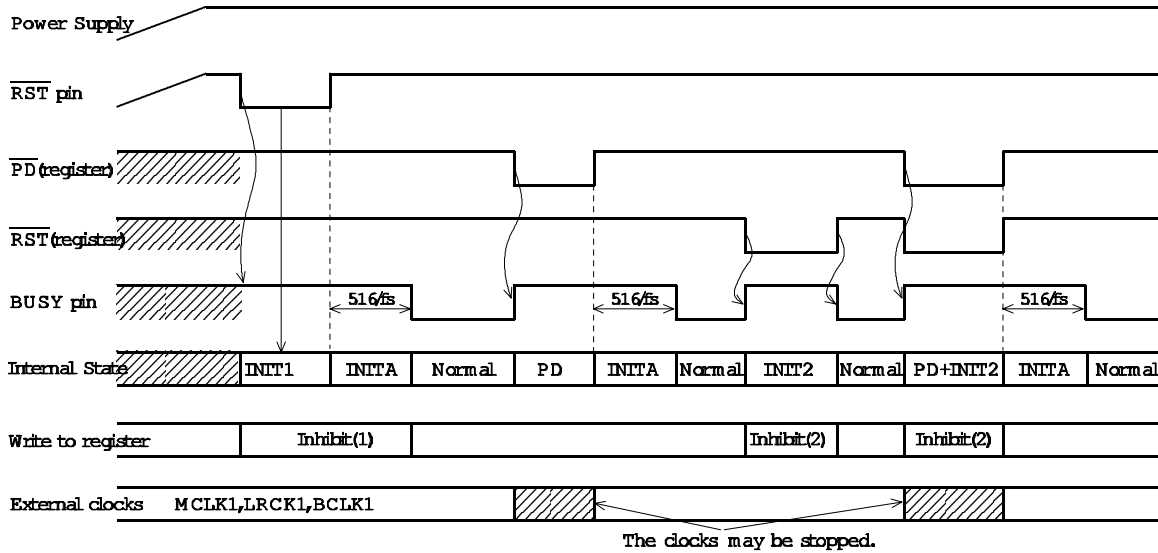
* In the PLL mode, the master clock(256fs) is supplied by the PLL circuit based on LRCK2.

ADSEL Selects the input source to ADC. The initial state is "0".
 0: output from Input Mixer
 1: AINL/AINR inputs

MGAIN Selects the gain of MIC amp. The initial state is "0".
 0: 0dB
 1: 30dB

4. Explanation of each sequence

4.1. Reset & Power down



- INIT1: Initializing all registers.
- INIT2: Initializing all registers except for \overline{PD} , \overline{RST} registers.
- INITA: Initializing the analog section. Initializing period is 516/fs.
- PD: Power down state. All analog outputs are floating. The contents of all registers are hold.
- Inhibit(1): Inhibits writing to all registers.
- Inhibit(2): Inhibits writing to all registers except for \overline{PD} , \overline{RST} registers.
- The AK4531A operates by the external clocks(MCLK1,LRCK1,BCLK1) during initializing the analog section.

Figure 1. Reset & Power Down Sequence

4.2. \overline{RST} pin operation

"H": Normal operation

"L": Initializing mode 1 (INIT1 in Figure 1)

- Initializing all registers.
- Inhibits writing to all registers.
- BUSY output goes "H".
- The initialization of the analog section starts from "L" of \overline{RST} pin.
- SDO pin stays "L" and BUSY pin holds "H" during the initializing period of 516/fs.

4.3. \overline{RST} register operation

"1": Normal Operation

"0": Initializing mode 2 (INIT2 in Figure 1)

- Initializing all registers except for \overline{PD} , \overline{RST} registers.
- Inhibits writing to all registers except for \overline{PD} , \overline{RST} registers.
- BUSY output goes "H".
- \overline{RST} register goes "1" when \overline{RST} pin goes "L".
- The analog section is not initialized.

4.4. $\overline{\text{PD}}$ register operation

"1": Normal Operation

"0": Power down

- The contents of all registers are hold.
- $\overline{\text{BUSY}}$ output goes "H".
- $\overline{\text{PD}}$ register goes "1" when $\overline{\text{RST}}$ pin goes "L".
- All analog outputs($\overline{\text{LOUT}}$, $\overline{\text{ROUT}}$, $\overline{\text{MOUT}}$, $\overline{\text{AOUTL}}$, $\overline{\text{AOUTR}}$, $\overline{\text{MAMP}}$) go floating.
- The initialization of the analog section starts when $\overline{\text{PD}}$ register returns to "1".
- $\overline{\text{SDO}}$ pin stays "L" and $\overline{\text{BUSY}}$ pin holds "H" during the initializing period of 516/fs.

4.5. $\overline{\text{BUSY}}$ output pin operation

$\overline{\text{BUSY}}$ output goes "H" in the following cases.

- $\overline{\text{RST}}$ pin="L"
- During initializing the analog section.
- $\overline{\text{RST}}$ register="0"
- $\overline{\text{PD}}$ register="0"
- During PLL unlock. But this is valid only when PLL clock is selected by CSEL registers. i.e. CSEL2,1=(0,0) or (0,1).

4.6. $\overline{\text{SDO}}$ output pin operation

$\overline{\text{SDO}}$ output is the 16bit data of ADC and goes "L"(0000H) in the following cases.

- $\overline{\text{RST}}$ pin="L"
- During initializing the analog section.
- $\overline{\text{RST}}$ register="0"
- $\overline{\text{PD}}$ register="0"
- During PLL unlock. But this is valid only when PLL clock is selected as ADC clock by CSEL registers. i.e. CSEL2,1=(0,0).

4.7. CODEC-DAC analog output pins($\overline{\text{AOUTL}}$, $\overline{\text{AOUTR}}$) operation

These outputs are muted internally and VCOM voltage is output in the following cases.

- $\overline{\text{RST}}$ pin="L"
- During initializing the analog section.
- $\overline{\text{RST}}$ register="0"
- During PLL unlock. But this is valid only when PLL clock is selected as ADC clock by CSEL registers. i.e. CSEL2,1=(0,0) or (0,1).

These outputs are floating in the following case.

- $\overline{\text{PD}}$ register="0"

4.8. Extra-DAC analog outputs operation

It is impossible to observe externally due to the internal signal.

These outputs are muted internally and VCOM voltage is output in the following cases.

- $\overline{\text{RST}}$ pin="L"
- During initializing the analog section.
- $\overline{\text{RST}}$ register="0"

These outputs are floating in the following case.

- $\overline{\text{PD}}$ register="0"

5. System clock

The external clocks which are required to operate the AK4531A are MCLK, LRCK, BCLK except for PLL mode. MCLK should be synchronized with LRCK but the phase is free of care. As the AK4531A includes the phase detect circuit for LRCK, the AK4531A is reset automatically when the synchronization is out of phase by changing the clock frequencies. Therefore, the reset is not required except only upon power-up.

All external clocks should always be present whenever the AK4531A is in normal operation mode. If these clocks are not provided, the AK4531A may draw excess current and do not possibly operate properly because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4531A should be in the power-down mode.

6. PLL lock speed

The AK4531A has a PLL to generate the CODEC master clock. The lock in time from 4kHz to 50kHz is about 100ms.

7. Digital High Pass Filter

The ADC of the AK4531A has a digital high pass filter for DC offset cancel. The cut-off frequency of the HPF is 6.85Hz at $f_s=44.1\text{kHz}$ and the frequency response at 20Hz is -0.5dB. It also scales with sampling rate(fs).

SYSTEM DESIGN

Figure 2,3 show the system connection diagram. An evaluation board is available which demonstrates the optimum layout, power supply arrangements and measurement results.

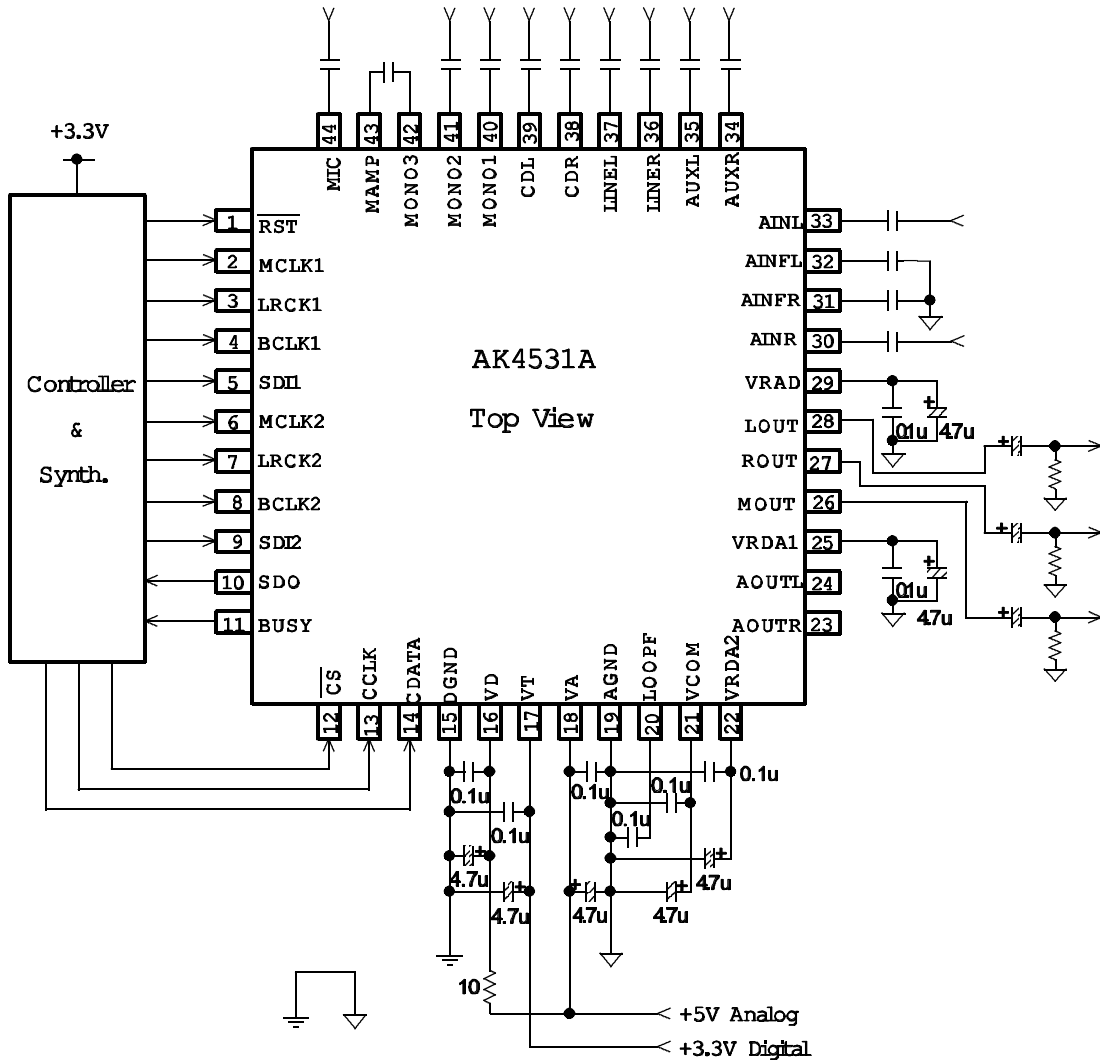


Figure 2. Typical Connection Diagram(VT=3.3V)

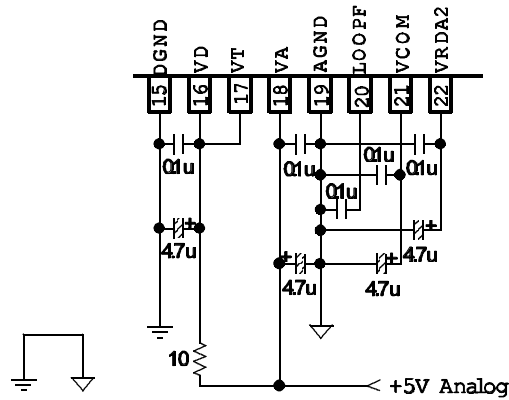


Figure 3. Typical Connection Diagram (VT=5V)

1. Grounding and Power Supply Decoupling

The AK4531A requires careful attention to power supply and grounding arrangements. VD should be supplied from analog power supply. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4531A as possible, with the small value ceramic capacitor being the nearest.

2. On-chip voltage reference

The on-chip voltage references are output on the VRAD,VRDA1,VRDA2 and VCOM pins for decoupling. The VRAD,VRDA1,VRDA2 pins are used as the reference of A/D and D/A conversion. The VCOM is a signal ground of this chip. An electrolytic capacitor less than 10uF in parallel with a 0.1uF ceramic capacitor attached to these pins eliminates the effects of high frequency noise. Especially, the small value ceramic capacitors should be as near to the AK4531A as possible. No load current may be drawn from the VRAD,VRDA1,VRDA2 and VCOM pins. All signals, especially clocks, should be kept away from the VRAD,VRDA1,VRDA2 and VCOM pins in order to avoid unwanted coupling into the modulators.

3. Analog Inputs

The mixer inputs and the ADC input are single-ended and internally biased to the VCOM voltage with 50k (typ) resistance. The input signal range is typically 2.88Vpp(1Vrms). Figure 4 is an example for 2Vrms line-level input circuit. The ADC output data format is 2's complement. The AK4531A accepts input voltages from AGND to VA. The output code is 7FFFH for input above a positive full scale and 8000H for input below a negative full scale. The ideal code is 0000H with no input signal. The DC offset is cancelled by the internal HPF.

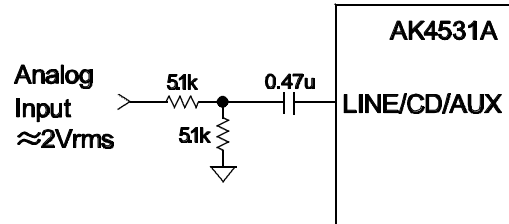


Figure 4. 2Vrms Line level Input

The AK4531A samples the analog inputs at 64fs. The digital filter rejects all noise higher than the stop band. However, the filter will not reject frequencies right around 64fs(and multiples of 64fs). Most audio signals do not have significant energy at 64fs.

4. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The output signal range is typically 2.80Vpp(1Vrms). The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFH and a negative full scale for 8000H in the case of CODEC-DAC. The ideal output is VCOM voltage for 0000H. The internal switched-capacitor filter and continuous-time filter almost remove the noise generated by the delta-sigma modulator of DAC beyond the audio passband, especially low sampling rate. In case of CODEC-DAC, the noise floor level is almost constant and the audible noise level is -83dB(typ) at 8kHz sampling. However, Extra-DAC should be operated at $f_s = 16\text{kHz}$.

5. Other information

5.1. Clock change

The clock change should be done after muting the DAC output by the master volume to avoid the click noise by out-of-synchronization.

5.2. Offset on mixer inputs

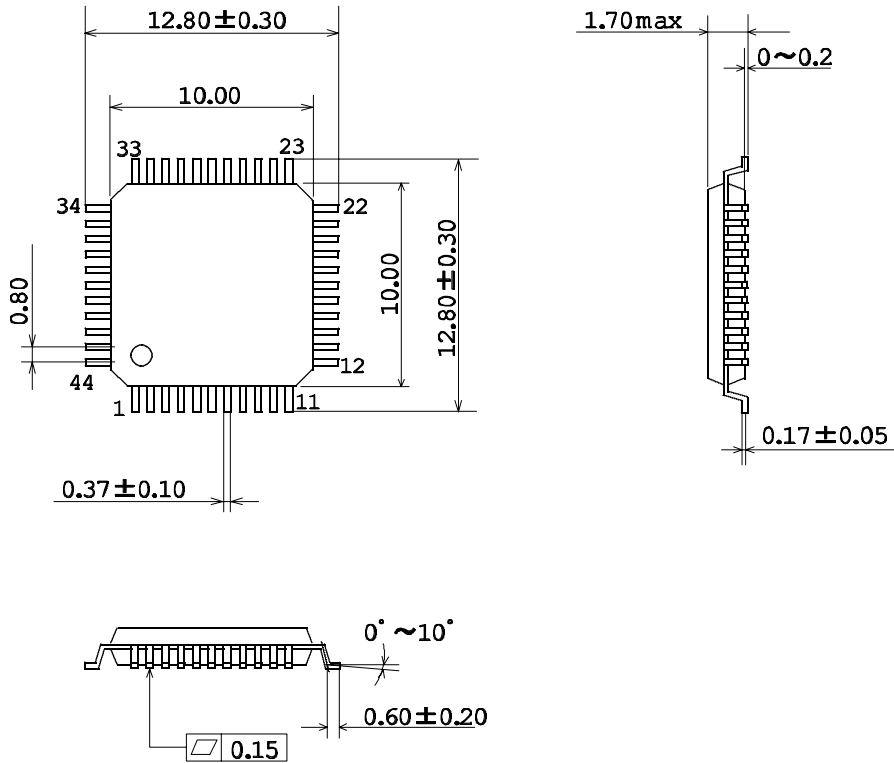
When the mixer gain is set to +12dB, the output has pretty large offset even if the inputs are no signal. Therefore, large click noise may occur when the gain level is changed quickly.

5.3. Click noise on the analog outputs.

The click noise of about -50dB occurs from the analog outputs(LOUT,ROUT,MOU,AOUT) at the power on/off or the transition of $\overline{\text{PD}}$ register. The analog outputs should be muted externally if the click noise influences system application.

PACKAGE

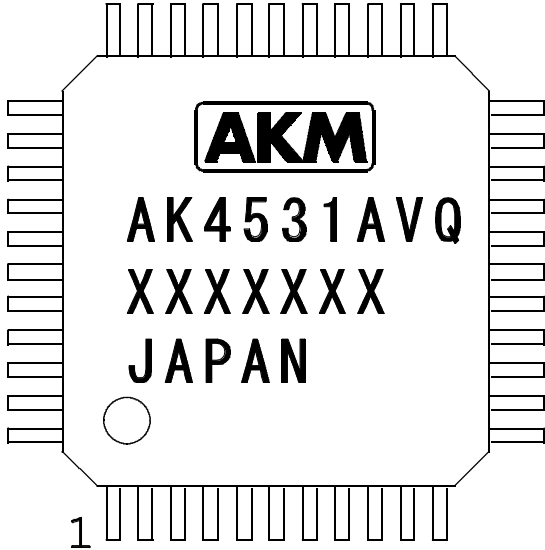
44pin LQFP (Unit: mm)



Package & Lead frame material

| | |
|-------------------------------|--------------|
| Package molding compound : | Epoxy |
| Lead frame material : | Cu |
| Lead frame surface treatment: | Solder plate |

MARKING



- 1) Pin #1 indication
- 2) Date Code : XXXXXXXX(7 digits)
- 3) Marketing Code : AK4531A-VQ
- 4) Country of Origin
- 5) Asahi Kasei Logo