Data Sheet
June 1995

AT&T Microelectronics

ATT20C408: 16-Bit Interface RAMDAC Dual Clock Synthesizers *PrecisionDAC*™ Technology

Features

- 170/135 MHz speed grades
  - — 170 MHz 2:1 multiplex 8-bit pseudocolor
  - — 73 MHz true-color operation
- 16-bit pixel port, usable as 8-bit port
  - — Compatible with 490 using P[7:0]
  - — Compatible with 498 using P[15:0]
- Nine software-selectable color modes
  - — 24-bit packed pixels
  - — 24-bit, 1[illegible]rue color
  - — 8-bit pse[illegible]r
- *PrecisionDAC* technology and on-chip voltage reference provide typical DAC output current accuracy of ±3%
- Dual programmable clock synthesizers
  - — Pixel clock and memory clock
  - — Reset to 28.322 MHz and 25.175 MHz VGA frequency
  - — Strobe input latches frequency select lines
- On-chip PLL clock doubler
  - — 85 MHz inp[illegible]Hz pixel output
- 2:1 and 1:1 pixel multiplexing
- Power dissipation 1.2 W typ. at 135 MHz
- 256 x 24 color RAM
- Software compatible to ATT21C498/21C499
- 68-pin PLCC package

Applications

- Screen resolutions (noninterlaced)
  - — 1600 x 1280, 8 bits per pixel, 60 Hz
  - — 1280 x 1024, 16 bits per pixel, 60 Hz
  - — 1024 x 768, 16 bits per pixel, 85 Hz
  - — 1024 x 768, 24 bits per pixel, packed, 70 Hz
  - — 800 x 600, 24 bits per pixel, unpacked, 72 Hz
- True-color desktop, PC add-in card
- *X-Windows** terminals
- Green PCs

Description

The ATT20C408 CMOS RAMDAC provides the same functionality as that of the ATT20C409, in a new pinout configuration. This device supports 8-bit multiplexed operation that can be input on 16 pixel pins. The ATT20C408 retains register compatibility with the ATT21C498, ATT20C409, and ATT21C499 parts.

The ATT20C408 features 24-bit packed pixel modes that provide 24-bit graphics in a 3 Mbyte frame buffer at 1024 x 768 screen resolution. Dual clock synthesizers offer two programmable and two fixed frequencies in PLL (A) and one programmable and three fixed frequencies in PLL (B). After reset, the frequencies are as follows:

PLL (A): 25.175 MHz, 28.322 MHz, 50 MHz, and 75 MHz

PLL (B): 30 MHz, 40 MHz, 50 MHz, and 60 MHz

Easy identification of the RAMDAC allows the video BIOS to determine if a requested mode is available on the hardware being used.

Each device's voltage reference is link-trimmed for typical DAC output current accuracies of ±3% with AT&T's *PrecisionDAC* technology. The device is offered in a 68-pin PLCC package. It is meant to work with an internal voltage reference.

* *X-Windows* is a registered trademark of Massachusetts Institute of Technology.

Table of Contents

Overview and Introduction

The ATT20C408 RAMDAC is compatible with the architecture of the ATT20C409, ATT21C499, and ATT21C498 RAMDACs. The ATT20C408 contains 24-bit packed pixels on a 16-pin interface. The device includes dual clock synthesizers that will synthesize a pixel clock and a memory clock from a reference frequency. The part includes a third analog PLL for pixel clock multiplication. The multiplication of 2x or 2/3x the pixel clock is set automatically when certain color modes are programmed. Clock synthesis and clock multiplication reduce the maximum clock speed on the board. The reduced clock speeds ease high-speed board design and FCC certification. See Table 1 for feature comparison and functional differences between the ATT20C408, ATT21C499, ATT21C498, and the ATT22C498 RAMDAC devices.

The ATT20C408 includes simple indexed addressing of all control, test, and identification registers using only two register select pins. This supplements multiple accesses of the pixel mask register used in this and other devices.

Connect a 14.318 MHz crystal across the XIN and XOUT pins when using the clock synthesizer (see Figure 1). Other input crystal frequencies can be used.

When using a reference frequency instead of a crystal, connect the signal to XIN and let XOUT float (leave disconnected).

Reset State

The purpose of this section is to describe how the RAMDAC is operating after the reset pin has been toggled low.

When $\overline{\text{RESET}}$ is asserted, OTCLKA outputs 25.175 MHz (VGA graphics frequency), 28.322 MHz (VGA text frequency), 50 MHz, or 75 MHz depending on the value of the frequency select pins or frequency select bits.

When $\overline{\text{RESET}}$ is asserted, OTCLKB delivers 30 MHz, 40 MHz, 50 MHz, or 60 MHz depending on the value of the frequency select pins or frequency select bits.

During normal operation, the clock synthesizer can be programmed to any frequency within the capability of the part. The clock synthesizers can be powered down. When powered down, the outputs are 3-stated.

Table 1. Feature Comparison of the ATT20C408, ATT21C499, ATT21C498, and ATT22C499

Feature	20C408	21C499	21C498	22C498
Pixel Interface	16 bits	24 bits	16 bits	16 bits
Packed 24-bit Pixels	Yes	Yes	Yes	Yes
Clock Synthesizers	Dual	Dual	None	None
Clock Multiply Factor	2, 0.67 PCLK (analog)	2, 0.67 PCLK (analog)	2x (digital)	2, 0.67 PCLK (analog)
Mux Rate for 8-bit Pixels	2:1	2:1	2:1	2:1
Color Modes	9	13	11	11
Software Compatible to 20C498	Yes	Yes	Yes	Yes
Control Registers	CR[1:0], CC0	CR[1:0], CC0	CR0	CR0
Clock Synth A, Reg. Set A, R/W Access: AA, AB AC, AD	— None Read/Write	— None Read/Write	— NA NA	— NA NA
Clock Synth B, Reg. Set B, R/W Access: BA, BB, BC BD	— None Read/Write	— None Read/Write	— NA NA	— NA NA
MSW Pin	None	Yes	Yes	Yes
Package	68 PLCC	68 PLCC	44 PLCC	44 PLCC
Manufacturer ID	MIR = $84	MIR = $84	MIR = $84	MIR = $84
Device ID	DIR = $09	DIR = $99	DIR = $98	DIR = $98
Revision ID	None	None	None	None
Maximum Speed (MHz)	170	170	170	170

Overview and Introduction (continued)

When $\overline{\text{RESET}}$ goes inactive, the RAMDAC loads each internal register with $00, unless otherwise noted.

The internal register can be written through the MPU port even though the RAMDAC is not being clocked. The internal RAM cannot be written unless the RAMDAC is clocked. The RAMDAC will reset as follows:

1. Crystal oscillator enabled.
2. 6-bit DACs (VGA, SVGA).
3. 8-bit pseudocolor mode.
4. Frequency select pins FS[1:0] determining the frequencies of both synthesizer A and synthesizer B.
5. Synthesizer A running at one of four preprogrammed frequencies (25.175 MHz, 28.322 MHz, 50 MHz, or 75 MHz), until register sets AC0—AC2 or AD0—AD2 are changed and selected.
6. Synthesizer B running at one of four preprogrammed frequencies (30 MHz, 40 MHz, 50 MHz, or 60 MHz), until register sets BC0—BC2 or BD0—BD2 are changed and selected.

Programming from Reset

The RAMDAC can be configured by programming the internal registers. To program all the internal registers, the device needs to have indexed addressing enabled. Indexed addressing is enabled by setting bit CR0[0] = 1. Bit CR0[0] is set to one using an addressing mode available through the read mask register (RMR).

Using the RMR to address internal registers allows backward compatibility with only four hardware-addressable registers. The following sequence of steps using DOS debug will allow the indexed addressing mode to be enabled. This can also be accomplished easily in a programming language such as C.

1. Read the current state of command register 0 (CR0) via the read mask register (RMR).
   -o 3C8 00 Write to port 3C8 (WMA) value $00.
   Reset back door state machine.
   -i 3C6 Read port 3C6 (RMR).
   Contents of the RMR.
   -i 3C6 Contents of the RMR.
   -i 3C6 Contents of the RMR.
   -i 3C6 Contents of the RMR.
   -i 3C6 Contents of the command register 0 (CR0).
2. Enable indexed programming by setting CR0[0] = 1.
   -o 3C8 00 Reset back door state machine.
   -i 3C6 Contents of the RMR.
   -i 3C6 Contents of the RMR.
   -i 3C6 Contents of the RMR.
   -i 3C6 Contents of the RMR.
   -o 3C6 xxxx xxx1 Set CR0[0] = 1.
3. Indexed programming is now enabled.
   3C8 is the address port.
   3C6 is the data port.
4. To exit indexed programming, set CR0[0] = 0.
   -o 3C8 01 Select CR0.
   -i 3C6 Read CR0.
   -o 3C6 XXXX XXX0 (binary).
   Reset bit 0; leave other bits programmed as they were.

Changing Clock Frequencies

The purpose of this section is to describe how to change the internal synthesizer frequencies without corrupting the on-chip pixel color RAM.

1. Power down the chip by setting CR0[3] = 1. The registers retain their values and can be read and written. The RAM cannot be read or written during this time.
2. Program a delay of approximately 300 µs. The delay will vary depending on the noise in the system and the signals connecting to the RAMDAC.
3. Change the synthesizer register settings and/or change the frequency select bits/lines.
4. Program another delay of approximately 300 µs. This will vary depending on the noise in the system and the signals connecting to the RAMDAC.
5. Power up the chip by setting CR0[3] = 0. The registers retain their values and can be read and written. The RAM can now be read or written.

The data (colors) integrity of the pixel color RAM should be intact. To add further protection to the values in the color RAM, copy the pixel color RAM to system memory before changing clock frequencies. Copy the values back after the frequency has settled.

Overview and Introduction (continued)

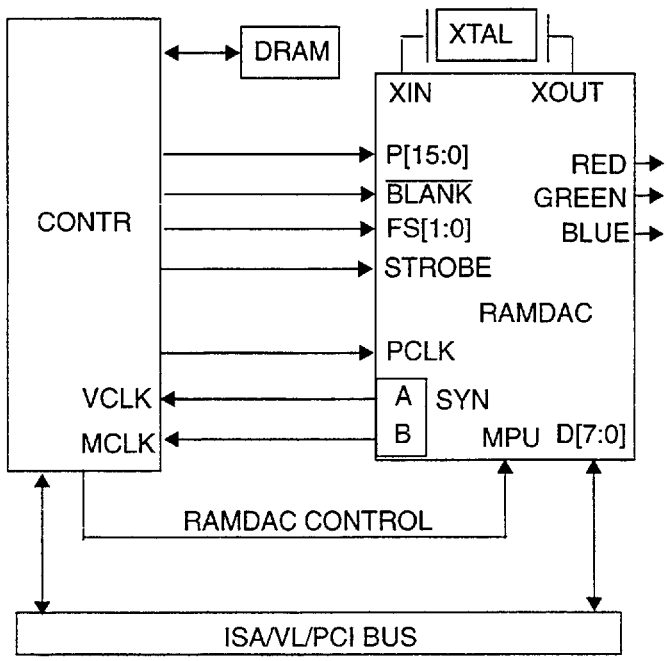


Figure 1. System Block Diagram

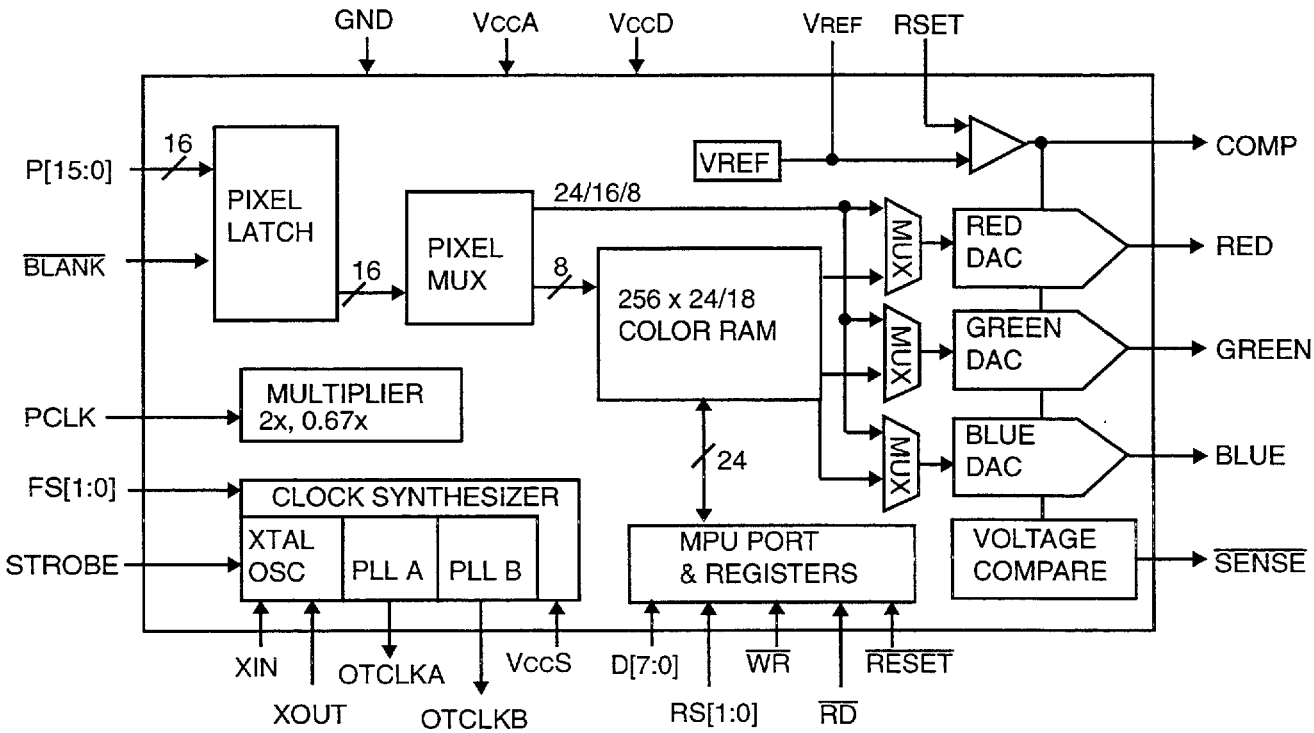


Figure 2. Block Diagram

Pin Information

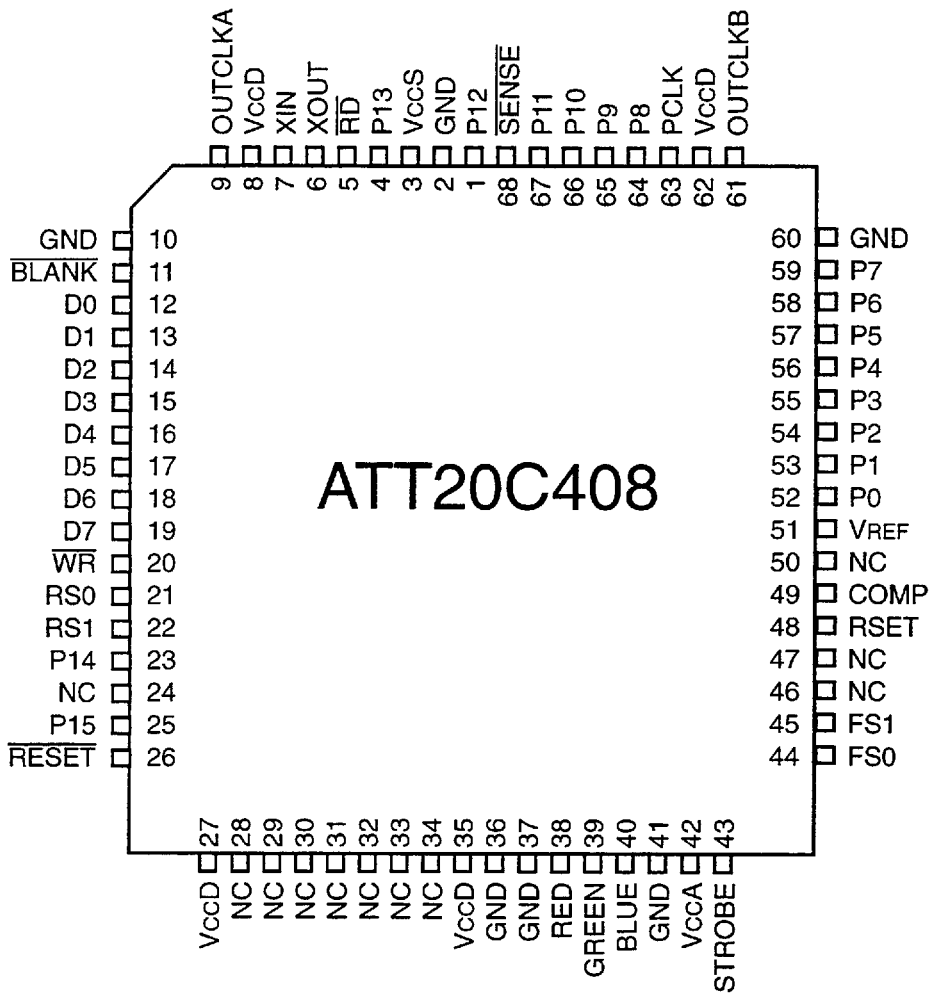


Figure 3. Pin Diagram

Pin Information (continued)

Table 2. Pin Descriptions

Pin #	Symbol	Type	Name/Function
Pixel and Control Pins			
1, 4, 23, 25, 59—52 67—64	P[12:13], P[14:15], P[7:0], P[11:8]	I	**Pixel Inputs.** TTL compatible. These pins are latched on the rising edge of PCLK. Pixels are presented to the DACs as color data in true-color modes and are used as addresses in pseudocolor mode to look up color data in the color RAM. Unused inputs should be connected to GND.
11	$\overline{\text{BLANK}}$	I	**BLANK (Active-Low).** TTL compatible. $\overline{\text{BLANK}}$ is latched on the rising edge of PCLK. When $\overline{\text{BLANK}}$ is low, the 1.44 mA current source on the analog outputs will be turned off. The DACs ignore digital input from memory. In mode 14, pixel data is aligned with the rising edge of PCLK after $\overline{\text{BLANK}}$ rises.
Clock Pins			
45, 44	FS[1:0]	I	**Frequency Select Lines.** TTL compatible. Clock frequency select lines. These lines select the register set that determines the frequency of the clock synthesizers. The FS[1:0] pins select the register sets when CC0[7] and CC0[3] = 0. When CC0[7] and CC0[3] = 1, bits in the CC register select the register sets.
43	STROBE	I	**STROBE.** TTL compatible. Input for strobing the reference frequency select lines. The FS[1:0] lines are connected to an internal transparent latch. When STROBE is high, data can be written to FS[1:0]. When STROBE is low, the latch is closed and data cannot be written to FS[1:0]. The falling edge of STROBE latches the FS[1:0] lines. If STROBE is tied permanently high, care must be taken to ensure that there is no noise or glitches on the FS[1:0] inputs.
9	OTCLKA	O	**Output Clock A.** TTL compatible. This pin functions as an output clock from analog PLL synthesizer A.
61	OTCLKB	O	**Output Clock B.** TTL compatible. This pin functions as an output clock from analog PLL synthesizer B.
7	XIN	I	**Crystal Input.** Connect external crystal or stable frequency source to internal crystal oscillator. The recommended frequency is 14.318 MHz system clock. When using a crystal, connect across XIN and XOUT.
6	XOUT	I	**Crystal Output.** Connect external crystal to internal crystal oscillator. All passive components are integrated on-chip to implement a tuned resonant circuit. Leave this pin floating when using a stable external frequency source connected to XIN.
63	PCLK	I	**Pixel Clock.** TTL compatible. The duty cycle of the clock should be between 45% and 55%. When using the analog pixel clock multiplier, the duty cycle can be 30% to 70%. The rising edge of the pixel clock latches the pixels and $\overline{\text{BLANK}}$ inputs.
MPU Port Pins			
5	$\overline{\text{RD}}$	I	**Read (Active-Low).** TTL compatible. When $\overline{\text{RD}}$ is low, data transfers from the selected internal register to the data bus. RS[1:0] is latched on the falling edge of $\overline{\text{RD}}$.
19—12	D[7:0]	I/O	**Data Bus.** TTL compatible. Data is transferred between the data bus and the internal registers under control of the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals. In an MPU write operation, D[7:0] is latched on the rising edge of $\overline{\text{WR}}$. To read data D[7:0] from the device, $\overline{\text{RD}}$ must be in an active-low state. The rising edge of the $\overline{\text{RD}}$ signal indicates the end of a read cycle. Following the read cycle, the data bus will go to a high-impedance state. **Note:** For 6-bit operation, color data is contained in the lower 6 bits of the data bus. D0 is the LSB, and D5 is the MSB. When the MPU writes color data, D6 and D7 are ignored. During MPU read cycles, D6 and D7 are a logic 0.

Pin Information (continued)

Table 2. Pin Descriptions (continued)

Pin #	Symbol	Type	Name/Function
20	$\overline{WR}$	I	**Write (Active-Low).** TTL compatible. $\overline{WR}$ controls the data transfer from the data bus to the selected internal register. D[7:0] data is latched at the rising edge of $\overline{WR}$, and RS[1:0] data is latched at the falling edge of $\overline{WR}$.
22, 21	RS[1:0]	I	**Register Select.** TTL compatible. These inputs are sampled on the falling edge of the $\overline{RD}$ or $\overline{WR}$ to determine which one of the internal registers is to be accessed.
DAC Pins			
38, 39, 40	RED GREEN BLUE	O	**Color Signals.** These pins are analog outputs. High-impedance current sources are capable of driving a double-terminated 75 Ω coaxial cable.
48	RSET	I	**Reference Resistor.** An external resistor (RSET) is connected between the RSET pin and GND to control the magnitude of the full-scale current. Refer to DAC Gain section under Functional Description.
49	COMP	I	**Compensation Pin.** Bypass this pin with an external 0.1 µF capacitor to Vcc.
51	VREF	—	**Voltage Reference.** Bypass this pin with an external 0.1 µF capacitor to GND.
68	$\overline{SENSE}$	O	**$\overline{SENSE}$ (Active-Low).** TTL compatible. Monitor detect signal. $\overline{SENSE}$ is a logic 0 if one or more of the red, green, or blue outputs has exceeded the internal voltage reference level of 340 mV ± 70 mV.
Miscellaneous Pins			
24, 28—34, 46, 47, 50	NC	—	**No Connect.** No internal connection to the chip.
26	$\overline{RESET}$	I	**$\overline{RESET}$.** TTL compatible. This pin resets internal registers to $00 and programs the clock synthesizer register sets to produce 28.322 MHz and 25.175 MHz.
Power and Ground Pins			
8, 27, 35, 62	VccD	—	**Power, Digital.** Connect these pins to +5 V. These pins can be connected to the filtered supply plane or connected to the digital supply plane of the RAMDAC.
2, 10, 36, 37, 41, 60	GND	—	**Ground.** Connect these pins to circuit ground.
42	VccA	—	**Power, Analog.** Connect this pin to +5 V. This pin supplies the power for the analog DACs and should be connected to a filtered supply plane.
3	VccS	—	**Power, Clock Synthesizer.** Connect this pin to +5 V. This can be a separate supply from the RAMDAC. See Application Information section.

Register Descriptions

Table 3. Standard Register Set

These registers are accessed directly by using RS[1:0].

Addressed by MPU	RS1	RS0	Register Name	Access	VGA PORT
Address Register (write mode)	0	0	WMA	R/W	3C8
Look-up Table Data Register; Sends Data to Pixel Color RAM	0	1	LUT	R/W	3C9
Pixel Read Mask Register	1	0	RMR	R/W	3C6
Address Register (read mode)	1	1	RMA	R/W	3C7

Table 4. State Machine Register Set

The pixel read mask register can be accessed using the state machine by setting CR0[0] = 0. When CR0[0] = 0, the registers can be accessed through the back door using the state machine. This mode is ATT21C498 function compatible and allows access to all '498 level functionality. For programming CR1, CC, and the clock synthesizer registers, indexed addressing must be used. RS[1:0] = 10 for all registers in this table.

Addressed by MPU	Register Name	Access	RMR Reads CR0[0] = 0
Pixel Read Mask Register	RMR	R/W	1—4
Control Register 0	CR0	R/W	5
Manufacturer's Identification Register	MIR	Read	6
Device Identification Register	DIR	Read	7
Test register for Red, Green, and Blue Signature Analysis	TST	R/W	8—10

Register Descriptions (continued)

Table 5. Indexed Register Set

These registers can be accessed by indexing.

Note: CR0 must be accessed through the RMR to set bit 0 to a 1 before indexed accessing can be used (see Functional Description). RS[1:0] = 10 for all registers in this table.

Addressed by MPU	Register Name	Access	Index (CR0[0] = 1)	Reset Value (Hex)	Reset Frequency (MHz)
Pixel Read Mask Register.	RMR	R/W	$00	FF *	—
Control Register 0.	CR0	R/W	$01	00	—
Manufacturer's Identification Register.	MIR	Read	$02	84	—
Device Identification Register.	DIR	Read	$03	09	—
Test Register for Red, Green, and Blue Signature Analysis.	TST	R/W	$04	—	—
Control Register 1.	CR1	R/W	$05	00	—
Clock Synthesizer Control Register.	CC	R/W	$06	00	—
Clock A Control Register 0 of Set A.	AA0	none	—	1A	25.175
Clock A Control Register 1 of Set A.	AA1	none	—	C0	
Clock A Control Register 2 of Set A.	AA2	none	—	A6	
Clock A Control Register 0 of Set B.	AB0	none	—	3D	28.322
Clock A Control Register 1 of Set B.	AB1	none	—	C2	
Clock A Control Register 2 of Set B.	AB2	none	—	A6	
Clock A Control Register 0 of Set C.	AC0	R/W	$48	1A	50.000
Clock A Control Register 1 of Set C.	AC1	R/W	$49	80	
Clock A Control Register 2 of Set C.	AC2	R/W	$4A	84	
Clock A Control Register 0 of Set D.	AD0	R/W	$4C	28	75.000
Clock A Control Register 1 of Set D.	AD1	R/W	$4D	42	
Clock A Control Register 2 of Set D.	AD2	R/W	$4E	A8	
Clock B Control Register 0 of Set A.	BA0	none	—	41	30.000
Clock B Control Register 1 of Set A.	BA1	none	—	C2	
Clock B Control Register 2 of Set A.	BA2	none	—	A6	
Clock B Control Register 0 of Set B.	BB0	none	—	36	40.000
Clock B Control Register 1 of Set B.	BB1	none	—	83	
Clock B Control Register 2 of Set B.	BB2	none	—	C4	
Clock B Control Register 0 of Set C.	BC0	none	—	1A	50.000
Clock B Control Register 1 of Set C.	BC1	none	—	80	
Clock B Control Register 2 of Set C.	BC2	none	—	84	
Clock B Control Register 0 of Set D.	BD0	R/W	$6C	41	60.000
Clock B Control Register 1 of Set D.	BD1	R/W	$6D	82	
Clock B Control Register 2 of Set D.	BD2	R/W	$6E	A6	

* Pixel read mask register (RMR) reset default—only after a $\overline{\text{RESET}}$. Contents unknown after powerup.

Register Descriptions (continued)

Internal Register Set

Tables 3, 4, and 5 list the internal register set of the ATT20C408. This device is designed to support enhanced features in a VGA compatible architecture. A typical VGA system only supports RS0 and RS1 register select signals. With only two register select lines, access to four registers is provided (see Table 3). In order to provide enhanced features, additional register locations are required and need to be located in the VGA accessible register space.

To provide the additional registers, a back door has been added. The back door provides access to a control register (CR0), a manufacturer's identification register (MIR), a device identification register (DIR), and test registers. The back door is opened by sequential reads to the pixel read mask register (RMR). The pixel read mask register was chosen because it is not used often in normal VGA operation.

The second method is indexed addressing. Indexed addressing can be used to access the RMR, CR0 (when CR0[0] = 1), MIR, DIR, TST, CR1, CC, and all the registers in Table 5. Indexed addressing is the only way to read or write CR1, CC, and the registers in Table 5.

To use this method, set CR0[0] = 1 by using the back door (multiple accesses to the RMR) or state machine addressing as indicated in Table 4. Write the address register (WMA) with the address of the register to be read or written. The index of the registers accessible are listed in the index column in Tables 3, 4, and 5. Perform a read or write operation when RS[1:0] = 10. The value will be read from, or written to, the register indexed by the contents of the address register. The following sections explain access to the standard registers.

Write Mode Address Register (WMA)

The write mode address register holds an 8-bit value that is used as an index when writing into the LUT data register, or extended registers.

This register points to one of the 256 look-up table (LUT) RAM address locations. Each of the LUT locations is 24 bits wide (8 bits red, 8 bits green, and 8 bits blue). To write all 24 bits of a LUT location, three successive writes are made to the same address. After the sequence of three writes is completed, the 24-bit value is transferred to the specified LUT's RAM address.

The WMA register is an autoincrementing register. When three writes to the LUT data register are complete, the LUT data register value is written to the LUT and the WMA register increments by 1. For this reason, the WMA should be written every time indexed registers are accessed.

Table 6. Standard Register Set

The LUT and RMR registers apply only in the 8-bit modes.

Reg. Name	Reg. Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WMA	R/W	A7	A6	A5	A4	A3	A2	A1	A0
LUT	R/W	D7	D6	D5	D4	D3	D2	D1	D0
RMR	R/W	M7	M6	M5	M4	M3	M2	M1	M0
RMA	R/W	A7	A6	A5	A4	A3	A2	A1	A0

Read Mode Address Register (RMA)

The read mode address register holds an 8-bit value that is used as an index when reading from the LUT data register, or extended registers.

This register also points to one of the 256 LUT RAM address locations. To read all 24 bits of a LUT location, three successive reads are made to the same address.The RMA register is an autoincrementing register. When written to, the RMA reads the LUT into the LUT data register and then increments. When the three reads from the LUT data register are complete, the device transfers the new LUT data at the RMA address into the LUT data register and increments again.

When using the RMA for access to the indexed registers, write a value one less than the desired index. The RMA register will increment by one before using the index to access the information being read or written.

LUT Data Register

The LUT data register is a data port through which reads and writes are made to the LUT. The LUT write mode address or read mode address registers are used to specify which LUT location is to be accessed. This register is an 8-bit port located in a 24-bit location. Three accesses are needed to read or write the LUT data register.

Register Descriptions (continued)

Because both the LUT write mode address and LUT read mode address registers are autoincrementing, accesses to this port should be made three at a time to avoid leaving a partial read or write to the LUT data register. A partially written data register is not transferred to the LUT. The blue value must be written before the LUT is updated.

Pixel Read Mask Register (RMR)

The contents of the pixel read mask register (RMR) can be accessed by the MPU at any time and are not initialized on powerup. The RMR bits are logic ANDed with the 8-bit pixels in pseudocolor mode. In true-color modes, pixels are not modified by the RMR. A logic 1 stored in a data bit of the read mask register leaves the corresponding bit in the pixel unchanged. A logic 0 in the read mask register sets the pixel bit to 0. Bit D0 of the pixel read mask register corresponds to pixel bit P0.

Reading the RMR four times without accessing another RAMDAC register will direct the next (fifth) access (read or write) to control register 0. The sixth consecutive read from the RMR will return the manufacturer identification register (MIR); the seventh consecutive read from the RMR will return the device identification register (DIR); and the eighth, ninth, and tenth consecutive reads from the RMR will return the signature analysis registers RTEST, GTEST, and BTEST. An eleventh read from the RMR results in the state machine being reset and RMR value being returned. See Figure 4.

Manufacturer Identification Register (MIR)

This 8-bit register contains an 8-bit value to identify the manufacturer of the RAMDAC. The MIR is read by reading the RMR six times without accessing any other RAMDAC register. The first four reads will return the contents of the RMR; the fifth read will return the CR0 contents; the sixth read will return the MIR contents; and the seventh read will return the DIR contents.The ATT20C408 returns the value 84 hex on the sixth read.

Device Identification Register (DIR)

This 8-bit register contains an 8-bit value to identify the type of RAMDAC. The DIR is read by reading the RMR seven times without accessing any other RAMDAC register. The ATT20C408 returns the value 09 hex.

Test Registers

The red, green, and blue test registers will analyze red, green, or blue signatures by using linear feedback shift registers (LFSRs). During signature analysis, the R, G, and B data is sampled and compressed at the pixel clock frequency. The signature is accumulated based on the initial seed value. A new signature value is produced every pixel clock. When writing a seed value to the test register, the red, green, and blue test registers are all seeded with the same value. When writing the seed value to the signature analysis registers (SARs), only write the seed to the red SAR. The seed value will be automatically copied to the green and blue SARs.

Table 7. Accessing the RMR Enables Indirect Access of CR0, MIR, and DIR

RMR Read #	Register Name	Register Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5	CR0	Read/Write	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
6	MIR	Read Only	1	0	0	0	0	1	0	0
7	DIR	Read Only	0	0	0	0	1	0	0	1

Table 8. Accessing the RMR Enables Indirect Access to RTEST, GTEST, and BTEST

RMR Read #	Register Name	Register Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8	RTEST	Read/Write	R7	R6	R5	R4	R3	R2	R1	R0
9	GTEST	Read/Write	G7	G6	G5	G4	G3	G2	G1	G0
10	BTEST	Read/Write	B7	B6	B5	B4	B3	B2	B1	B0

Register Descriptions (continued)

Attempting to write a seed value to the green or blue SARs will result in the last value written being copied to all three SARs. Reading the RMR register eight, nine, and ten times will produce the red, green, and blue signatures. The first value read is the red signature, followed by the green and blue signatures (see Table 8). The test register may be read or written only during the blanking interval. During active video, the signatures are being accumulated. When $\overline{\text{BLANK}}$ is low, the SARs are frozen. When $\overline{\text{BLANK}}$ rises, signatures accumulate to whatever value is in the SARs.

Control Register 0 (CR0)

The control register is written to or read by the MPU and is not initialized at powerup. CR0 bit 0 is the least significant bit in the control register and corresponds to D0 of the MPU port. Table 9 defines the bits of the control register. CR0 bits [7:4] determine the color mode as shown in Table 17.

CR0 bit [3] — Setting this bit to a 1 places the RAMDAC in powerdown mode. In the powerdown state, the device retains the information in the color look-up table. Access to the color look-up table is disabled during sleep. The internal registers can be written while the device is sleeping.

CR0 bit [2] is reserved.

CR0 bit [1] — 8-/6-bit Select — Determines whether the MPU port reads and writes 8 bits or 6 bits of color data to the color look-up table RAM. In 6-bit mode, color data is on the lower 6 bits of the data bus, with D0 being the LSB and D5 being the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be logic 0. Note that in the 6-bit mode, the full-scale output current will be about 1.5% lower than when in the 8-bit mode. This is a result of the two LSBs of each 8-bit DAC always being a logic 0 in the 6-bit mode. In the 8-bit color mode, bit D0 is the color data LSB and bit D7 is the MSB.

CR0 bit [0] controls access to the indexed addressed registers.

Table 9. Control Register 0

This register is operational upon powerup. It can be read or written to by the MPU at any time and is not initialized. All bits are set to zero upon asserting $\overline{\text{RESET}}$. To read or write this register, use the internal state machine for access via the read mask register (see Table 4).

Bit	Name/Description
CR0[7:4]	**Color Mode.** These bits are used to control the color modes (see Table 17).
CR0[3]	**Powerdown (RAMDAC).** Logic 0: Normal operation. Logic 1: Sleep. Powers the RAMDAC off. Device does not wake up for MPU updates. The data in the LUT is maintained during powerdown. Internal registers can be accessed while the RAMDAC is asleep. CR1[3:2] powers down the clock synthesizers (for green PC compatibility).
CR0[2]	**Reserved.**
CR0[1]	**8/6-bit Select.** Logic 0: 6-bit data to the DAC. Logic 1: 8-bit data to the DAC. A logic 1 specifies 8 bits per DAC operation (16M possible colors). A logic 0 specifies 6 bits per DAC operation (256K possible colors).
CR0[0]	**Extended Register Enable (Indirect or Indexed Access).** Logic 0: Disables indexed access to extended registers. Logic 1: Enables indexed access to extended registers. This bit controls access to the extended registers. If this bit is a logic 0, access to the extended registers is enabled by multiple accesses to the read mask register (state machine addressing). This does not allow access to CR1, clock control, or configuration registers. If this bit is a logic 1, all extended registers can be accessed with indexed addressing using the WMA or RMA registers as an address pointer, and the read mask register with register select lines RS[1:0] = 10.

Register Descriptions (continued)

Control Register 1 (CR1)

This register is operational on powerup. It can be read or written to by the MPU at any time and is not initialized. All bits are set to zero upon asserting $\overline{\text{RESET}}$. To read or write this register, set bit CR0[0] = 1, write $05 to the WMA, and set RS[1:0] = 10. This register can be accessed by using indexed addressing (see Table 5). CR1 bit 0 is the least significant bit and corresponds to D0 on the MPU port.

Table 10 defines the bits of the control register. CR1[7] = 1 disables the crystal oscillator. This must be enabled to use an external crystal for the reference frequency. This must be disabled to achieve minimum powerdown supply current. Bits CR1[6:5] determine whether the digital clock doubler or the analog clock multiplier are used. They also determine the frequency range of the multiplier.

Bit 4 enables the blank pedestal. Bit 3 powers down clock synthesizer A. Bit 2 powers down clock synthesizer B. Bit 1 disables the $\overline{\text{SENSE}}$ output pin.

Bit 0 is reserved. Bit 0 always returns a zero regardless of what value is written.

Table 10. Control Register 1

Bit	Name/Description
CR1[7]	**Crystal Oscillator Disable.** Logic 0: Enable the crystal oscillator. Logic 1: Disable the crystal oscillator. This bit enables or disables the internal crystal oscillator. This bit must be enabled to use an external crystal. This bit should be a logic 1 to achieve the lowest power state for the device.
CR1[6:5]	**Frequency Range Select: 2X Clock Multiplier.** Logic 00: Digital doubler. Logic 01: Program PLL greater than or equal to 45 MHz. Logic 10: Program PLL from 22.5 MHz to 45 MHz. Logic 11: Program PLL from 11.25 MHz to 22.5 MHz. Programming these bits helps ensure minimum jitter for the analog clock doubler. These bits must be programmed for mode 13 in Table 17.
CR1[4]	**Blank Pedestal Enable.** Logic 0: No blank pedestal. Logic 1: Blank pedestal enabled. This pin controls whether the $\overline{\text{BLANK}}$ pin shuts off a 7.5 IRE current source on R, G, and B when blanking is asserted. For VGA compatibility, write a 0 to this bit.
CR1[3]	**OTCLKA Synthesizer Powerdown.** Logic 0: OTCLKA synthesizer enabled. Logic 1: OTCLKA synthesizer powered down and output is 3-stated. A logic 1 disables clock synthesizer A. This bit should be a logic 1 to achieve the lowest power state for the device. Set this bit to a logic 1 when not using clock synthesizer A.
CR1[2]	**OTCLKB Synthesizer Powerdown.** Logic 0: OTCLKB synthesizer enabled. Logic 1: OTCLKB synthesizer powered down and output is 3-stated. A logic 1 disables clock synthesizer B. This bit should be a logic 1 to achieve the lowest power state for the device. Set this bit to a logic 1 when not using clock synthesizer B.
CR1[1]	**$\overline{\text{SENSE}}$ Disable.** Logic 0: $\overline{\text{SENSE}}$ pin enabled. Logic 1: $\overline{\text{SENSE}}$ pin disabled and output is 3-stated. A logic 0 enables the $\overline{\text{SENSE}}$ pin to output the sense signal.
CR1[0]	**Reserved.** This bit always returns a zero without regard to what was written.

Register Descriptions (continued)

Clock Synthesizer Control Register (CC)

This register is operational on powerup. It can be read or written to by the MPU at any time. All bits are set to zero upon asserting $\overline{\text{RESET}}$. To read/write this register, set bit CR0[0] = 1, write $06 to the WMA, and set RS[1:0] = 10. This register can be accessed via indexed addressing (see Table 5). CC bit 0 is the least significant bit and corresponds to D0 on the MPU port.

Table 11 defines the bits of the clock synthesizer control register. CC[7] determines whether the frequency select input pins FS[1:0] or the clock synthesizer control register bits CC[5:4] control the frequency selection for clock synthesizer A and OTCLKA. Bit CC[6] is reserved, and this bit may be read and will return the value written, but will not affect the function of the device.

Table 11. Clock Synthesizer Control Register

Bit	Name/Description
CC[7]	**Control Option Clock A Select.** Logic 0: Input pins FS[1:0] control clock A. Logic 1: Bits CC[5:4] control clock A. This bit determines what is controlling clock synthesizer A.
CC[6]	**Reserved.** This bit may be read and will return the value written, but will not affect the function of the device.
CC[5:4]	**Register Set Select (for Clock A).** Logic 00: Register set A. (Fixed frequency selection.) Logic 01: Register set B. (Fixed frequency selection.) Logic 10: Register set C. (Programmable frequency selection.) Logic 11: Register set D. (Programmable frequency selection.) These bits select which register set will configure clock A.
CC[3]	**Control Option Clock B Select.** Logic 0: Input pins FS[1:0] control clock B. Logic 1: Bits CC[1:0] control clock B. This bit determines what is controlling clock synthesizer B.
CC[2]	**Reserved.** This bit may be read and will return the value written, but will not affect the function of the device.
CC[1:0]	**Register Set Select (for Clock B).** Logic 00: Register set A. (Fixed frequency selection.) Logic 01: Register set B. (Fixed frequency selection.) Logic 10: Register set C. (Fixed frequency selection.) Logic 11: Register set D. (Programmable frequency selection.) These bits select which register set will configure clock B.

Register Descriptions (continued)

Clock Synthesizer Register Sets

The clock synthesizer register sets determine the frequency of OTCLKA and OTCLKB for a given reference frequency. There are four sets for OTCLKA and four sets for OTCLKB. One set of registers is chosen by toggling either the FS[1:0] pins or the CC[5:4] or CC[1:0] bits.

Each register set consists of four registers. The four registers have information affecting seven functions of the clock synthesizer. The feedback divider term, M, together with the reference divider term and postscaler terms determine the frequency according to equation 1 in the clock synthesizer section. The M term is 8 bits, the N term is 6 bits, and the P term is 2 bits. The loop filter and bias control bits determine the loop filter time constant and phase detector gain. Table 12 shows the fields associated with each term. The fourth register is reserved and can be read. It will return the value written, but will not affect the function of the device.

Table 12. Fields for Clock Register Sets

Clock Register 0, Bits and Fields								Clock Register 1, Bits and Fields							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
M[7:0]								P[1:0]		N[5:0]					
Clock Register 2, Bits and Fields								**Clock Register 3, Bits and Fields**							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
L[3:0]				IB[3:0]				Reserved							

Notes:
M[7:0], 8 bits, integer from 0 to 255 (two will be added to this value). P[1:0], 2 bits, integer from 0 to 3 (this bit indicates the power of two). N[5:0], 6 bits, integer from 0 to 63 (two will be added to this value). L[3:0], 4 bits, integer from 0 to 15. IB[3:0], 4 bits, integer from 0 to 15.

Table 13. Parameters for Clock A

This register is operational on powerup. It can be read or written to by the MPU at any time. All bits are reset to the values in Table 5 upon asserting $\overline{\text{RESET}}$. To read or write this register, set bit CR0[0] = 1, write $40—$4F to the WMA, and set RS[1:0] = 10. These registers can be accessed via indexed addressing (see Table 5).

Register	Control Set	Access	Reg. #	Description
AA0[7:0]	A CC[5:4] or FS[1:0] = 00	None	0	Feedback divider term (M)
AA1[7:6] AA1[5:0]			1	Postscaler (P) Reference divider (N)
AA2[7:4] AA2[3:0]			2	Loop filter control bits (L) Ibias control (IB)
AB0[7:0]	B CC[5:4] or FS[1:0] = 01	None	0	Feedback divider term (M)
AB1[7:6] AB1[5:0]			1	Postscaler (P) Reference divider (N)
AB2[7:4] AB2[3:0]			2	Loop filter control bits (L) Ibias control (IB)
AC0[7:0]	C CC[5:4] or FS[1:0] = 10	Read or Write	0	Feedback divider term (M)
AC1[7:6] AC1[5:0]			1	Postscaler (P) Reference divider (N)
AC2[7:4] AC2[3:0]			2	Loop filter control bits (L) Ibias control (IB)
AD0[7:0]	D CC[5:4] or FS[1:0] = 11	Read or Write	0	Feedback divider term (M)
AD1[7:6] AD1[5:0]			1	Postscaler (P) Reference divider (N)
AD2[7:4] AD2[3:0]			2	Loop filter control bits (L) Ibias control (IB)

Register Descriptions (continued)

Table 14. Parameters for Clock B

This register is operational on powerup. It can be read or written to by the MPU at any time. All bits are reset to the values in Table 5 upon asserting $\overline{\text{RESET}}$. To read or write this register, set bit CR0[0] = 1, write $40—$4F to the WMA, and set RS[1:0] = 10. These registers can be accessed via indexed addressing (see Table 5).

Register	Control Set	Access	Reg. #	Description
BA0[7:0]	A CC[1:0] or FS[1:0] = 00	None	0	Feedback divider term (M)
BA1[7:6] BA1[5:0]			1	Postscaler (P) Reference divider (N)
BA2[7:4] BA2[3:0]			2	Loop filter control bits (L) Ibias control (IB)
BB0[7:0]	B CC[1:0] or FS[1:0] = 01	None	0	Feedback divider term (M)
BB1[7:6] BB1[5:0]			1	Postscaler (P) Reference divider (N)
BB2[7:4] BB2[3:0]			2	Loop filter control bits (L) Ibias control (IB)
BC0[7:0]	C CC[1:0] or FS[1:0] = 10	None	0	Feedback divider term (M)
BC1[7:6] BC1[5:0]			1	Postscaler (P) Reference divider (N)
BC2[7:4] BC2[3:0]			2	Loop filter control bits (L) Ibias control (IB)
BD0[7:0]	D CC[1:0] or FS[1:0] = 11	Read or Write	0	Feedback divider term (M)
BD1[7:6] BD1[5:0]			1	Postscaler (P) Reference divider (N)
BD2[7:4] BD2[3:0]			2	Loop filter control bits (L) Ibias control (IB)

Functional Description

State Machine Access to Extended Registers

State machine access to the extended registers is provided to give backward compatibility to the ATT21C498 RAMDAC. Indirect access to the extended registers is described by a state diagram shown in Figure 4. Table 16 indicates the register access in each state. The extended registers accessible in this manner are CR0, MIR, DIR, RTEST, GTEST, and BTEST.

To read CR0, read the RMR five times. The fifth read results in the contents of CR0. To write CR0, read the RMR four times. This sets an internal flag allowing access to control register 0. The next write will be directed to control register 0. The MIR, DIR, and test registers are accessed in a similar manner, as shown by Figure 4. The sixth read of the RMR results in the MIR (read only). The seventh read of the RMR results in the DIR (read only). The eighth, ninth, and tenth reads of the RMR result in the red, green, and blue signature analysis registers. A further read resets the state machine back to state 0.

Table 15 indicates I/O operations that reset the state machine to state 0. Any write operation will reset the state machine to state 0.

Table 15. I/O Operations Reset the State Machine to State 0

$\overline{WR}$	RS1	RS0
↓	0	0
↓	0	1
↓	1	0
↓	1	1

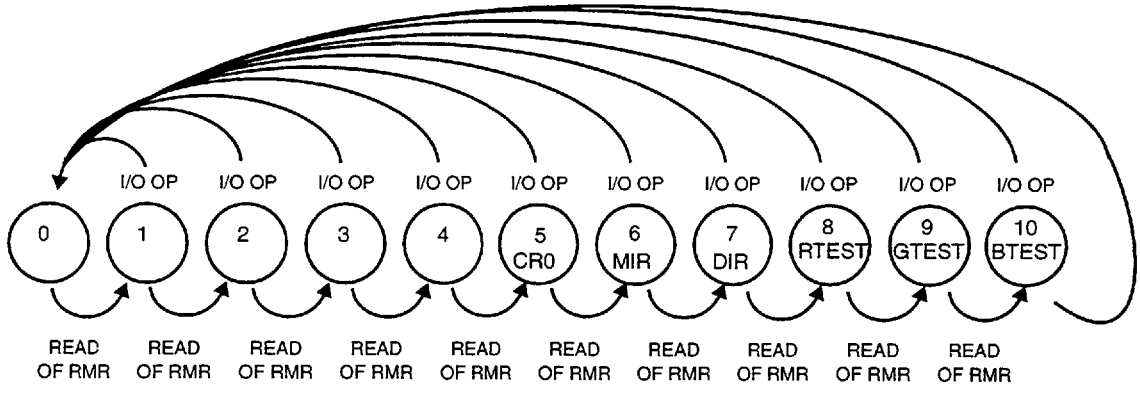
Indexed Access to Extended Registers

Indexing provides another way to access the extended registers. Indexing is the only way to access CR1, CC, and the clock synthesizer register sets. CR0 must be accessed through state machine addressing to set bit 0 to a 1 before indexed accessing can be used. The CR0, MIR, DIR, RTEST, GTEST, and BTEST registers can be accessed either by the RMR or by indexing.

To use this method, do the following:

1. Set CR0[0] = 1 using state machine accessing (multiple accesses to the RMR).
2. Write the address register (WMA) with the address of the register to be read or written.
3. Set RS[1:0] = 10.
4. Perform a read or write operation.

The value will be read from or written to the desired register. The address register does not increment automatically. If the RMA is used for indexing, write a value one less than the desired value. The RMA increments before being used as an index. The address of the registers accessible by indexing are listed in the Index column in Table 5.



Note: I/O OP is any I/O write to 3C6, 3C7, 3C8, or 3C9.

Figure 4. State Diagram Illustrating Access to Indirect Registers

Functional Description (continued)

Table 16. State Table Showing Access to CR0, MIR, DIR, and Test Registers

State	State Entry Conditions	State Activity
0	Any I/O write.	Normal I/O access.
1	Read of RMR while in state 0.	Normal I/O access.
2	Read of RMR while in state 1.	Normal I/O access.
3	Read of RMR while in state 2.	Normal I/O access.
4	Read of RMR while in state 3.	Normal I/O access.
5	Read or write of RMR while in state 4.	I/O access to CR0.
6	Read of RMR while in state 5.	Returns manufacturer identification.
7	Read of RMR while in state 6.	Returns device identification number.
8	Read of RMR while in state 7.	Returns RTEST signature analysis register.
9	Read of RMR while in state 8.	Returns GTEST signature analysis register.
10	Read of RMR while in state 9.	Returns BTEST signature analysis register.

Color Modes

The ATT20C408 provides nine different color modes that are selectable by programming the MPU control register bits CR0[7:4] (see Table 17).

in true-color modes with multiple or fractional clocks per pixel, a clock multiplier will provide the internal load pulse that latches the data into a 16- or 24-bit pixel. True-color modes bypass the look-up table and are not gamma corrected. A discussion of each mode follows.

Mode 0: (See Figure 5.) This mode displays data formatted in 8-bit pseudocolor. Mode 0 is selected by setting control register CR0 bits [7:4] to 0000. Mode 0 ignores the P[23:8] inputs.

Mode 1: (See Figure 6.) This mode displays data formatted for 15-bit per pixel true color (5/5/5). The mode switch is determined by the C bit (P15). When C = 0, the pixel data is interpreted as 15-bit true color. When C = 1, the pixel data is interpreted as mode 0, 8-bit pseudocolor. This mode is selected by setting control register CR0 bits [7:4] to 0001. Mode 1 uses all P[15:0] inputs.

Mode 2: This mode accepts two 8-bit pseudocolor pixels on each clock. This mode is selected by setting control register CR0 bits [7:4] to 0010. The internal clock doubler outputs the pixels at twice the PCLK frequency. This allows the RAMDAC to output 8-bit pseudocolor pixels at 135 MHz with 67.5 MHz data rates. Mode 2 uses all P[15:0] inputs.

Mode 3: This mode formats data in 16-bit per pixel true color. This mode is selected by setting control register CR1 bits [7:4] to 0011. Mode 3 uses all P[15:0] inputs (see Figure 5).

Mode 4: This mode accepts data formatted as 8-bit pseudocolor latched by two pixel clocks as 4-bit nibbles. Latching two nibbles allows backward compatibility to previous RAMDACs. This mode is selected by setting control register CR0 bits [7:4] to 0100. Mode 4 ignores the P[15:4] inputs.

Mode 5: This mode accepts a 24-bit pixel formatted as two 16-bit words latched by two pixel clocks. This is not a packed mode. On the second pixel clock, the upper byte is ignored. This mode is selected by setting control register CR0 bits [7:4] to 0101. Mode 5 uses all P[15:0] inputs.

Mode 6: The 16-bit 5/6/5 pixel is latched in 2 bytes with two PCLKs. Latching 1 byte per clock allows backward compatibility to previous RAMDACs. This mode is selected by setting control register CR0 bits [7:4] to 0110. $\overline{\text{BLANK}}$ going high will signal that the first pixel information is available on P[15:0]. The rising edge of PCLK that captures $\overline{\text{BLANK}}$ going high also captures the LSBs of the pixel information. The LSBs are latched first followed by the MSBs. The LSBs and MSBs follow in succession until $\overline{\text{BLANK}}$ goes low. The LSBs of the DACs are set to logic zero. Mode 6 ignores the P[15:8] inputs.

Mode 7: The 24-bit pixel is latched in 3 bytes with three PCLKs. This mode is selected by setting the control register CR0 bits [7:5] to 0111. The pixel information is collected over three rising edges of the pixel clock. $\overline{\text{BLANK}}$ going high will signal the first pixel information is available on P[7:0]. P[15:8] are ignored. The rising edge of PCLK that captures $\overline{\text{BLANK}}$ going high also captures the blue information of the first pixel. The blue pixel is latched first followed by the green and red. Blue, green, and red follow in succession until $\overline{\text{BLANK}}$ goes low. Mode 7 ignores the P[15:8] inputs.

Functional Description (continued)

Modes 8 through 13: Reserved.

Mode 14: This mode is 24-bit true color packed using P[15:0] pins. This mode formats data in packed 24-bit-per-pixel true color (two pixels for three pixel clocks). 24 bits of BGR data are latched every 1 1/2 pixel clocks or two 24-bit pixels every three pixel clocks. An internal clock multiplier multiplies the external pixel clock by two-thirds (2/3). This mode is selected by setting control register CR1 bits [7:4] to 1110. Mode 14 uses all P[15:0] inputs (see Figure 7).

Mode 15: Reserved.

Table 17. Color Modes

Table 17 outlines the 16 display formatting modes of the ATT20C408. These modes are set by bits CR0[7:4] of control register 0. Pixel data inputs are only latched on the rising edge of PCLK. P[7:0] indicates an address for the LUT. R, G, or B indicates an input to the DACs. All Rs, Gs, and Bs indicate bypass modes.

Pri. Mode #	Sec. Mode #	CR0 [7:4]	Pri. Mode Description	PCLK	Pixel Data	
					0—7	8—15
0	—	0000	8-bit	↑	P0 P1 P2 P3 P4 P5 P6 P7	X X X X X X X X
1	—	0001	15-bit + C CR0[2] = 1 CR0[2] = 0 CR0[2] = 0	↑	 B3 B4 B5 B6 B7 G3 G4 G5 B3 B4 B5 B6 B7 G3 G4 G5 P0 P1 P2 P3 P4 P5 P6 P7	 G6 G7 R3 R4 R5 R6 R7 C = X G6 G7 R3 R4 R5 R6 R7 C = 0 X X X X X X X X C = 1
2	—	0010	2X 8-bit	↑	P0 P1 P2 P3 P4 P5 P6 P7	P0 P1 P2 P3 P4 P5 P6 P7
3	—	0011	16-bit	↑	B3 B4 B5 B6 B7 G2 G3 G4	G5 G6 G7 R3 R4 R5 R6 R7
4	—	0100	8-bit 2 clock	↑ ↑	P0 P1 P2 P3 X X X X P4 P5 P6 P7 X X X X	X X X X X X X X X X X X X X X X
5	—	0101	24-bit true color	↑ ↑	B0 B1 B2 B3 B4 B5 B6 B7 R0 R1 R2 R3 R4 R5 R6 R7	G0 G1 G2 G3 G4 G5 G6 G7 X X X X X X X X
6	—	0110	16-bit true color	↑ ↑	B3 B4 B5 B6 B7 G2 G3 G4 G5 G6 G7 R3 R4 R5 R6 R7	X X X X X X X X X X X X X X X X
7	—	0111	24-bit true color	↑ ↑ ↑	B0 B1 B2 B3 B4 B5 B6 B7 G0 G1 G2 G3 G4 G5 G6 G7 R0 R1 R2 R3 R4 R5 R6 R7	X X X X X X X X X X X X X X X X X X X X X X X X
8	—	1000	Reserved	—	Reserved	Reserved
9	—	1001	Reserved	—	Reserved	Reserved
10	—	1010	Reserved	—	Reserved	Reserved
11	—	1011	Reserved	—	Reserved	Reserved
12	—	1100	Reserved	—	Reserved	Reserved
13	—	1101	Reserved	—	Reserved	Reserved
14	—	1110	2x 24-bit true color	↑ ↑ ↑	B0 B1 B2 B3 B4 B5 B6 B7 R0 R1 R2 R3 R4 R5 R6 R7 G0 G1 G2 G3 G4 G5 G6 G7	G0 G1 G2 G3 G4 G5 G6 G7 B0 B1 B2 B3 B4 B5 B6 B7 R0 R1 R2 R3 R4 R5 R6 R7
15	—	1111	Reserved	—	Reserved	Reserved

Notes:
CR0[2] = 1 will also cause the C field to be ignored.
The clock multiplier operates in modes 2 and 14. In mode 2, the multiplier doubles the PCLK. In mode 14, the multiplier multiplies PCLK by 2/3.

Functional Description (continued)

Table 18. Color Mode Speed

The following table details the pixel clock and rates of the ATT20C408 for each speed grade. These modes are set by bits CR[7:4] of control register 0. The pipeline delay for each mode is also included.

	170 MHz Max		135 MHz Max		
Primary Mode #	PCLK Max	Pixel Rate (MHz)	PCLK Max	Pixel Rate (MHz)	Pipeline (CLKs)
0	110	110	110	110	6
1	110	110	110	110	6
2	85	170	67.5	135	6
3	110	110	110	110	6
4	110	55	110	55	7
5	110	55	110	55	7
6	110	55	110	55	7
7	110	36	110	36	8
8	—	—	—	—	—
9	—	—	—	—	—
10	—	—	—	—	—
11	—	—	—	—	—
12	—	—	—	—	—
13	—	—	—	—	—
14	110	73	110	73	6
15	—	—	—	—	—

Functional Description (continued)

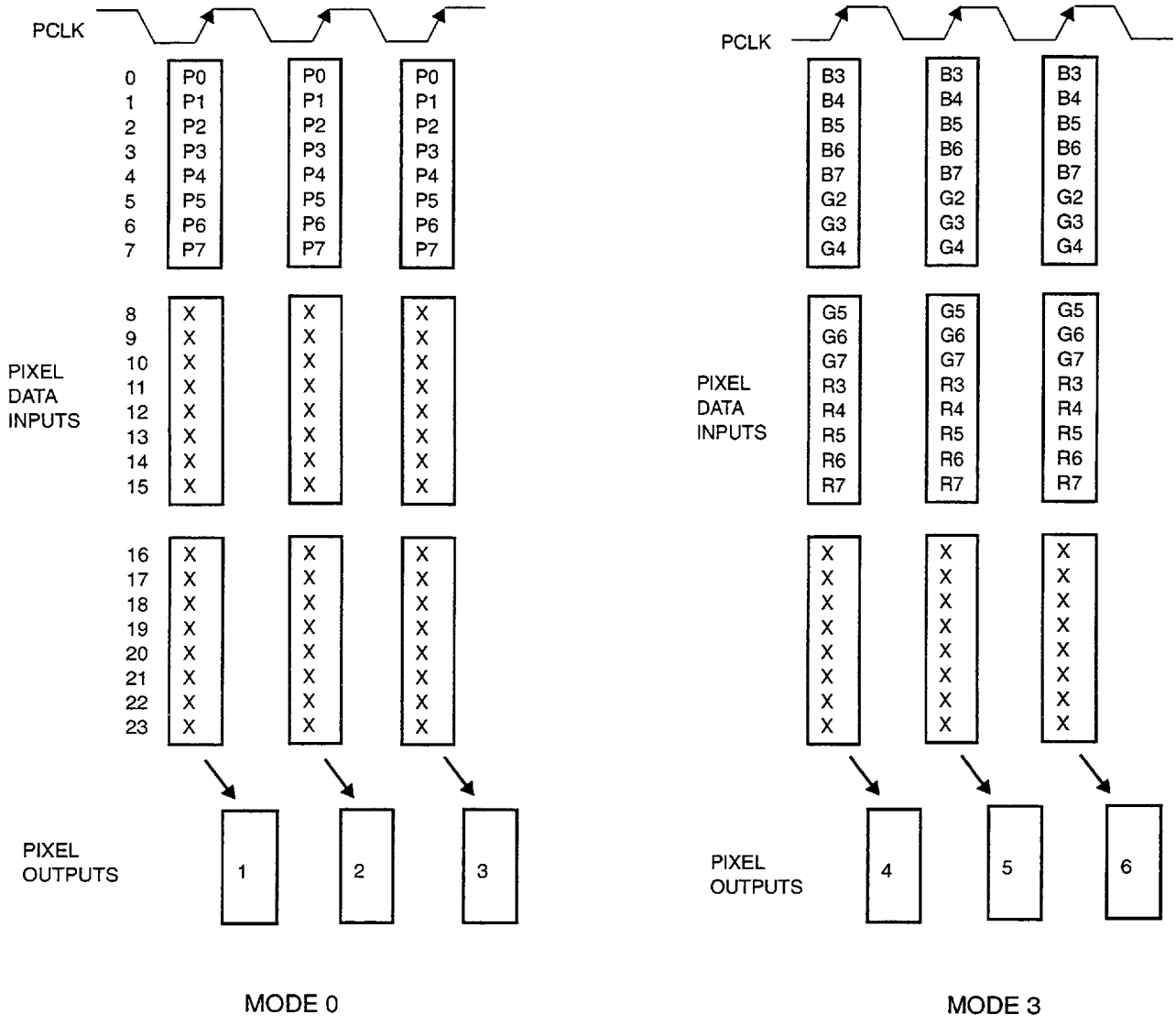


Figure 5. Mode 0 and Mode 3

Functional Description (continued)

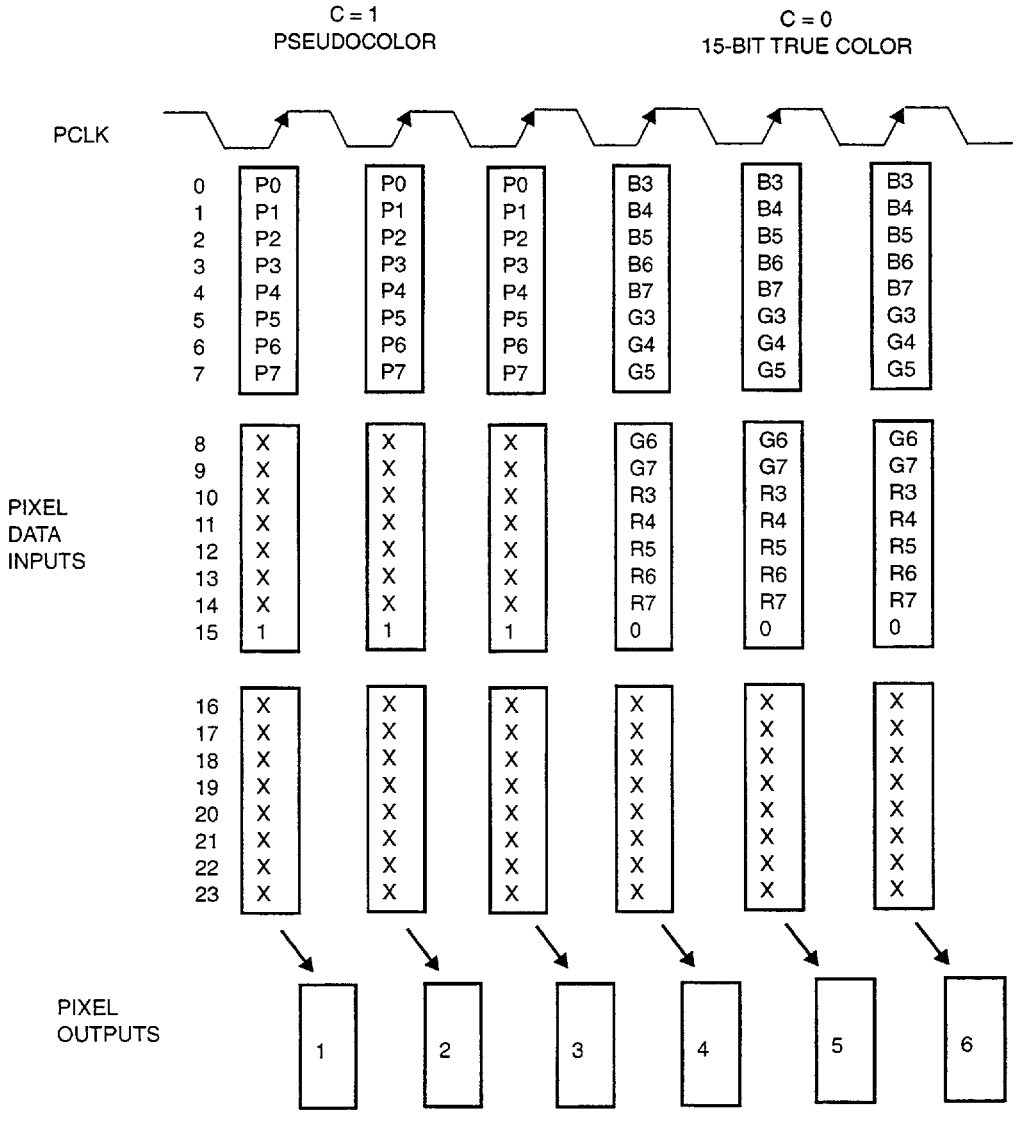


Figure 6. On-the-Fly Mode Switch from 8 Bits Per Pixel to 15 Bits Per Pixel (Mode 1, C = 1 Changing to C = 0, 498 Compatible)

Functional Description (continued)

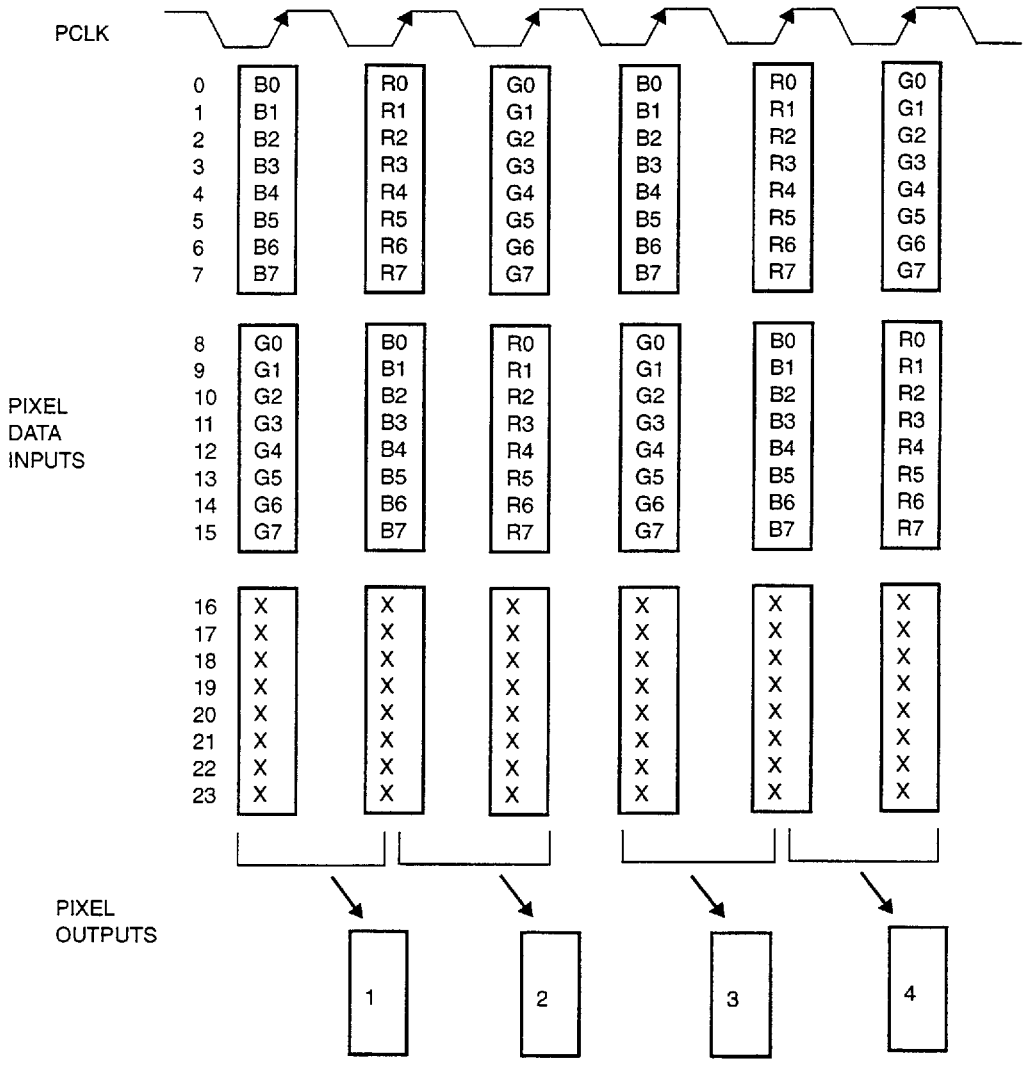


Figure 7. Mode 14, 24 Bits Per Pixel, Packed in 16-Pin Port

In this mode, two pixels are delivered for every three pixel clocks. The internal clock multiplier factor is 2/3. Thus, a 110 MHz PCLK results in a pixel rate of 73 Mpixels/s.

Functional Description (continued)

Clock Synthesizers Description

The ATT20C408 includes dual programmable clock synthesizers. The synthesizer signals are output on the OTCLKA and OTCLKB pins.

An internal loop filter eliminates the need for external loop filter components. The clock synthesizers are included to reduce the number of components on the circuit board. This also reduces the high-frequency signals on the circuit board by generating them internally.

One synthesizer can be used to generate a pixel clock; the other, for a system or memory clock. The synthesizers reset to a predefined frequency. The reset frequencies for the PLL clocks are shown in Table 19. Select the PLL frequencies by programming the clock control registers.

Program the synthesizers by writing to the clock control and configuration registers. These registers are included in the indexed register map of the RAMDAC (see Table 5).

The synthesizer includes a crystal oscillator for connection to an external crystal using XIN and XOUT. XIN can also connect to a standard 14.318 MHz system clock. The synthesizer will synthesize any frequency up to the maximum frequency supported by the device. The maximum frequency is achieved by programming the M, N, and P values in the synthesizer loop.

Once the digital integer values have been programmed in the register sets (up to four), the clock control register bits can switch between the predefined frequencies.

The internal loop filter can be adjusted for loop filter time constant and phase detector gain. The L bits tune the loop filter by adjusting the resistance and changing the time constant. The IB bits change the bias current (or gain) for the charge pump. These values can be adjusted for each frequency on each synthesizer.

Table 19. Clock Synthesizer Reset Frequencies and FS[1:0] Pin Logic Levels

Upon reset, the M, N, and P values are loaded to give the reset frequencies below. The reset frequencies can be changed by reloading new values for M, N, and P.

OTCLKA	
FS[1:0] or CC0[5:4]	**Reset Frequency**
00	25.175
01	28.322
10	50.000
11	75.000
OTCLKB	
FS[1:0] or CC0[1:0]	**Reset Frequency**
00	30.000
01	40.000
10	50.000
11	60.000

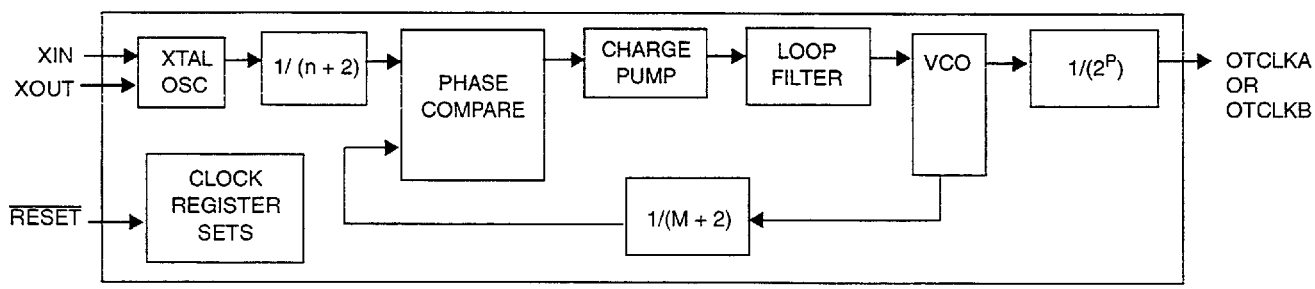


Figure 8. Clock Synthesizer Block Diagram

This diagram is duplicated for the internal PLL clock. (There are two PLLs on-chip.)

Functional Description (continued)

PCLK must meet the minimum high time as specified by the clock period and duty cycle ac specifications. When switching PCLK frequencies, LUT corruption can occur if PCLK high time is not met. Allow approximately 1 second after switching frequencies for the synthesizer outputs to settle to a valid clock signal.

Determining Output Frequency

The output frequency, OTCLK, is determined by the following equation (equation 1).

$$OTCLK = \frac{FREF \times (M+2)}{(N+2) \times 2^P}$$

FREF is the input reference frequency, M is the feedback divider (8 bits), N is the input reference frequency divider (6 bits), and P is the exponent setting the output frequency divider (2 bits). Each synthesizer has four selectable frequencies. There are eight sets of M, N, and P registers. These registers are listed in Table 5.

The values of M, N, and P should be chosen such that the VCO (output frequency before being divided by 2P) is between the values of 120 MHz < VCO < 240 MHz. Choose a low value of N (preferably below 5). Next, choose the value of M that corresponds to the highest VCO frequency in the VCO range that can be divided to yield the desired output frequency.

As an example, for a 55 MHz clock output OTCLKA or OTCLKB, choose the VCO to run at 220 MHz. This requires P = 2 to divide the frequency down by four. Using an FREF of 14.318 MHz, an N = 1, and solving for M, yields M = 44 or $2C.

The loop filter value L and the bias current Ibias have recommended range values. These can be experimented with to determine the best values for each independent application.

Clock synthesizer A and clock synthesizer B can be controlled by frequency select lines or by control register bits. Each synthesizer is independently programmed to determine whether the FS[1:0] pins or the frequency select bits will control its frequency. When both synthesizers are programmed to use the frequency select lines, both synthesizers will move in frequency at the same time to their respective register sets A, B, C, or D. When using the control register bits to control frequency, synthesizers A and B move in frequency independently and can move to different register sets. They do not have to both be set to the same register set A, B, C, or D. See the Applications Information section for component connections and values for the clock synthesizer.

Clock Multiplier

The clock multiplier is a third PLL that is automatically activated when either mode 2 or mode 14 is programmed. In mode 2, the multiplier doubles the PCLK. In mode 14, the multiplier multiplies PCLK by 2/3.

MPU Interface

The ATT20C408 supports a standard MPU interface, allowing the MPU direct access to the WMA, RAMDAC color RAM, RMR, or RMA. As outlined in Table 3, the RS[1:0] select inputs indicate whether the MPU is accessing the address register WMA, RAMDAC color RAM, RMR, or RMA. To eliminate the requirement for external address multiplexers, the 8-bit address register is used to address the RAMDAC RAM. The address register is also used as an indexed address to access the extended registers inside the ATT20C408. For indexed addressing, CR0[0] = 1, RS[1:0] = 10 becomes the indexed data register. WMA[0] and RMA[0] correspond to D0 and are the least significant bits.

Writing the RAMDAC Color RAM

The MPU writes the address register (WMA) with the address of the RAMDAC color RAM location to be modified. Using RS[1:0] to select the RAMDAC color RAM (LUT), the MPU completes three continuous write cycles (6 or 8 bits each of red, green, and blue). Following the blue write cycle, the 3 bytes of color information are concatenated into an 18- or 24-bit word and written to the location specified by the address register. The address register advances to the next location which the MPU can modify by simply writing another sequence of red, green, and blue data. A block of color values in successive locations can be written to by writing the start address and performing continuous R, G, and B write cycles until the entire block has been written.

Reading the RAMDAC Color RAM

The MPU loads the address register (RMA) with the address of the RAMDAC color RAM location to be read. The contents of the RAMDAC color RAM at the specified address are copied into the RGB register, and the address register advances to the next RAM location. Using RS[1:0] to select the RAMDAC color RAM (LUT), the MPU completes three continuous read cycles (6 or 8 bits each of red, green, and blue).

Functional Description (continued)

After the blue read cycle, the contents of the RAMDAC color RAM at the address specified by the address register are copied into the RGB registers, and the address register advances to the next address. A block of color values in successive locations can be read by writing the start address and performing continuous R, G, and B read cycles until the entire block has been read.

Additional Information

Following a blue read or write cycle to color RAM location 0xFF, the address register resets to 0x00.

Operation of the MPU interface occurs asynchronously to the pixel clock. Internal logic synchronizes data transfers between the RAMDAC color RAM and the R, G, and B color subregister. The transfers occur between MPU accesses. As a result, the $\overline{WR}$ and $\overline{RD}$ signals must maintain a logic high for several clock cycles. See the ac timing characteristics under $\overline{RD}$ and $\overline{WR}$ high time for further information (see CR0[0]). To eliminate sparkling on the CRT screen during MPU access to the RAMDAC RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between look-up table RAMs and the RGB registers occurs.

To monitor the red, green, and blue read/write cycles, the address register has two additional bits (ADa, ADb) that count modulo three, as shown in Table 20. They are reset to 0 when the MPU writes to the address register (WMA or RMA), and they are not reset to 0 when the MPU reads the address register. The MPU does not have access to these bits.

The WMA and RMA address registers increment following a blue read or write cycle, and they are accessible to the MPU and are used to address RAMDAC RAM locations (LUT). The MPU can read the address register at any time without modifying its contents or the existing read/write mode. Note that the pixel clock must be active for MPU accesses to the RAMDAC RAM (LUT).

Table 20. Modulo Counter Operation

AD[b:a]	Addressed by MPU
00	Red color RAM byte
01	Green color RAM byte
10	Blue color RAM byte

$\overline{SENSE}$ Output

$\overline{SENSE}$ is a logic 0 if one or more of the red, green, or blue outputs have exceeded the internal voltage reference level of 340 mV. This output is used to determine the presence of a CRT monitor, and, via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The 340 mV reference has a ±70 mV tolerance.

DAC Gain

The device gain from the voltage reference to the DAC output current is shown below. To set the full-scale white current on the DACs while using an internal or external voltage reference, use the formula below.

V_{REF} is the voltage reference in volts, and K is the gain constant. RSET is the resistor connected between the RSET pin and ground.

$$I_{OUT}\ (mA) = \frac{(V_{REF}\ (V) \times 1000 \times K)}{RSET\ (\Omega)}$$

In this case, a voltage reference of 1.235 V with RSET = 147 Ω and a K factor of 3.17 results in I_{OUT} = 26.63 mA. A 6-bit DAC with no blank results in a K factor of 2.1 and I_{OUT} = 17.64 mA.

The recommended RSET for RS-343A compatibility applications (doubly terminated 75 Ω) is 147 Ω. The recommended RSET for *PS/2** applications (50 Ω) is 182 Ω.

* *PS/2* is a registered trademark of International Business Machines Corporation.

Table 21. Gain Factor (K) and I_{OUT} Current

SYNC	BLANK	K (8-Bit)	K (6-Bit)
Yes	Yes	3.195	3.17
Yes	No	3.17	3.0
No	Yes	2.28	2.26
No	No	2.12	2.1

Functional Description (continued)

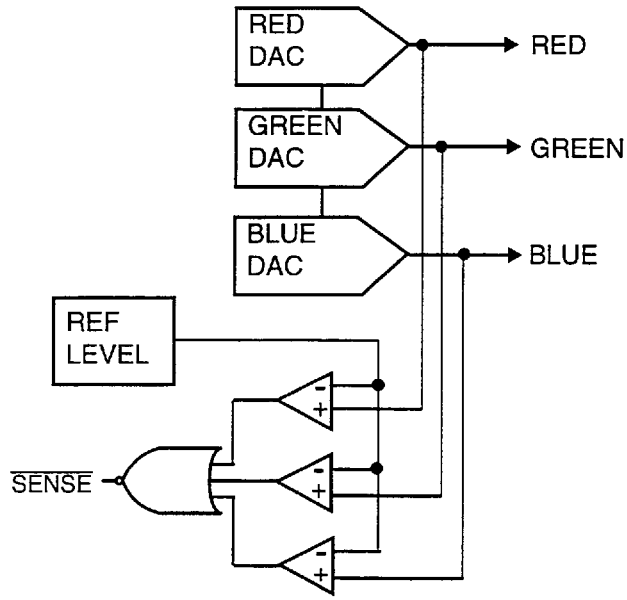


Figure 9. DAC Output Comparison Circuitry

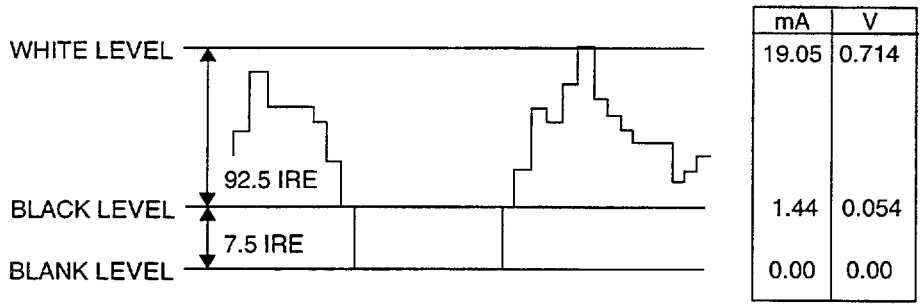


Figure 10. RS-343A Composite Video Output Waveforms

Table 22. RS-343A Video Output Truth Table (Blank Offset Current to Equal 7.5 IRE)

DAC Input Data	$\overline{\text{BLANK}}$	Output Level	I_{OUT} (mA)
$FF	1	White	19.05
data	1	DATA	data + 1.44
$00	1	BLACK	1.44
$XX	0	$\overline{\text{BLANK}}$	0

Note: 75 Ω doubly terminated load, SETUP = 7.5 IRE. V_{REF} = internal, RSET = 147 Ω.

Functional Description (continued)

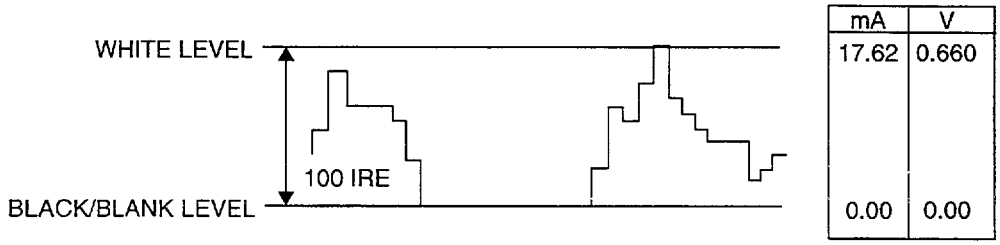


Figure 11. RS-343A Video Output Waveforms (No Blank Pedestal)

Table 23. RS-343A Video Output Truth Table (No Blank Offset Current)

DAC Input Data	$\overline{\text{BLANK}}$	Output Level	IOUT (mA)
$FF	1	White	17.62
data	1	DATA	data
$00	1	BLACK	0
$XX	0	$\overline{\text{BLANK}}$	0

Note: 75 Ω doubly terminated load, SETUP = 0 IRE. VREF = internal, RSET = 147 Ω.

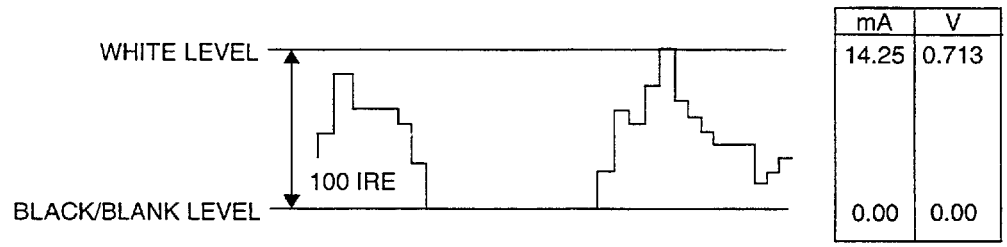


Figure 12. *PS/2* Composite Video Output Waveforms

Table 24. *PS/2* Video Output Truth Table (No Blank Offset Current)

DAC Input Data	$\overline{\text{BLANK}}$	Output Level	IOUT (mA)
$FF	1	White	14.25
data	1	DATA	data
$00	1	BLACK	0
$XX	0	$\overline{\text{BLANK}}$	0

Note: 75 Ω doubly terminated load, SETUP = 0 IRE. VREF = internal, RSET = 182 Ω.

Application Information

Board Layout

Careful configuration and placement of supply planes, components, and signal traces ensure a low-noise board. This also helps ensure proper functionality and low signal emissions in restricted frequency bands as mandated by regulatory agencies.

A four-layer PC board with separate power and ground planes will likely result in a board with quieter signals and supplies.

The ATT20C408 should be placed close to the video output connector and between the video output connector and the edge card connector. (See Figure 13.) This will keep the high-speed DAC output traces short and minimize the amount of circuitry between the RAMDAC and the supply pins on the edge card connector.

Power Distribution

Separate the power plane into digital and analog areas as illustrated in Figures 13, 16, 17, and 18. Place all digital components over the digital plane and all analog components over the analog plane. The analog components include the RAMDAC, reference circuitry, comparators, mixed-signal chips, and any passive support components for analog circuits.

The analog and digital power plane should be connected with at least one ferrite bead across the separation as illustrated in Figure 13. This bead provides resistance to high-frequency currents. Select a ferrite bead with an impedance curve suitable for your design. The ferrite should have a resistance at a higher frequency than the maximum signal frequency on the board, but lower than the second harmonic (2x) of that frequency. The following beads provide resistances of approximately 75 Ω at 100 MHz: Ferroxcube VK20019-4B, Fair-Rite 2743001111, or Philips 431202036690. The power and ground traces or vias to the RAMDAC should be at least 50 mil wide. This is especially important on the ATT20C408 because the device has only two Vcc pins.

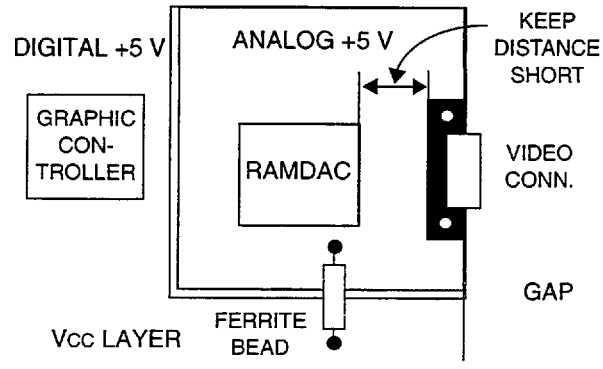


Figure 13. Digital and Analog Supply Plane Split

Decoupling Capacitors

All decoupling capacitors should be located within 0.25 in. of the device to be decoupled. Chip capacitors are recommended, but radial and axial leads will work. Keep lead lengths as short as possible to reduce inductance and EMI. For leaded capacitors, use devices with a self-resonance above the pixel clock frequency.

For the ATT20C408, decouple Vcc pin to ground with a 0.1 µF capacitor. For higher-frequency pixel clocks (>110 MHz), use a 0.01 µF capacitor in parallel with the 0.1 µF capacitor to shunt the higher-frequency noise to ground. Power supply noise should be less than 200 mV for a good design. About 10% of any noise below 1 MHz will be coupled onto the DAC outputs. As illustrated in Figure 15, the COMP pin should also be decoupled with a 0.1 µF capacitor. For designs showing ghosting or smearing, add a parallel COMP capacitance of 2.2 µF.

Application Information (continued)

Digital Signals

The digital inputs should not travel over the analog power plane if possible. The RAMDAC should be located over the analog plane close to the digital/ analog supply separation. The RAMDAC may also be placed over the supply separation so the digital pixel inputs are over the digital supply plane. The digital inputs, especially the P[15:0] high-speed inputs, should be isolated from the analog outputs. Placing the digital inputs over the digital supply reduces coupling into the analog supply plane. High-speed signals (both analog and digital) should not be routed under the RAMDAC.

Avoid high slew rate edges since they can contribute to undershoot, overshoot, ringing, EMI, and noise feedthrough. Edges can be slowed down by using series termination (33 Ω to 150 Ω). Edge noise will result if the digital signal propagates from an impedance mismatch while the signal arises. The reflection noise is particularly troublesome in the TTL threshold region. For a 2 ns edge, the trace length must be less than 4 in.

The clock signal trace should be as short as possible and should not run parallel to any high-speed signals. To ensure a quality clock signal without high-frequency noise components, decouple the supply pins on the clock driver. If necessary, transmission line techniques should be used on the clock by providing controlled-impedance striplines and parallel termination.

The 2x clock doubler in the ATT20C408 will help to reduce signal quality problems and EMI radiations by reducing the frequency of the clock signal to the device.

Analog Signals

The load resistor should be as close as possible to the DAC outputs. The resistor should equal the destination termination which is usually a 75 Ω monitor. Unused analog outputs should be connected to ground. The DAC output traces should be as short as possible to minimize any impedance mismatch in the trace or video connector.

Match the impedance of the R, G, and B traces with the termination (75 Ω). The width of the traces will be determined by the distance from the ground plane and the dielectric constant of the PC board material. Try to keep the R, G, and B traces at least 20 mil to 50 mil wide. Series ferrite beads can be added to the analog video signal to reduce high-frequency signals coupled onto the DAC outputs or reflected from the monitor.

To reduce the interaction of the analog video return current with board components, a separate video ground return trace can be added to the ground plane or signal layer. This trace connects directly to the ground of the edge card connector (see Figure 14). Using a separate video ground return path ensures that the RAMDAC ground is not corrupted with video return current.

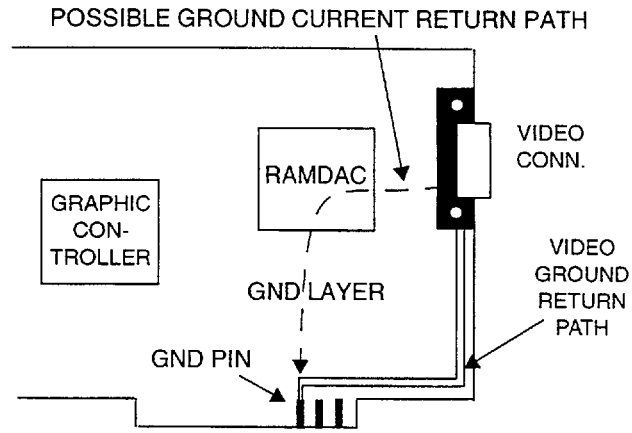


Figure 14. Video Ground Return Current Path

Clock Synthesizer

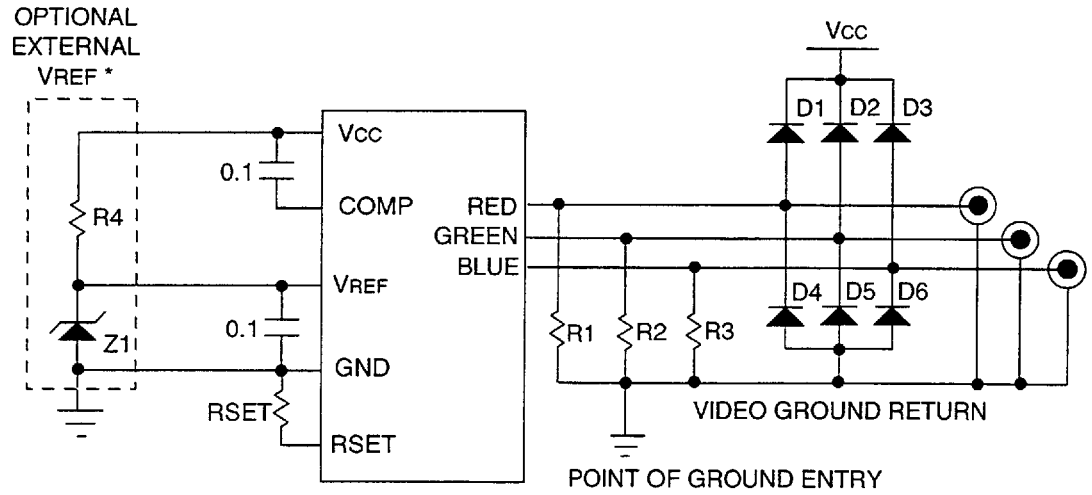
A quiet and clean voltage source for the ATT20C408 clock synthesizer must be provided. This will result in reduced or no clock jitter. A 15 µH inductor must be used on clock synthesizer power pin VccS (pin 3) to ensure optimum performance. (See Figures 16, 17, and 18 for power supply configuration and necessary filtering.)

DAC Outputs

The ATT20C408 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching ac-coupled monitors.

The diode protection circuit shown in Figure 16 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes.

Application Information (continued)



* Use of an external VREF for nonstandard operation will defeat the accuracy provided by the *PrecisionDAC* technology.

Figure 15. Internal and External Voltage Reference Typical Connection Diagram

See next page for Vcc connections.

Table 25. External and Internal Voltage Reference Parts List

Location	Description
R1—R3	75 Ω, 1% metal film resistor.
RSET	1% metal film resistor.
D1—D6	Fast-switching diodes.
Z1*	Voltage reference (1.2 V).
R4*	1 kΩ, 5% resistor.

* Optional for external VREF.

Application Information (continued)

Power Circuits

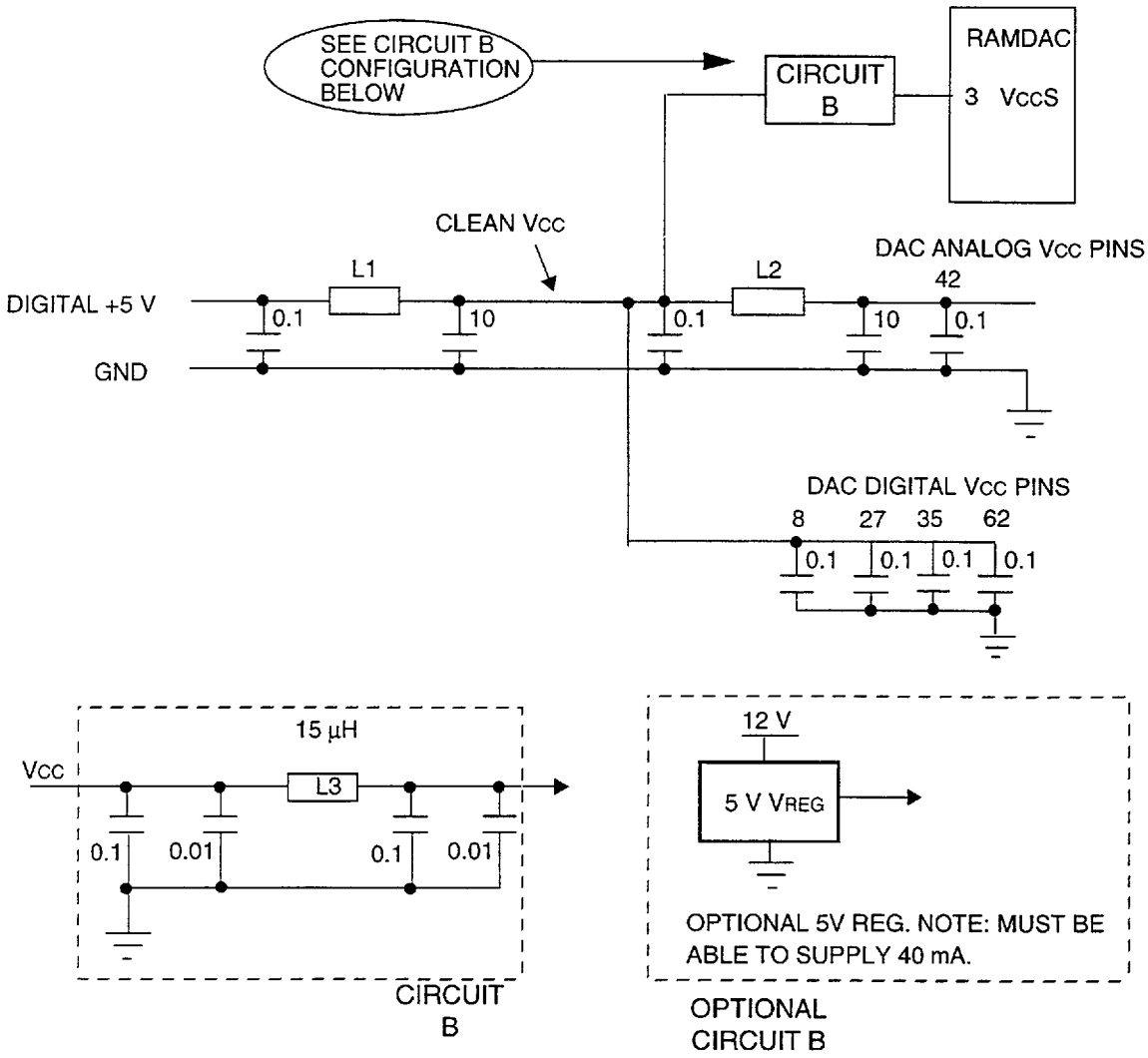


Figure 16. Split Power Supply

Figure 16 shows a connection diagram for a split supply to the chip showing the clock synthesizer pin and DAC digital and analog power pins.

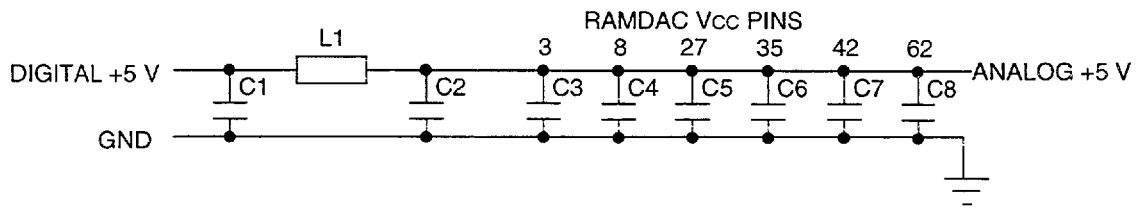


Figure 17. Optional Power Filtering Circuit for Combined Power Supply

Application Information (continued)

Pin Layout

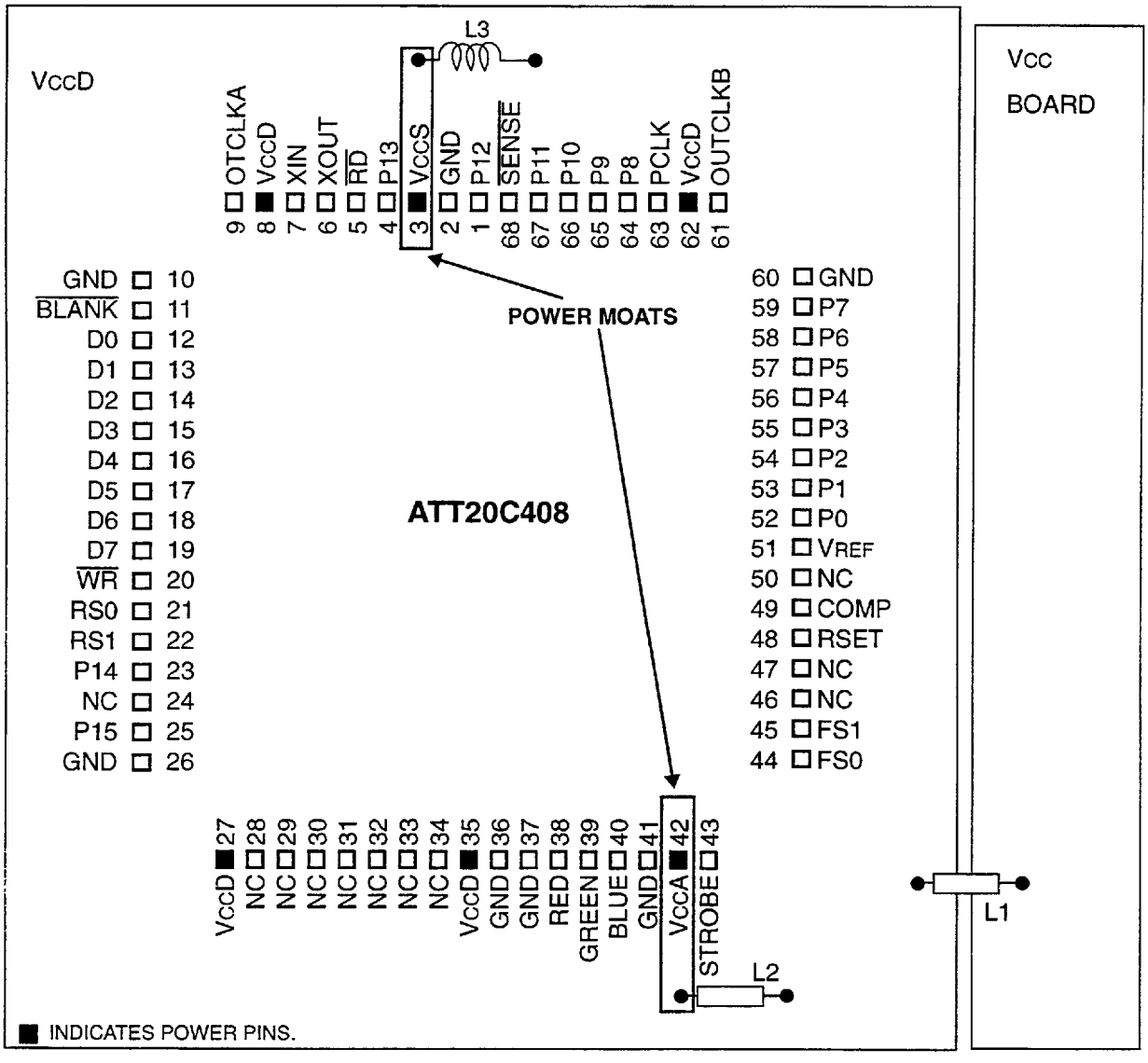


Figure 18. Physical Layout (Power Moats for VccD, VccS, and VccA)

Table 26. External and Internal Voltage Reference Parts List

Component Name	Description
—	0.1 µF ceramic capacitor.
—	10 µF capacitor.
L1, L2	Ferrite bead.
L3	15 µH inductor.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
Vcc (measured to GND)	—	—	—	7.0	V
Voltage on Any Digital Pin	—	GND – 0.5	—	Vcc + 0.5	V
Analog Output Short Circuit: Duration to Any Power Supply or Common	ISC	—	Indefinite	—	—
Ambient Operating Temperature	TA	–55	—	125	°C
Storage Temperature	Tstg	–65	—	150	°C
Junction Temperature	TJ	—	—	150	°C
Vapor Phase Soldering (60 s)	TVSOL	—	—	220	°C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	VCC	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0	—	70	°C
Output Load	RL	—	37.5	—	Ω
White Level Adjust Resistor	RSET	—	147	—	Ω
Reference Voltage (use internal VREF)	VREF	—	Internal	—	V
Crystal Input Frequencies (200 ppm*)	Fin	—	14.318	—	MHz
Crystal Loading	—	Parallel	Parallel	Parallel	—
Crystal Series Resistance	—	—	35	—	Ω

* Other crystal frequencies can be used. See control register bits CR1[6:5].

Electrical Characteristics

Table 27. dc Characteristics 1

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, internal VREF (trimmed for DAC current accuracy). The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

Parameter	Symbol	Min	Typ	Max	Unit
Digital Inputs: (including XIN and XOUT)					
Input Voltage:					
Low	V_{IL}	GND – 0.5	—	0.8	V
High	V_{IH}	2.0	—	V_{CC} + 0.5	V
Input Current:					
Low (V_{IN} = 0.4 V)	I_{IL}	—	—	–1	µA
High (V_{IN} = 2.4 V)	I_{IH}	—	—	1	µA
Capacitance (f = 1 MHz, V_{IN} = 2.4 V)	Cin	—	—	7	pF
Digital Outputs (except OTCLKA or OTCLKB):					
Output Voltage:					
Low (I_{OL} = 4 mA)	V_{OL}	—	—	0.4	V
High (I_{OH} = –4 mA)	V_{OH}	2.4	—	—	V
OTCLKA or OTCLKB Output:					
Low (I_{OL} = 12 mA)	V_{OL}	—	—	0.4	V
High (I_{OH} = –12 mA)	V_{OH}	2.4	—	—	V
3-State Current	I_{OZ}	—	—	50	µA
Capacitance	C_{DOUT}	—	—	7	pF
Output Impedance, Active	Zout	—	—	100	Ω
Output Impedance, Inactive (3-state)	Zoff	10K	—	—	Ω

Electrical Characteristics (continued)

Table 28. dc Characteristics 2

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, internal VREF (trimmed for DAC current accuracy). The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

Parameter	Symbol	Min	Typ	Max	Unit
Resolution (each DAC):	—	8	8	8	bits
Accuracy (each DAC):					
Integral Linearity Error	IL	—	—	±1	LSB
Differential Linearity Error	DL	—	—	±1	LSB
Gain Error	—	—	±3	±5	%
Monotonicity	—	—	Guaranteed	—	Scale
Coding	—	—	—	—	Binary
Analog Outputs:					
Gray Scale Current Range	Igray	—	—	20	mA
Output Current:					
White Level Relative to Black	Iwb	16.74	17.62	18.50	mA
Black Level Relative to Blank:	Ibb				
With Pedestal	—	0.95	1.44	1.90	mA
Without Pedestal	—	0	5	50	µA
Blank Level	Iblank	0	5	50	µA
LSB Size	Ilsb	—	69.9	—	
DAC to DAC Matching	—	—	2	5	%
Output Compliance	VOC	–0.5	—	1.5	V
Output Impedance	RAOUT	—	10	—	kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT	—	—	30	pF
Internal Reference Output (trimmed for DAC current accuracy)	VREF	—	1.235	—	V
SENSE Trip Level	VSEN	270	340	410	mV
Power Supply Rejection Ratio	PSRR	—	—	0.5	%/% change in Vcc
COMP = 0.1 µF, f = 1 kHz	—	—	—	–6	dB

Electrical Characteristics (continued)

Table 29. ac Characteristics

The recommended operation condition for generating test signals is RSET = 147 Ω, internal VREF (trimmed for DAC current accuracy). TTL level input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤10 pF, $\overline{\text{SENSE}}$, D[7:0] output load ≤50 pF. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

		170 MHz Devices			135 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Internal 2x Clock Rate (reference only):	fmax	—	—	170	—	—	135	MHz
PCLK Rate, 2x Clock Enabled	f2x	0	—	85	0	—	67.5	MHz
PCLK Rate, 2x Clock Disable*	fmax	—	—	110	—	—	110	MHz
PCLK Cycle Time	1	9.09	—	—	9.09	—	—	ns
PCLK Duty Cycle, Digital Doubler	—	45	50	55	45	50	55	%
PCLK Duty Cycle, Analog Doubler	—	30	50	70	30	50	70	%
DAC Performance:								
Analog Output Delay	3	—	—	30	—	—	30	ns
Analog Output Rise/Fall Time	4	—	3	—	—	3	—	ns
Analog Output Setting Time	—	—	13	—	—	13	—	ns
Clock and Data Feedthrough*	—	—	–30	—	—	–30	—	dB
Glitch Energy	—	—	75	—	—	75	—	pV-s
SENSE Output Delay	—	—	1	—	—	1	—	µs
DAC to DAC Crosstalk	—	—	–23	—	—	–23	—	dB
Analog Output Skew	—	—	—	2	—	—	2	ns
Pixel and Control Timing:								
P[15:0], $\overline{\text{BLANK}}$ Setup	5	2.0	—	—	2.0	—	—	ns
P[15:0], $\overline{\text{BLANK}}$ Hold	6	2.0	—	—	2.0	—	—	ns
Supply Current and Pipeline Delay:								
Pipeline Delay:†	Pipe							
VCC Supply Current‡	ICC	—	275	365	—	240	320	mA
Sleep Current (PCLK = 35 MHz)§	ISIP	—	5	—	—	5	—	mA

* Clock and data feedthrough are functions of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74 HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough. –3 dB test bandwidth = 2x clock rate.

† Pipeline delay is fixed for each mode (see Table 18 for pipeline delay for each mode).

‡ At fmax, ICC (typ) at VCC = 5 V; ICC (max) at VCC (max).

§ External voltage reference is automatically disabled during powerdown. Test conditions: 25 °C to 70 °C. Pixel and data ports at 0.4 V.

Electrical Characteristics (continued)

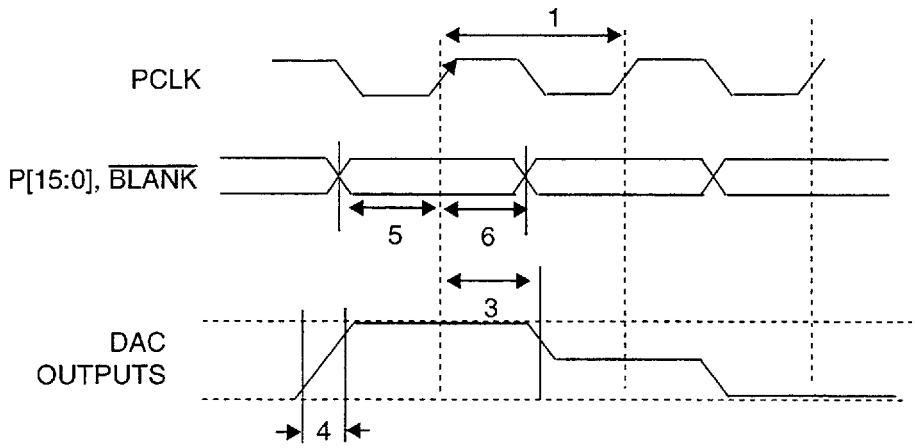


Figure 19. Pixel Input and Video Output Timing

Timing Characteristics

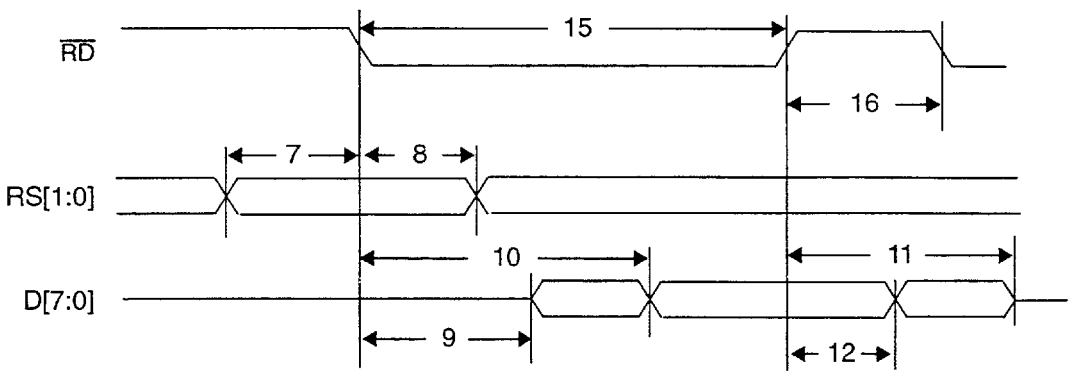


Figure 20. Basic Read-Cycle Timing

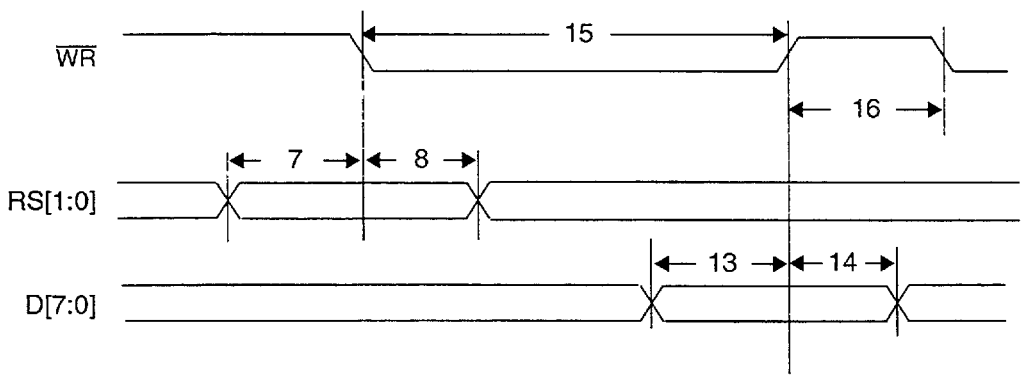


Figure 21. Basic Write-Cycle Timing

Timing Characteristics (continued)

Table 30. ac Characteristics

TTL level input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

		170 MHz and 135 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Microprocessor Port:					
RS[1:0] Setup Time	7	10	—	—	ns
RS[1:0] Hold Time	8	10	—	—	ns
$\overline{RD}$ Asserted to D[7:0] Driven	9	5	—	—	ns
$\overline{RD}$ Asserted to D[7:0] Valid	10	—	—	40	ns
$\overline{RD}$ Negated to D[7:0] 3-Stated	11	—	—	20	ns
Read D[7:0] Hold Time	12	5	—	—	ns
Write D[7:0] Setup Time	13	10	—	—	ns
Write D[7:0] Hold Time	14	10	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	15	50	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	16	3	—	—	PCLK

Clock Synthesizer Characteristics

TTL level input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Digital output load ≤15 pF. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table. Crystal or reference frequency = 14.318 MHz; OTCLKA or OTCLKB loading ≤15 pF.

Parameter	Symbol	Min	Typ	Max	Unit
Maximum Synthesizer Frequency for OTCLKA or OTCLKB (external)	Fmax	—	—	85	MHz
Duty Cycle OTCLKA or OTCLKB	ODC	45	—	55	%
FREF and XIN, XOUT Input Duty Cycle	IDC	45	—	55	%
OTCLKA or OTCLKB Phase Jitter (6 Sigma)	17	—	500	—	ps
OTCLKA or OTCLKB Duty Cycle Jitter (6 Sigma)	18	—	500	—	ps
STROBE Pulse Width High or Low	19	20	—	—	ns
FS[1:0] to STROBE Setup Time	20	2	—	—	ns
FS[1:0] to STROBE Hold Time	21	—	—	4	ns
Frequency Select* to OTCLKA or OTCLKB Unstable	22	—	—	0	ns
Frequency Select* to OTCLKA or OTCLKB Stable	23	—	1	10	ms
Power Up to OTCLKA or OTCLKB Stable	—	—	—	10	ms
OTCLKA or OTCLKB Rise or Fall Time	Tr/Tf	—	—	3	ns

* Frequency select can refer to the FS[1:0] pins or to the control register bits CC[5:4] or CC[1:0].

Notes:
Output pnase and duty cycle jitter excludes the reference clock or crystal oscillator jitter.
Rise time and fall time measured from 10% to 90% points using 0 V and 3 V levels.

Clock Synthesizer Characteristics (continued)

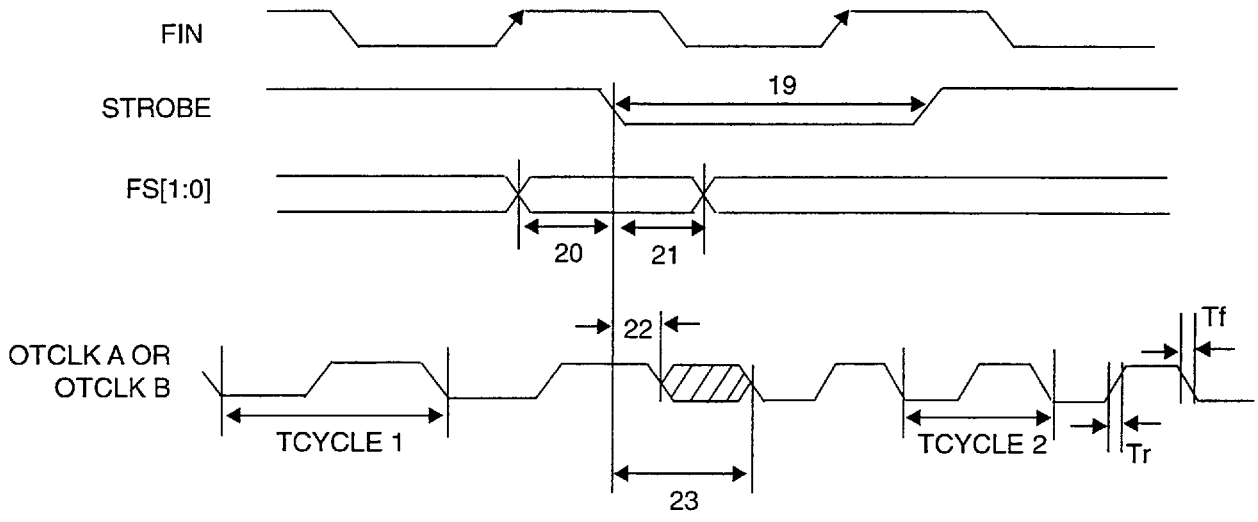


Figure 22. Clock Synthesizer (OTCLKA or OTCLKB) Timing

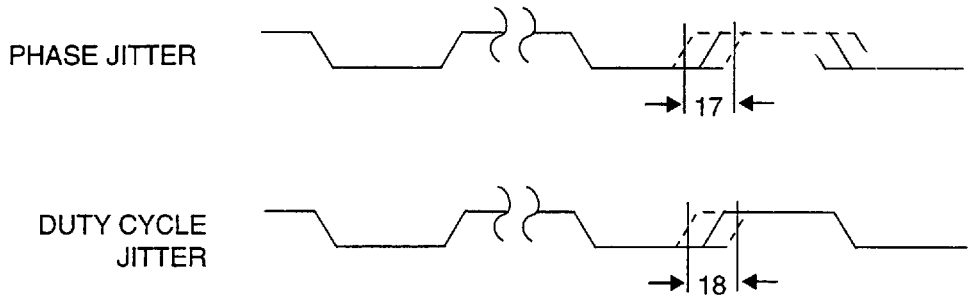
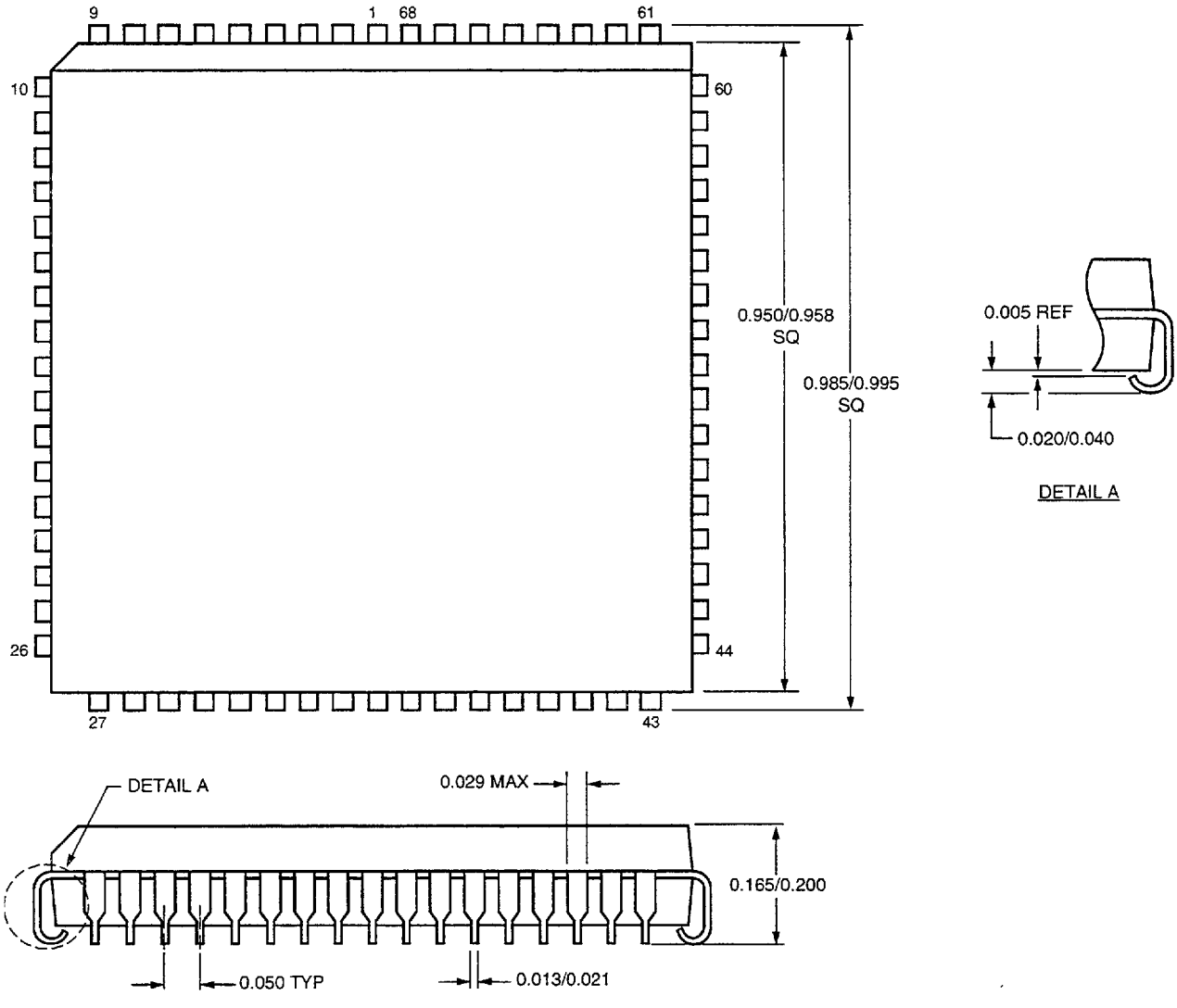


Figure 23. Clock Synthesizer Waveform Specifications (OTCLKA or OTCLKB)

Outline Diagram

68-Pin PLCC Package

Dimensions are in inches.



Appendix A—Register Summary for ATT20C408

The purpose of this section is to briefly show the internal registers and the control they have on the RAMDAC functions.

Address Registers

Address Register — Write (WMA)							
7	6	5	4	3	2	1	0
Write Mode Address							

Address Register 1 (Write function)
Read/Write, RS[1:0] = 00, Not Reset
7:0 Address to write pixel color RAM

Address Register — Read (RMA)							
7	6	5	4	3	2	1	0
Read Mode Address							

Address Register 1 (Read function)
Read/Write, RS[1:0] = 11, Not Reset
7:0 Address to read pixel color RAM

Control Registers

Control Register 0 (CR0)

Control Register 0 (CR0)							
7	6	5	4	3	2	1	0
Color Mode				PD	Reserved	8/6	Ext. Acc.

Read/Write, RS[1:0] = 10, Index (WMA) = $01, Reset = $00

7:4 Color Mode
0000 8-bit pseudo
0001 15-bit + C
0010 2X 8-bit pseudo
0011 16-bit 5/6/5
0100 8-bit in two clocks
0101 24-bit on 16 pins, two clocks
0110 16-bit 5/6/5 on 8 pins in two clocks
0111 24-bit on 8 pins in three clocks
1000 Reserved
1001 Reserved
1010 Reserved
1011 Reserved
1100 Reserved
1101 Reserved
1110 2x 24-bit on 16 pins in three clocks
1111 Reserved
3 Power Down (1)
2 Reserved
1 8-bit (1) or 6-bit (0) Select
0 Extended register access (1)

Control Register 1 (CR1)

Control Register 1 (CR1)							
7	6	5	4	3	2	1	0
Osc Dis	PLL Freq Range Sel		Blank En	ClkA PD	ClkB PD	Sense Dis	Reserved

Read/Write, RS[1:0] = 10, Index (WMA) = $05, Reset = $00

7 Disable crystal oscillator (1)
6:5 Frequency range select
00 Digital Multiplier
01 Enable PLL, input > 40 MHz
10 Enable PLL, 20 > input > 40 MHz
11 Enable PLL, 10 > input > 20 MHz
4 Blank pedestal enable (1)
3 OTCLKA powerdown (1)
2 OTCLKB powerdown (1)
1 SENSE disable (1)
0 Reserved

Clock Control Register 0 (CC0)

Clock Control Register 0 (CC0)							
7	6	5	4	3	2	1	0
ClkA Contr	Reserved	Clock A Freq Select		ClkB Contr	Reserved	Clock B Freq. Select	

Read/Write, RS[1:0] = 10, Index (WMA) = $06, Reset = $00

7 Bits CC0[5:4] (1), input pins FS[1:0] (0), control clock A
6 Reserved
5:4 Register set select for clock A
00 25.175
01 28.332
10 Register set C (after reset = 50 MHz)
11 Register set D (after reset = 75 MHz)
3 Bits CC0[1:0] (1), input pins FS[1:0] (0), control clock B
2 Reserved
1:0 Register set select for clock B
00 30 MHz
01 40 MHz
10 Register set C (after reset = 50 MHz)
11 Register set D (after reset = 60 MHz)

Appendix A—Register Summary for ATT20C408 (continued)

RMR, Test, and ID Registers

Read Mask Register

Read Mask Register (RMR)							
7	6	5	4	3	2	1	0
8-Bit Read Mask Value							

Read/Write, RS[1:0] = 10, Index (WMA) = $00, or CR0[0] = 0, or use state machine, Not Reset

7:0 8-bit Read mask value

Manufacturer ID Register

MANUFACTURER ID REGISTER (MIR)							
7	6	5	4	3	2	1	0
1	0	0	0	0	1	0	0

Read Only, RS[1:0] = 10, Index (WMA) = $02

7:0 Value = $84

Device ID Register

Device ID Register (DIR)							
7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1

Read Only, RS[1:0] = 10, Index (WMA) = $03

7:0 Value = $09

Test Registers

Test Registers (TST)							
7	6	5	4	3	2	1	0
Red, Green, Blue Sequential 8-Bit Values							

Read/Write, RS[1:0] = 10, Index (WMA) = $04, Not Reset

7:0 Red, green, and blue values vary

Color RAM

Pixel Color RAM

Pixel Color RAM (LUT)							
7	6	5	4	3	2	1	0
8-Bit R, G, B Value, Autoincrementing							

Read/Write, RS[1:0] = 01, modulo three, direct read/write, autoincrementing, Not Reset

7:0 Red[7:0], Green[7:0], Blue[7:0] pixel color

Synthesizer Registers

Feedback Divider Term

Feedback Divider (M)							
7	6	5	4	3	2	1	0
8-Bit Feedback Divider Term							

Read/Write, RS[1:0] = 10, Index (WMA) = $48, $4C, $6C, Reset to values in table INDEXREG

7:0 8-bit divider term for the feedback circuit

Postscaler and Reference Divider

Postscaler and Reference Dividers (P,N)							
7	6	5	4	3	2	1	0
2-Bit P Value	6-Bit N Value						

Multiple registers some Read/Write and some Read Only. Reset to values in Table 5. RS[1:0] = 10, Index (WMA) = $49, $4D, $6D.

7:6 2-bit postscale divider
5:0 6-bit input reference divider

Loop Filter and Bias Control

Loop Filter Resistance and Bias Current							
7	6	5	4	3	2	1	0
Loop Filter Resistance, L				Bias Current, IB			

Multiple registers some Read/Write and some Read Only. Reset to values in Table 5. RS[1:0] = 10, Index (WMA) = $4A, $4E, $6E.

7:4 L, 4-Loop filter resistance control
3:0 IB, 4-bit bias control for charge pump

Ordering Information

Device	Speed (MHz)	Temperature
ATT20C408-17M68	170	0 °C to 70 °C
ATT20C408-13M68	135	0 °C to 70 °C

Note: Comcodes also indicate how the devices are packaged for shipment (i.e., tape and reel, dry pack, etc.).