NCP4894

1.8 Watt Differential Audio Power Amplifier with Selectable Shutdown

The NCP4894 is a differential audio power amplifier designed for portable communication device applications. This feature and the excellent audio characteristics of the NCP4894 are a guarantee of a high quality sound, for example, in mobile phones applications. With a 10% THD+N value the NCP4894 is capable of delivering 1.8 W of continuous average power to an 8.0 Ω load from a 5.5 V power supply. With the same load conditions and a 5.0 V battery voltage, it ensures 1.0 W to be delivered with less than 0.01% distortion.

The NCP4894 provides high quality audio while requiring few external components and minimal power consumption. It features a low−power consumption shutdown mode.

To be flexible, shutdown may be enabled by either a logic high or low depending on the voltage applied on the SD MODE pin.

The NCP4894 contains circuitry to prevent from “pop and click” noise that would otherwise occur during turn−on and turn−off transitions.

For maximum flexibility, the NCP4894 provides an externally controlled gain (with resistors), as well as an externally controlled turn−on time (with bypass capacitor).

Due to its excellent PSRR, it can be directly connected to the battery, saving the use of an LDO.

This device is available in 9−Pin Flip−Chip, Micro−10 and DFN10 3x3 mm packages.

Features

- Differential Amplification
- Shutdown High or Low Selectivity
- 1.0 W to an 8.0 Ω Load from a 5.0 V Power Supply
- Superior PSRR: Direct Connection to the Battery
- “Pop and Click” Noise Protection Circuit
- Ultra Low Current Shutdown Mode
- 2.2 V−5.5 V Operation
- External Gain Configuration Capability
- External Turn−on Configuration Capability
- Thermal Overload Protection Circuitry
- Pb−Free Packages are Available

Typical Applications

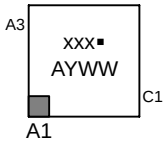
- Portable Electronic Devices
- PDAs
- Mobile Phones

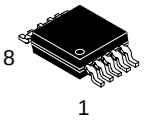
ON Semiconductor®

http://onsemi.com

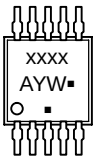
MARKING DIAGRAMS

9−PIN FLIP−CHIP
FC SUFFIX
CASE 499AL

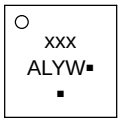




Micro−10
DM SUFFIX
CASE 846B



DFN10
MN SUFFIX
CASE 485C



xxxx = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W, WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

© Semiconductor Components Industries, LLC, 2005

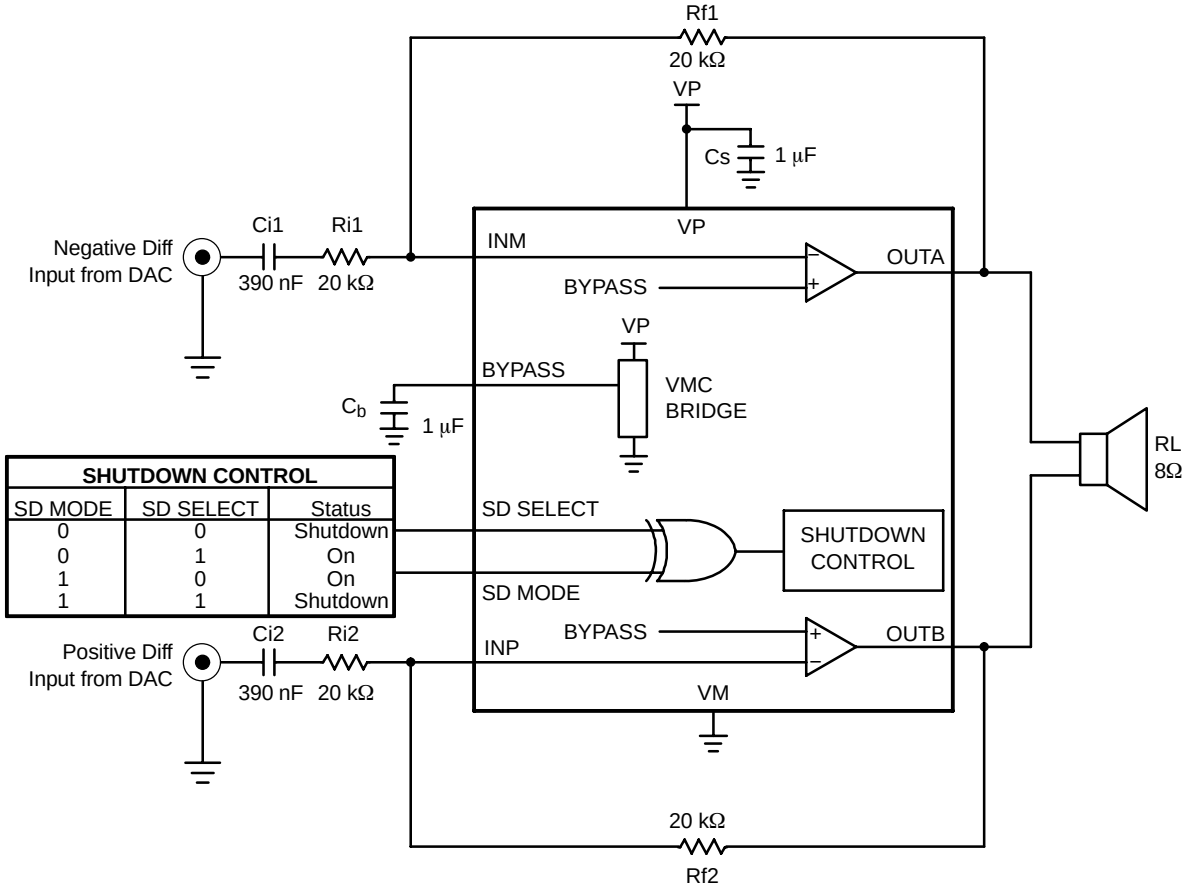
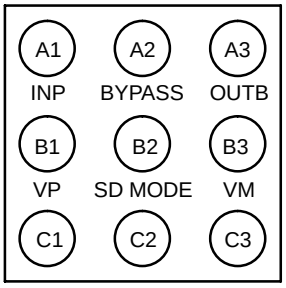


Figure 1. Typical NCP4894 Application Circuit with Differential Input

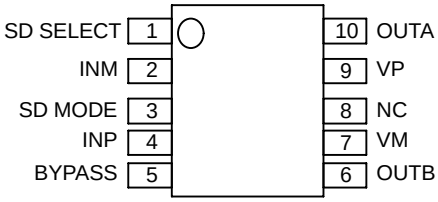
PIN CONNECTIONS

9−Pin Flip−Chip



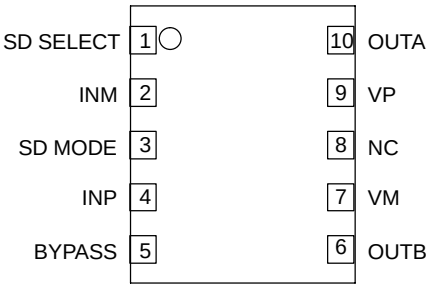
(Top View)

Micro−10



(Top View)

DFN10



(Top View)

PIN DESCRIPTION

9−Pin Flip−Chip	Micro−10/DFN10	Type	Symbol	Description
A1	4	I	INP	Positive Differential Input
A2	5	O	BYPASS	Bypass Capacitor Pin which Provides the Common Mode Voltage
A3	6	I	OUTB	Negative BTL Output
B1	9	I	VP	Positive Analog Supply of the Cell
B2	3	I	SD MODE	Shutdown High or Low Selectivity (Note 1)
B3	7	I	VM	Ground
C1	2	I	INM	Negative Differential Input
C2	1	O	SD SELECT	(Note 1)
C3	10	I	OUTA	Positive BTL Output

1. The SD SELECT pin must be toggled to the same state as the SD MODE pin to force the device in shutdown mode.

MAXIMUM RATINGS (Note 2)

Rating	Symbol	Value	Unit
Supply Voltage	VP	6.0	V
Operating Supply Voltage	Op VP	2.2 to 5.5 V	−
Input Voltage	V_{in}	−0.3 to Vcc +0.3	V
Max Output Current	Iout	500	mA
Power Dissipation (Note 3)	Pd	Internally Limited	−
Operating Ambient Temperature	T_A	−40 to +85	°C
Max Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Thermal Resistance Junction−to−Air Micro−10 DFN 3x3 mm 9−Pin Flip−Chip	$R_{\theta JA}$	200 70 (Note 4)	°C/W
ESD Protection Human Body Model (HBM) (Note 5) Machine Model (MM) (Note 6)	−	> 2000 > 200	V
Latchup Current at T_A = 85°C (Note 7)	−	±100 mA	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

2. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = +25°C.
3. The thermal shutdown set to 160°C (typical) avoids irreversible damage on the device due to power dissipation. For further information see page 6.
4. For the 9−Pin Flip−Chip CSP package, the $R_{\theta JA}$ is highly dependent of the PCB Heatsink area. For example, $R_{\theta JA}$ can equal 195°C/W with 50 mm^2 total area and also 135°C/W with 500 mm^2. For further information see page 10. The bumps have the same thermal resistance and all need to be connected to optimize the power dissipation.
5. Human Body Model, 100 pF discharge through a 1.5 kΩ resistor following specification JESD22/A114.
6. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.
7. Maximum ratings per JEDEC standard JESD78.

ELECTRICAL CHARACTERISTICS Limits apply for T_A between −40°C to +85°C (Unless otherwise noted).

Characteristic	Symbol	Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Supply Quiescent Current	I_{dd}	VP = 3.0 V, No Load VP = 5.0 V, No Load	− −	1.9 2.1	− −	mA
		VP = 3.0 V, 8.0 Ω VP = 5.0 V, 8.0 Ω	− −	2.0 2.2	− 4.0	
Common Mode Voltage	V_{cm}	−	−	VP/2	−	V
Shutdown Current	I_{SD}	For VP between 2.2 V to 5.5 V SDM = SDS = GND T_A = 25°C T_A = −40°C to +85°C	 − −	 20 −	 600 2.0	 nA μA
SD SELECT Threshold High	V_{SDIH}	−	1.4	−	−	V
SD SELECT Threshold Low	V_{SDIL}	−	−	−	0.4	V
Turning On Time (Note 10)	T_{WU}	C_{by} = 1.0 μF	−	140	−	ms
Turning Off Time (Note 10)	T_{SD}	−	−	20	−	ms
Output Swing	$V_{loadpeak}$	VP = 3.0 V, R_L = 8.0 Ω	−	2.5	−	V
		VP = 5.0 V, R_L = 8.0 Ω (Note 9) T_A = 25°C T_A = −40°C to +85°C	 4.0 3.85	 4.3 −	 − −	V
Rms Output Power	P_O	VP = 3.0 V, R_L = 8.0 Ω THD + N < 0.1% VP = 3.3 V, R_L = 8.0 Ω THD + N < 0.1% VP = 5.0 V, R_L = 8.0 Ω THD + N < 0.1%	− − −	0.39 0.48 1.08	− − −	W
Output Offset Voltage	V_{OS}	For VP between 2.2 V to 5.5 V	−30	1.0	30	mV
Power Supply Rejection Ratio	PSRR V+	G = 2.0, R_L = 8.0 Ω VP_{ripple_pp} = 200 mV C_{by} = 1.0 μF Input Terminated with 10 Ω F = 217 Hz VP = 5.0 V VP = 3.0 V F = 1.0 kHz VP = 5.0 V VP = 3.0 V	 − − − −	 −80 −80 −85 −85	 − − − −	dB
Efficiency	η	VP = 3.0 V, P_{orms} = 380 mW VP = 5.0 V, P_{orms} = 1.0 W	− −	64 63	− −	%
Thermal Shutdown Temperature	T_{sd}		−	160	−	°C
Total Harmonic Distortion	THD	VP = 3.0 V, F = 1.0 kHz R_L = 8.0 Ω, A_V = 2.0 P_O = 0.32 W VP = 5.0 V, F = 1.0 kHz R_L = 8.0 Ω, A_V = 2.0 P_O = 1.0 W	− − − − − −	− 0.007 − − 0.006 −	− − − − − −	%

8. Min/Max limits are guaranteed by design, test or statistical analysis.
9. This parameter is not tested in production for 9−Pin Flip−Chip CSP package in case of a 5.0 V power supply, however it is correlated based on a 3.0 V power supply testing.
10. See page 11 for a theoretical approach of these parameters.

TYPICAL PERFORMANCE CHARACTERISTICS

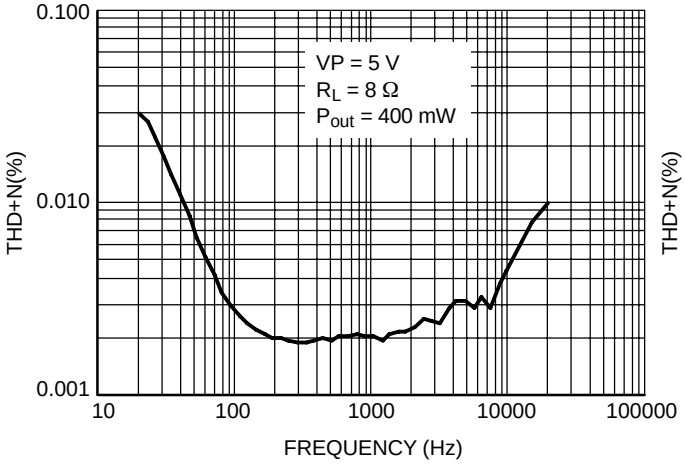


Figure 2. THDN versus Frequency

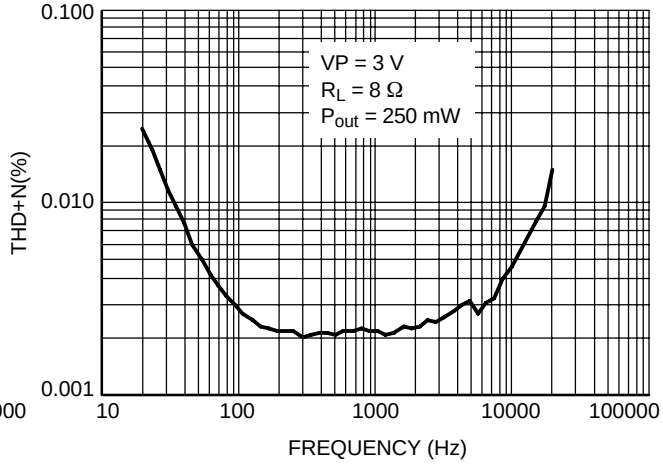


Figure 3. THDN versus Frequency

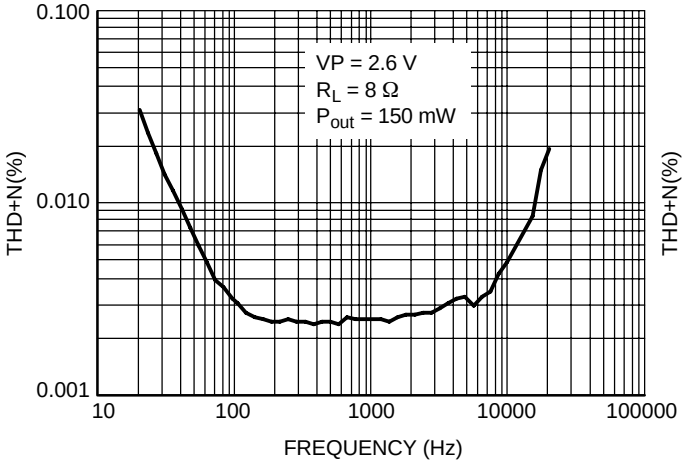


Figure 4. THDN versus Frequency

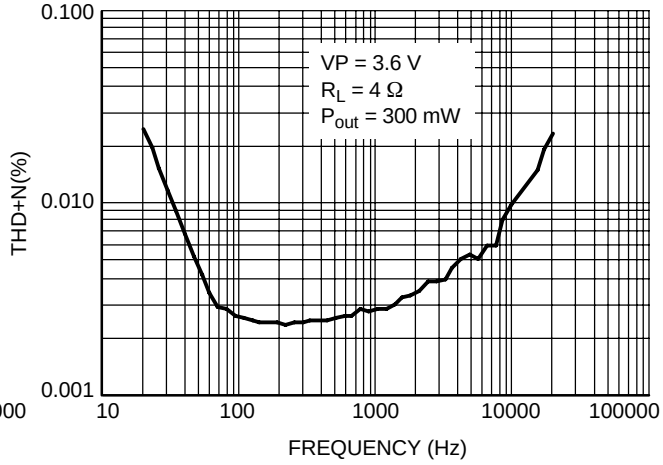


Figure 5. THDN versus Frequency

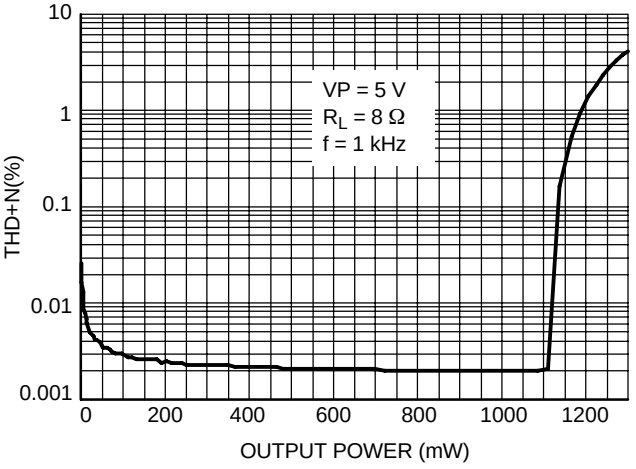


Figure 6. THDN versus Output Power

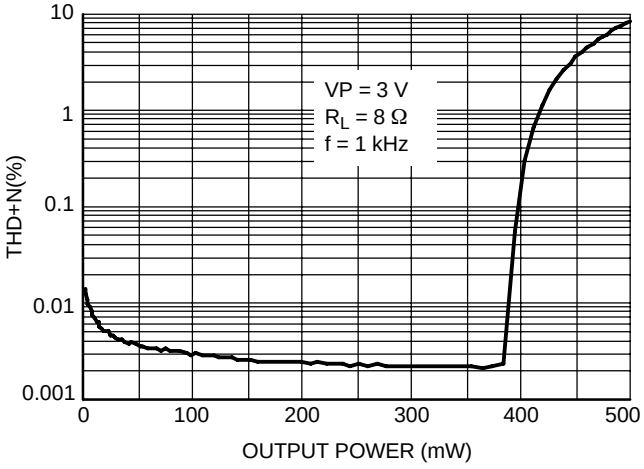


Figure 7. THDN versus Output Power

TYPICAL PERFORMANCE CHARACTERISTICS

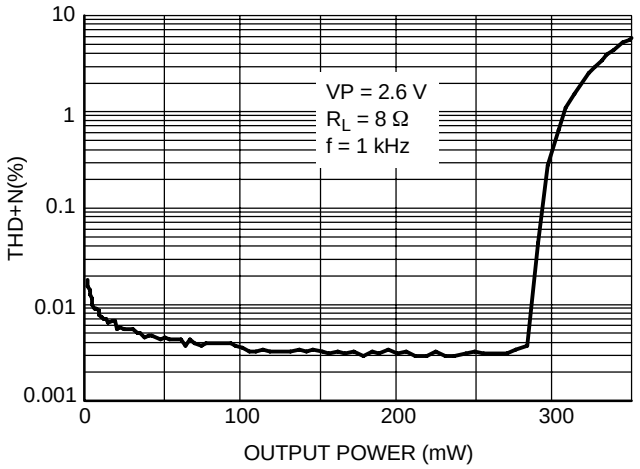


Figure 8. THDN versus Output Power

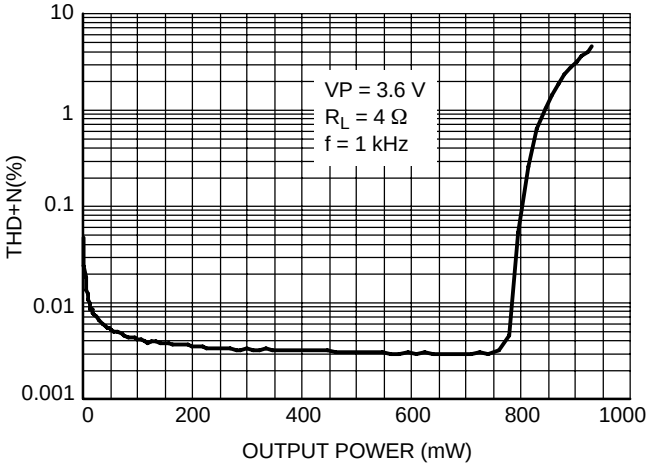


Figure 9. THDN versus Output Power

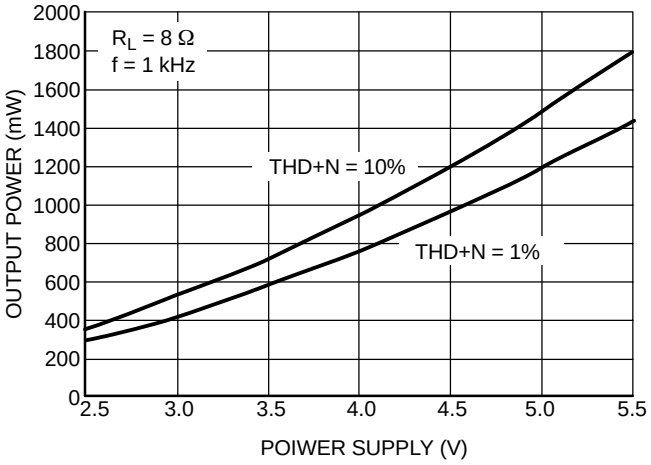


Figure 10. THDN versus Output Power

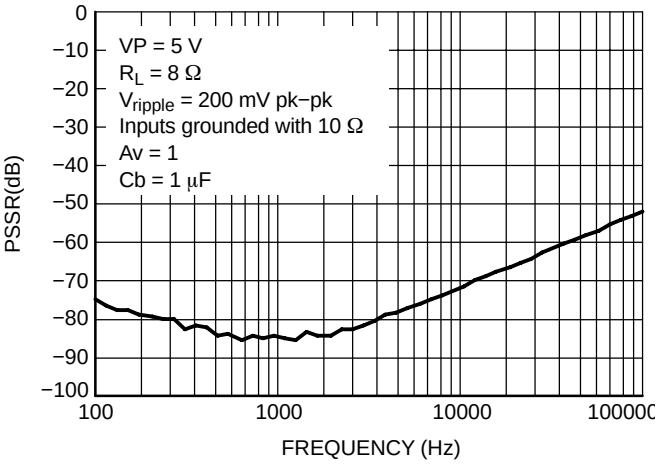


Figure 11. PSRR @ VP = 5 V

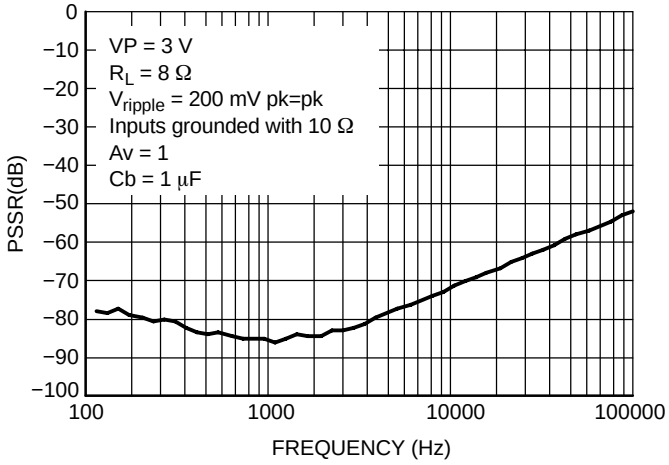


Figure 12. PSRR @ VP = 3 V

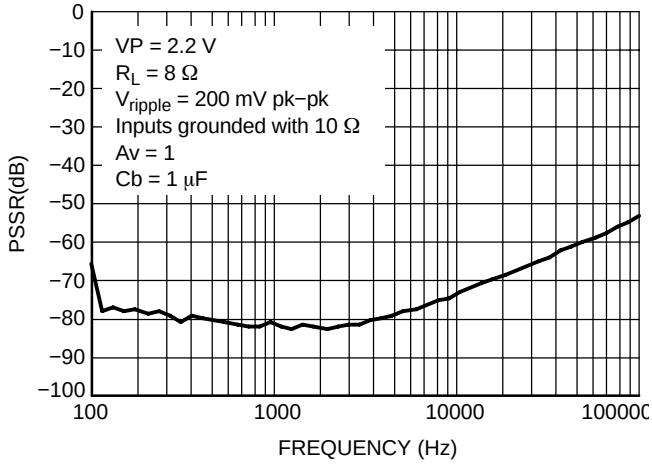


Figure 13. PSRR @ VP = 2.2 V

TYPICAL PERFORMANCE CHARACTERISTICS

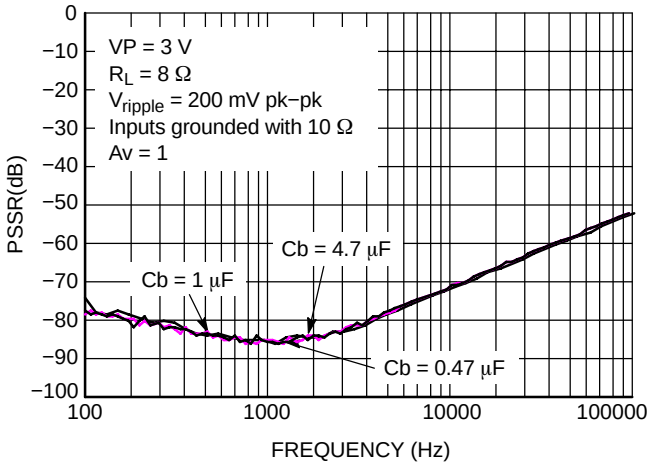


Figure 19. PSRR versus Cb @ VP = 3 V

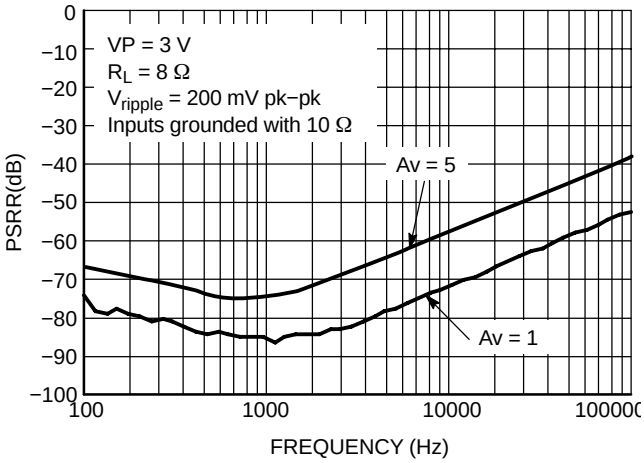


Figure 14. PSRR versus Av @ VP = 3 V

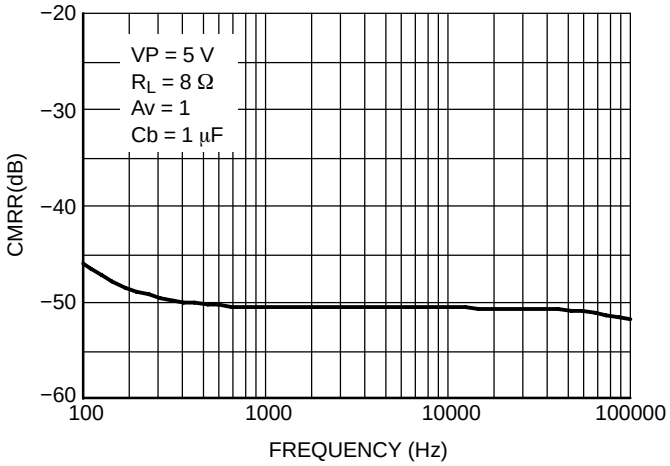


Figure 15. CMRR @ VP = 5 V

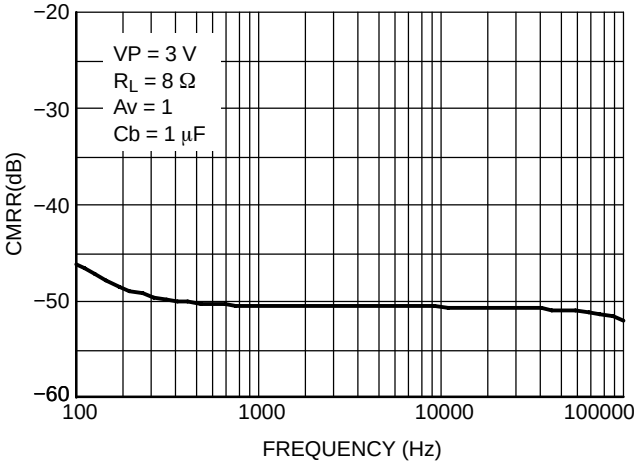


Figure 16. CMRR @ VP = 3 V

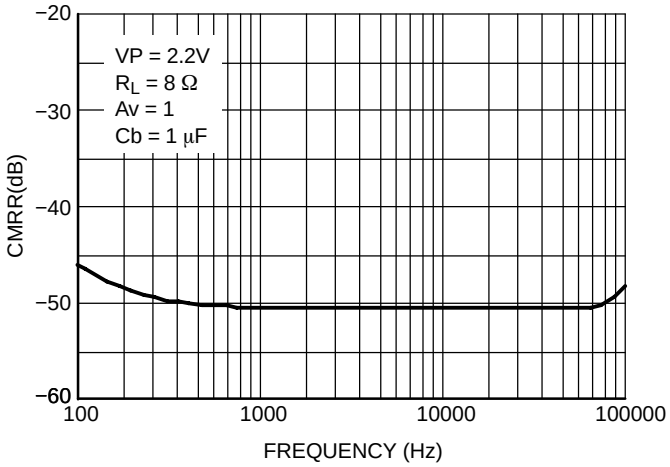


Figure 17. CMMR @ VP = 2.2 V

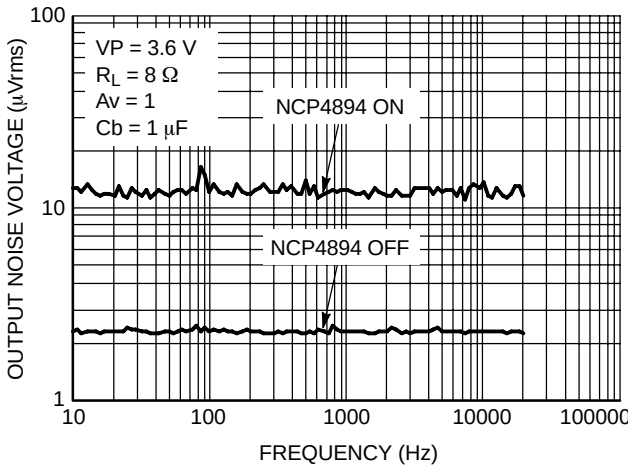
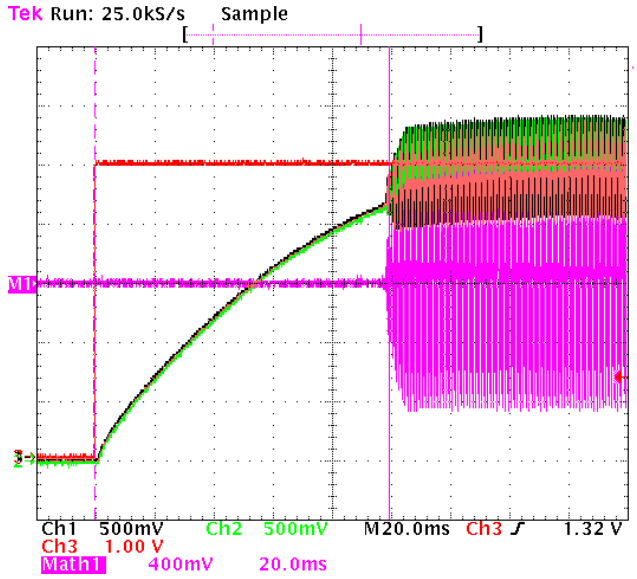


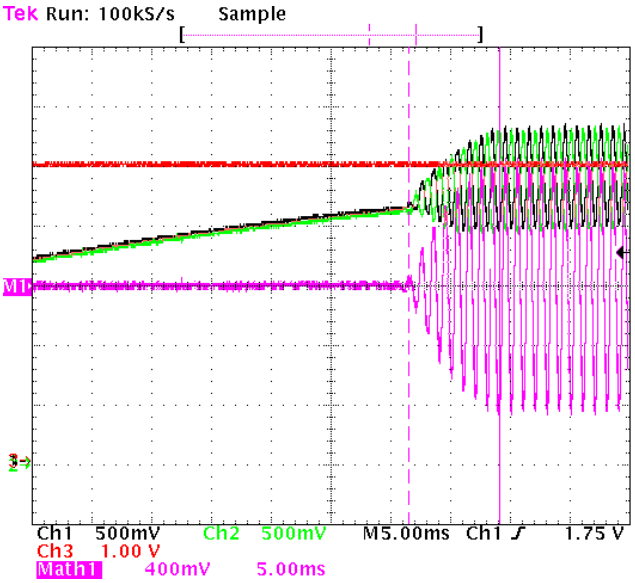
Figure 18. Noise Floor @ VP = 3.6 V

TYPICAL PERFORMANCE CHARACTERISTICS



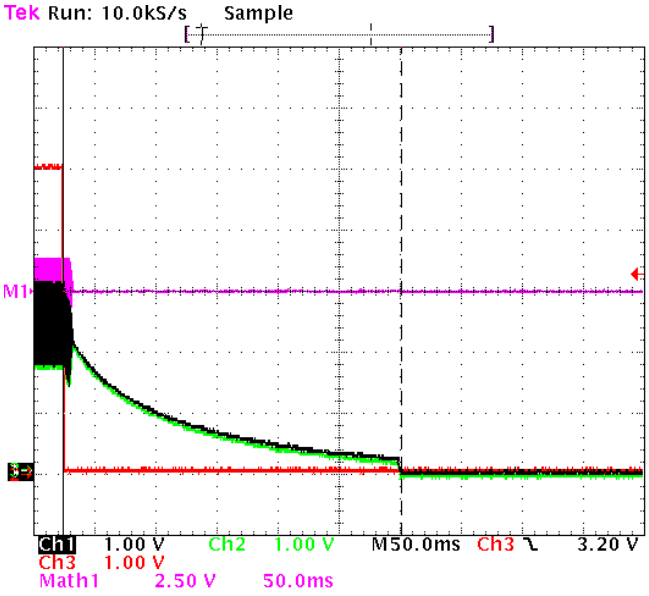
Ch1 = OUTA
Ch2 = OUTB
Ch3 = Shutdown &
Math1 = OUTA−OUTB

Figure 20. Turning−on Sequence @ VP = 5 V and f = 1 kHz



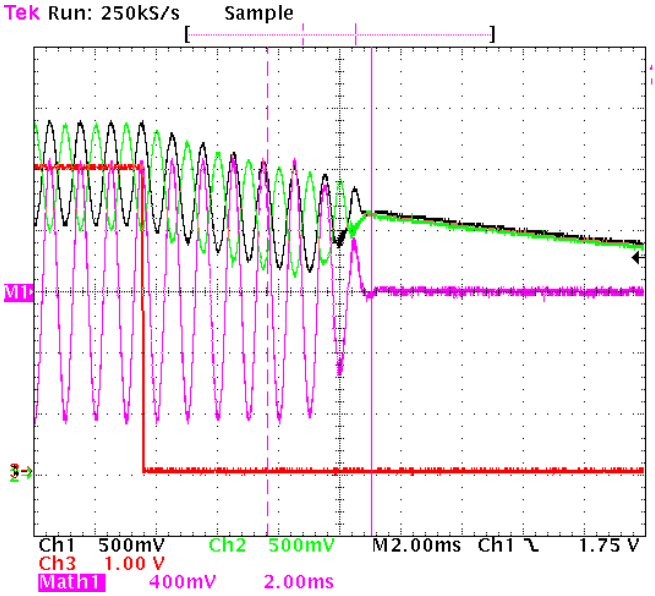
Ch1 = OUTA
Ch2 = OUTB
Ch3 = Shutdown &
Math1 = OUTA−OUTB

Figure 21. Turning−on Sequence Zoom @ VP = 5 V and f = 1 kHz



Ch1 = OUTA
Ch2 = OUTB
Ch3 = Shutdown &
Math1 = OUTA−OUTB

Figure 22. Turning−off Sequence @ VP = 5 V and f = 1 kHz



Ch1 = OUTA
Ch2 = OUTB
Ch3 = Shutdown &
Math1 = OUTA−OUTB

Figure 23. Turning−off Sequence Zoom @ VP = 5 V and f = 1 kHz

TYPICAL PERFORMANCE CHARACTERISTICS

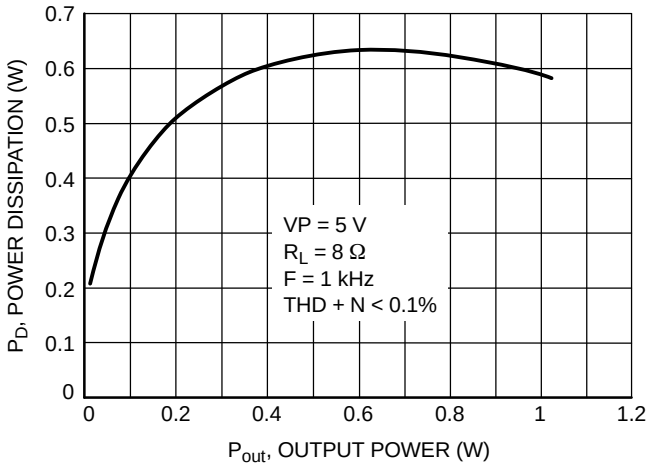


Figure 24. Power Dissipation versus Output Power

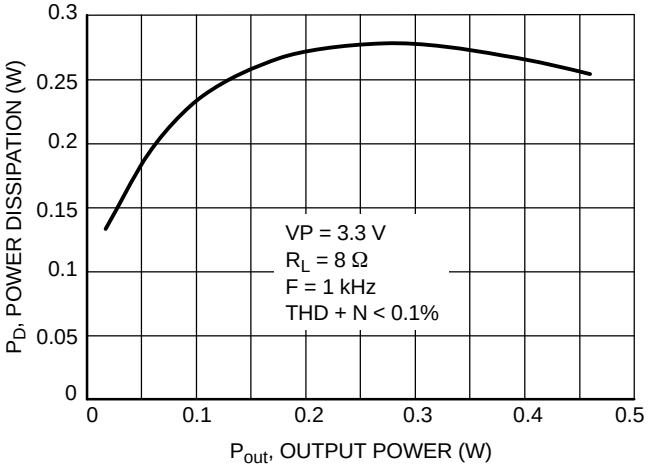


Figure 25. Power Dissipation versus Output Power

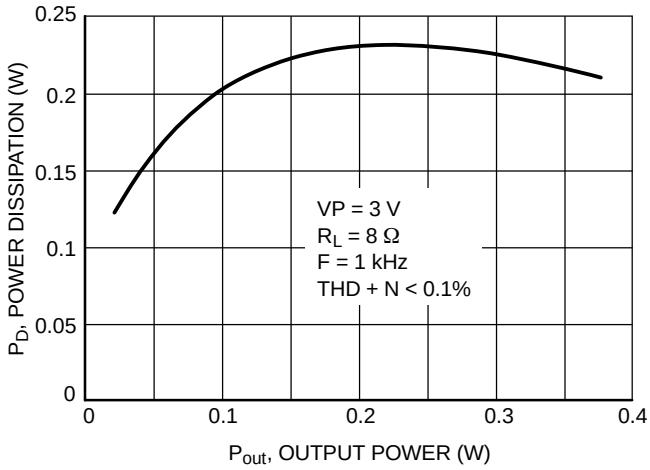


Figure 26. Power Dissipation versus Output Power

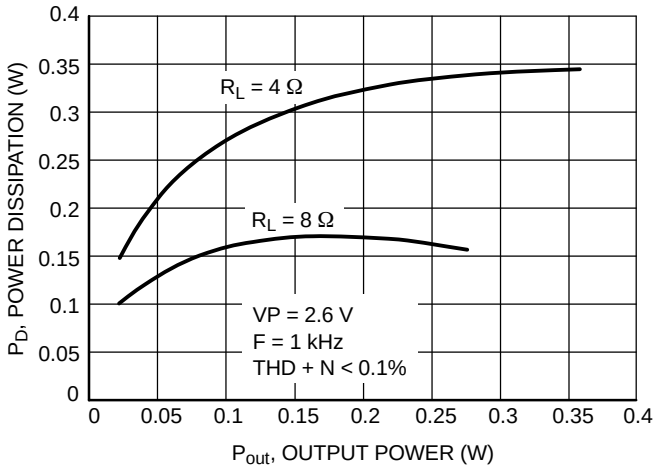


Figure 27. Power Dissipation versus Output Power

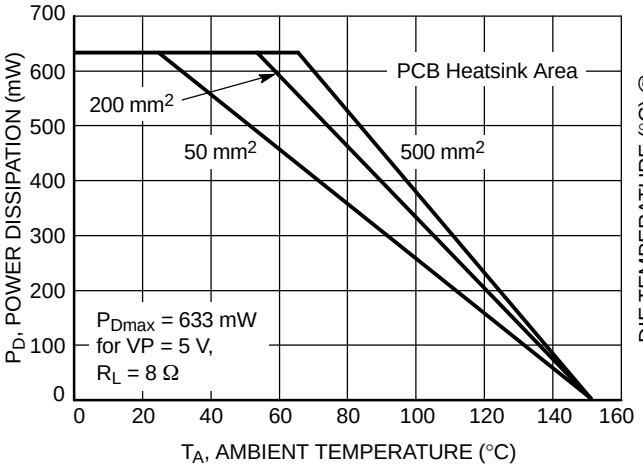


Figure 28. Power Derating − 9−Pin Flip−Chip CSP

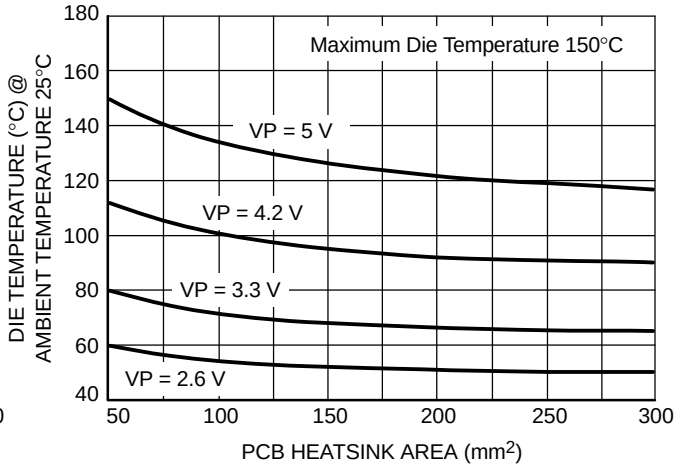


Figure 29. Maximum Die Temperature versus PCB Heatsink Area

APPLICATION INFORMATION

Detailed Description

The NCP4894 audio amplifier can operate under 2.6 V until 5.5 V power supply. It delivers 320 mW rms output power to 4.0 Ω load (VP = 2.6 V) and 1.0 W rms output power to 8.0 Ω load (VP = 5.0 V).

The structure of the NCP4894 is basically composed of two identical internal power amplifiers. Both are externally configurable with gain−setting resistors R_{in} and R_f (the closed−loop gain is fixed by the ratios of these resistors). The load is driven differentially through OUTA and OUTB outputs. This configuration eliminates the need for an output coupling capacitor.

Internal Power Amplifier

The output PMOS and NMOS transistors of the amplifier were designed to deliver the output power of the specifications without clipping. The channel resistance (R_{on}) of the NMOS and PMOS transistors does not exceed 0.6 Ω when they drive current.

The structure of the internal power amplifier is composed of three symmetrical gain stages, first and medium gain stages are transconductance gain stages to obtain maximum bandwidth and DC gain.

Turn−On and Turn−Off Transitions

A cycle with a turn−on and turn−off transition is illustrated with plots that show both single ended signals on the previous page.

In order to eliminate “pop and click” noises during transitions, output power in the load must be slowly established or cut. When logic high is applied to the shutdown pin, the bypass voltage begins to rise exponentially and once the output DC level is around the common mode voltage, the gain is established slowly (20 ms). Using this turn−on mode, the device is optimized in terms of rejection of “pop and click” noises.

A theoretical value of turn−on time at 25°C is given by the following formula.

C_{by}: bypass capacitor

R: internal 150 k resistor with a 25% accuracy

$T_{on} = 0.95 * R * C_{by}$

The device has the same behavior when it is turned−off by a logic low on the shutdown pin. During the shutdown mode, amplifier outputs are connected to the ground. However, to totally cut the output audio signal, you only need to wait for 20 ms.

Shutdown Function

The device enters shutdown mode once the SD SELECT and SD MODE pins are in the same logic state. This brings flexibility to the design, as the SD MODE pin must be permanently connected to VP or GND on the PCB. If the SD SELECT pin is not connected to the output of a microcontroller or microprocessor, it’s not advisable to let it float. A pulldown or pullup resistor is then suitable. During the shutdown state, the DC quiescent current has a typical value of 10 nA.

Current Limit Circuit

The maximum output power of the circuit (Porms = 1.0 W, VP = 5.0 V, R_L = 8.0 Ω) requires a peak current in the load of 500 mA.

In order to limit the excessive power dissipation in the load when a short−circuit occurs between both outputs, the current limit in the load is fixed to 800 mA.

Thermal Overload Protection

Internal amplifiers are switched off when the temperature exceeds 160°C, and will be switched on again only when the temperature decreases below 140°C.

The NCP4894 is unity−gain stable and requires no external components besides gain−setting resistors, an input coupling capacitor and a proper bypassing capacitor in the typical application.

Both internal amplifiers are externally configurable (R_f and R_{in}) with gain configuration.

The differential−ended amplifier presents two major advantages:

- The possible output power is four times larger (the output swing is doubled) as compared to a single−ended amplifier under the same conditions.
- Output pins (OUTA and OUTB) are biased at the same potential VP/2, this eliminates the need for an output coupling capacitor required with a single−ended amplifier configuration.

The differential closed loop−gain of the amplifier is given by $A_{vd} = *\frac{R_f}{R_{in}} = \frac{V_{orms}}{V_{inrms}}$. V_{orms} is the rms value of the voltage seen by the load and V_{inrms} is the rms value of the input differential signal.

Output power delivered to the load is given by $P_{orms} = \frac{(Vopeak)^2}{2 * R_L}$ (Vopeak is the peak differential output voltage).

When choosing gain configuration to obtain the desired output power, check that the amplifier is not current limited or clipped.

The maximum current which can be delivered to the load is 500 mA $I_{opeak} = \frac{V_{opeak}}{R_L}$.

Gain−Setting Resistor Selection (R_{in} and R_f)

R_{in} and R_f set the closed−loop gain of both amplifiers.

In order to optimize device and system performance, the NCP4894 should be used in low gain configurations.

The low gain configuration minimizes THD + noise values and maximizes the signal to noise ratio, and the amplifier can still be used without running into the bandwidth limitations.

A closed loop gain in the range from 2 to 5 is recommended to optimize overall system performance.

An input resistor (R_{in}) value of 22 kΩ is realistic in most applications, and doesn't require the use of a very large capacitor C_{in}.

Input Capacitor Selection (C_{in})

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. This capacitor creates a high−pass filter with Rin, the cut−off frequency is given by $fc = \frac{1}{2 * \Pi * R_{in} * C_{in}}$.

The size of the capacitor must be large enough to couple in low frequencies without severe attenuation. However a large input coupling capacitor requires more time to reach its quiescent DC voltage (VP/2) and can increase the turn−on pops.

An input capacitor value between 0.1 μ and 0.39 μF performs well in many applications (With R_{in} = 22 kΩ).

Bypass Capacitor Selection (Cby)

The bypass capacitor Cby provides half−supply filtering and determines how fast the NCP4894 turns on.

This capacitor is a critical component to minimize the turn−on pop. A 1.0 μF bypass capacitor value (C_{in} = < 0.39 μF) should produce clickless and popless shutdown transitions. The amplifier is still functional with a 0.1 μF capacitor value but is more susceptible to "pop and click" noises.

Thus, a 1.0 μF bypassing capacitor is recommended.

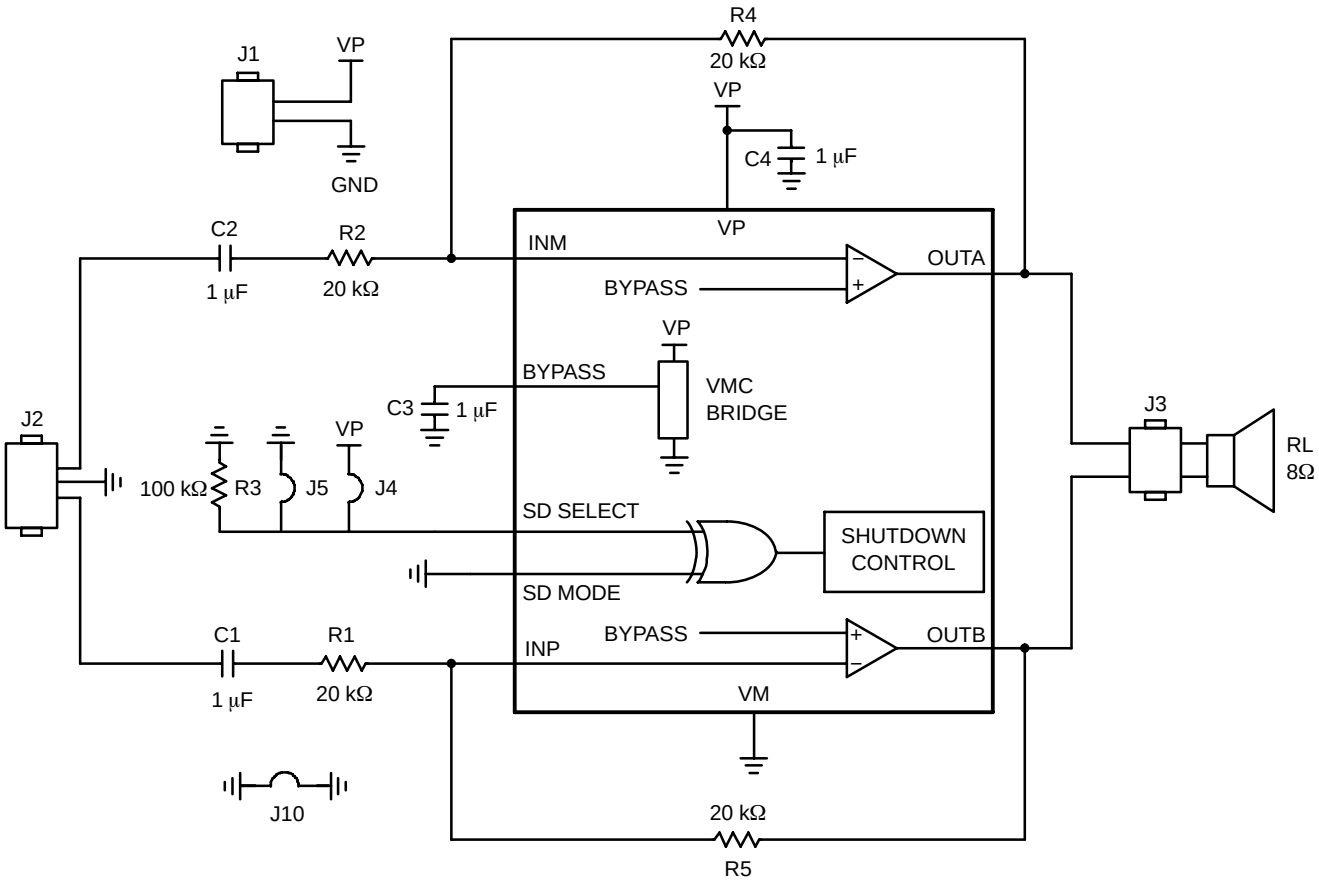
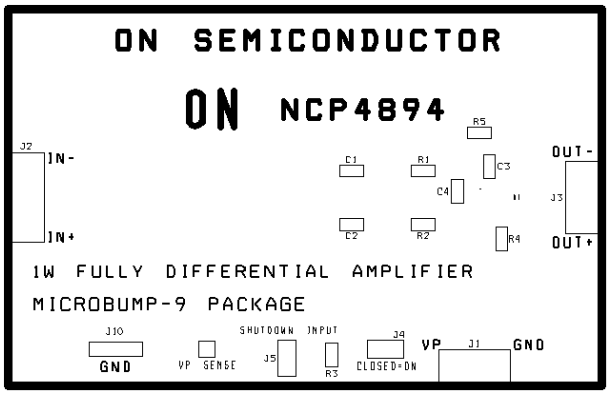
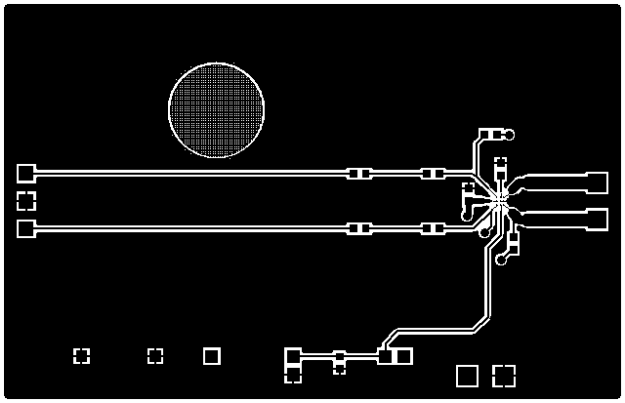


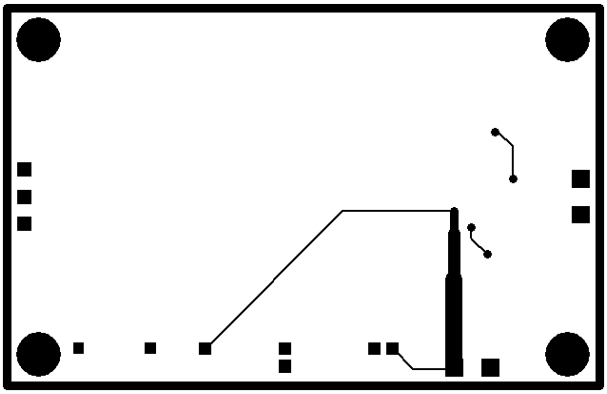
Figure 30. Demonstration Board Schematic



Silkscreen Layer



Top Layer



Bottom Layer

Figure 31. Demonstration Board for 9−Pin Flip−Chip CSP Device − PCB Layers

BILL OF MATERIAL

Item	Part Description	Ref	PCB Footprint	Manufacturer	Manufacturer Reference
1	NCP4894 Audio Amplifier	−	−	ON Semiconductor	NCP4894
2	SMD Resistor 100 kΩ	R3	0603	Vishay−Draloric	CRCW0603 Series
3	SMD Resistor 20 kΩ	R1, R2 R4, R5	0603	Vishay−Draloric	CRCW0603 Series
4	Ceramic Capacitor 1.0 μF 6.3 V X5R	C1, C2 C3, C4	0603	Murata	GRM188 Series
5	Jumper Header Vertical Mount, 2*1, 100 mils	J4, J5	−	−	−
6	Jumper Connector, 400 mils	J10	−	−	−
7	I/O Connector. It can be plugged by MC−1,5/3−ST−3,81 (Phoenix Contact Reference)	J2	−	Phoenix Contact	MC−1,5/3−G
8	I/O Connector. It can be plugged by BLZ5.08/2 (Weidmüller Reference)	J1, J3	−	Weidmüller	SL5.08/2/90B

ORDERING INFORMATION

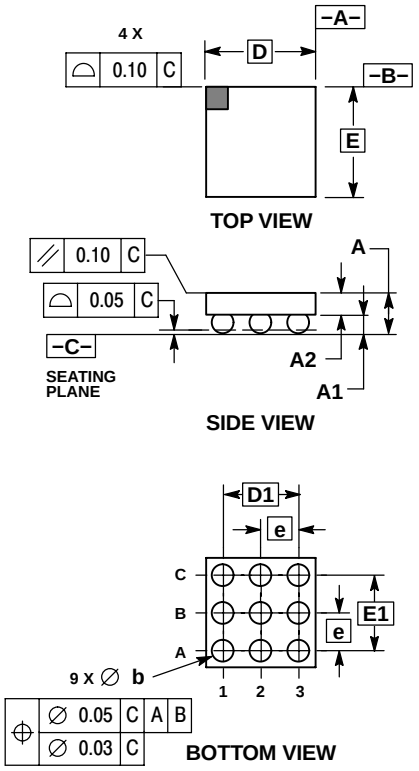
Device	Marking	Package	Shipping†
NCP4894FCT1	MAI	9−Pin Flip−Chip	3000 / Tape & Reel
NCP4894FCT1G	MAI	9−Pin Flip−Chip (Pb−Free)	3000 / Tape & Reel
NCP4894DMR2	MAK	Micro−10	4000 / Tape & Reel
NCP4894DMR2G	MAK	Micro−10 (Pb−Free)	4000 / Tape & Reel
NCP4894MNR2	4894	DFN10	3000 / Tape & Reel
NCP4894MNR2G	4894	DFN10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: This product is offered with either autectic (SnPb−tin/lead) or lead−free solder bumps (G suffix) depending on the PCB assembly process. The NCP4894FCT1G, NCP4894DMR2G, NCP4894MNR2G version requires a lead−free solder paste and should not be used with a SnPb solder paste.

PACKAGE DIMENSIONS

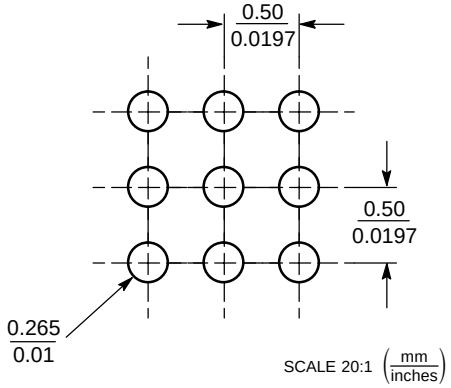
9−PIN FLIP−CHIP
FC SUFFIX
CASE 499AL−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.540	0.660
A1	0.210	0.270
A2	0.330	0.390
D	1.450 BSC	
E	1.450 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

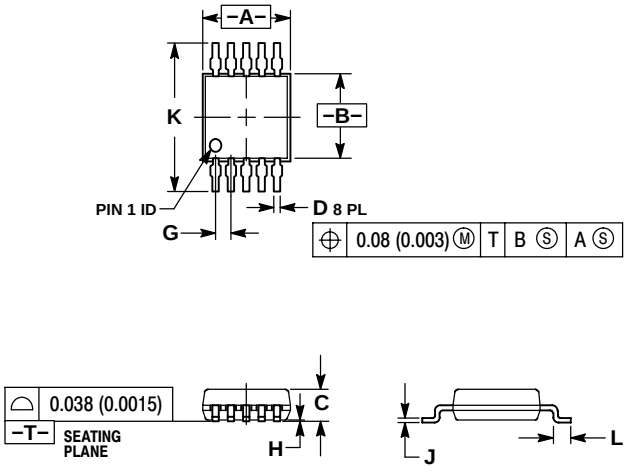
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

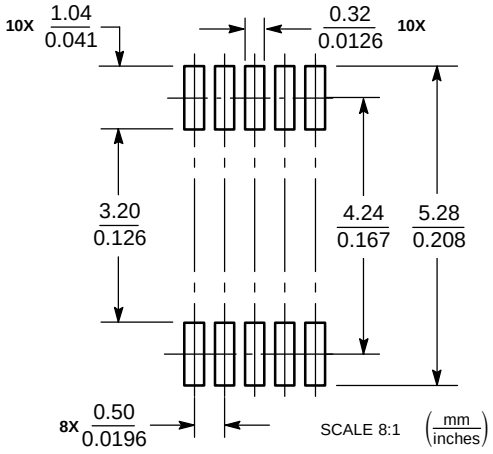
Micro−10
DM SUFFIX
CASE 846B−03
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION “A” DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION “B” DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846B−01 OBSOLETE. NEW STANDARD 846B−02

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.95	1.10	0.037	0.043
D	0.20	0.30	0.008	0.012
G	0.50 BSC		0.020 BSC	
H	0.05	0.15	0.002	0.006
J	0.10	0.21	0.004	0.008
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

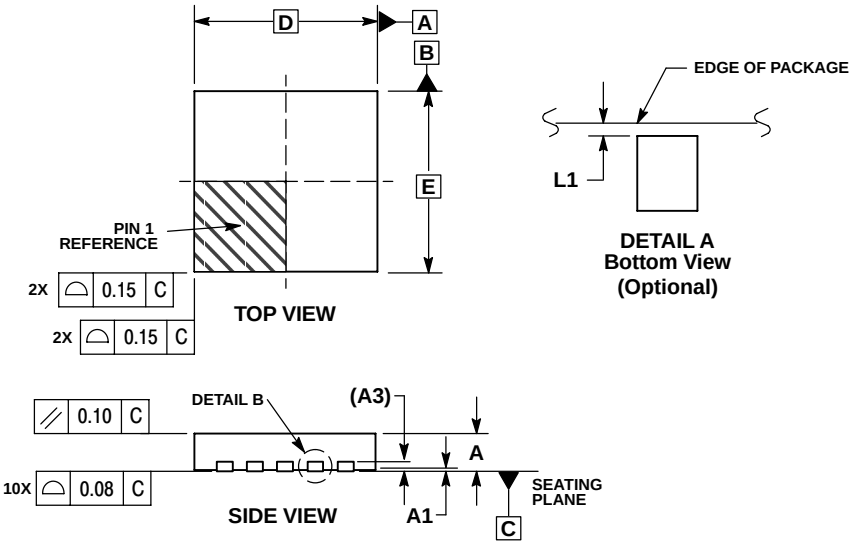
SOLDERING FOOTPRINT*

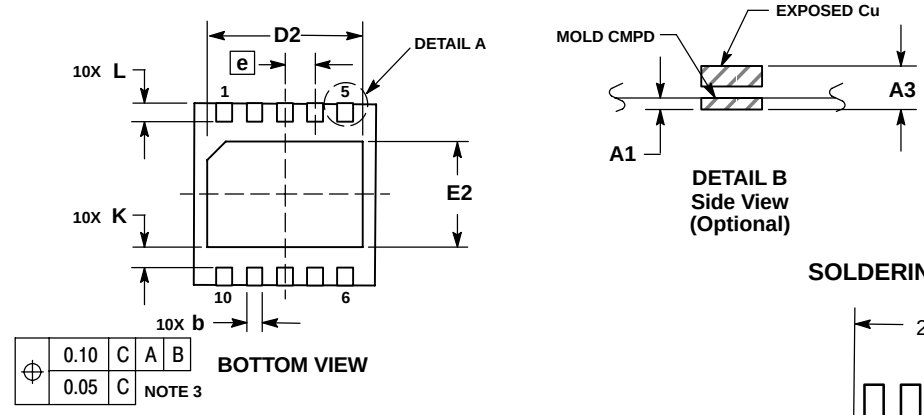


*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

DFN10
MN SUFFIX
CASE 485C−01
ISSUE A

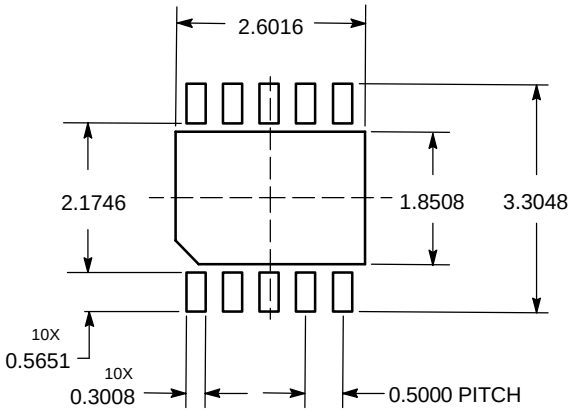




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASHING MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL b.
6. DETAILS A AND B SHOW OPTIONAL VIEWS FOR END OF TERMINAL LEAD AT EDGE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	2.45	2.55
E	3.00 BSC	
E2	1.75	1.85
e	0.50 BSC	
K	0.19 TYP	
L	0.35	0.45
L1	0.00	0.03

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.

NCP4894/D