# Nonvolatile DACPOT™ Electronic Potentiometer With Up/Down Counter Interface

## FEATURES

- **Digitally Controlled Electronic Potentiometer**

- **8-Bit Digital-to-Analog Converter (DAC)**
  - **Independent Reference Inputs**
  - **Differential Non-Linearity - $\pm$0.5LSB max**
  - **Integral Non-Linearity - $\pm$1LSB max**
- **$V_{OUT}$ Value in E$^2$PROM for Power-On Recall**
  - **Equivalent to 256-Step Potentiometer**
- **Unity Gain Op Amp Drives up to 1mA**

- **Simple Trimming Adjustment**
  - **Up/Down Counter Style Operation**
- **Low Noise Operation**

- **"Clickless" Transitions between DAC Steps**

- **No Mechanical Wearout Problem**
  - **1,000,000 Stores (typical)**
  - **100 Year Data Retention**

- **Operation from +2.7V to +5.5V Supply**

- **Low Power, 1mW max at +5V**

## OVERVIEW

The S9318 DACPOT™ trimmer is an 8-bit nonvolatile DAC designed to replace mechanical potentiometers. The S9318 includes a unity-gain amplifier to buffer the DAC output and enables $V_{OUT}$ to swing from rail to rail. The DACPOT trimmer operates over a supply voltage range of 2.7V to 5.5V.

The S9318's simple up/down counter input provides an ideal interface for automatic test equipment to dither and monitor the $V_{OUT}$ voltage. This interface allows for quick and consistent calibration of even the most sophisticated systems.

The S9318 is a pin-compatible performance upgrade for other industry nonvolatile potentiometers. The S9318 offers double the resolution of these devices and provides 'clickless' transitions of $V_{OUT}$.

## FUNCTIONAL BLOCK DIAGRAM



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Characteristics subject to change without notice
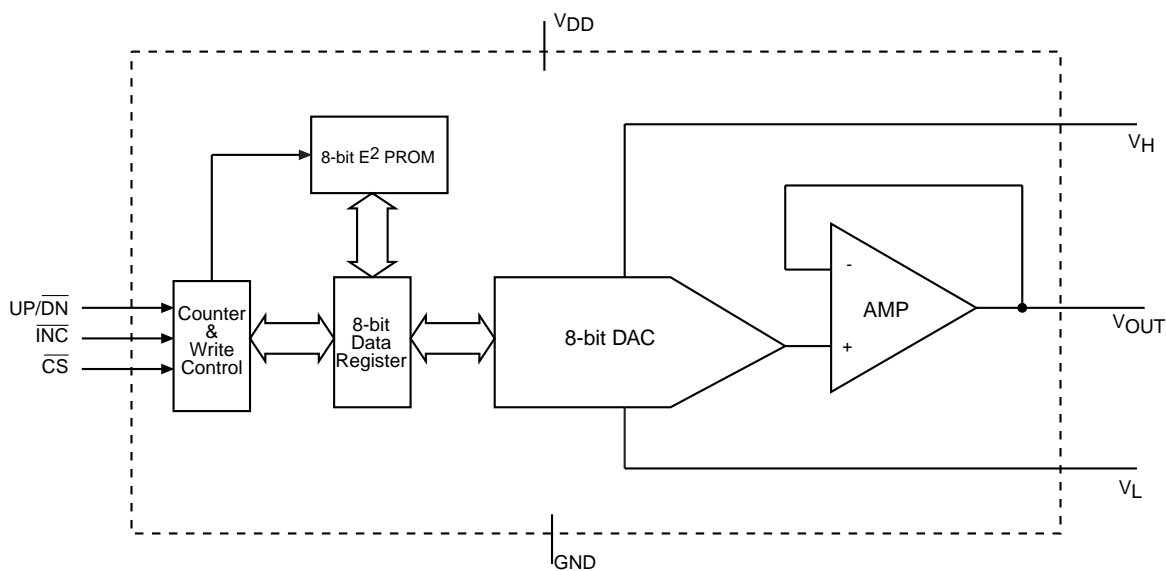
**PIN NAMES**

| Symbol | Description |
|--------|-------------|
| $\overline{\text{INC}}$ | Increment Input, High to Low Edge Trigger |
| UP/$\overline{\text{DN}}$ | Up/Down Input controlling relative $V_{OUT}$ movement |
| $V_H$ | V+ reference input |
| GND | Analog and Digital Ground |
| $V_{OUT}$ | Trimmed Voltage Output |
| $V_L$ | V- reference input |
| $\overline{\text{CS}}$ | Active low chip select input |
| $V_{DD}$ | Supply Voltage (2.7V to 5.5V) |

**PINOUT**



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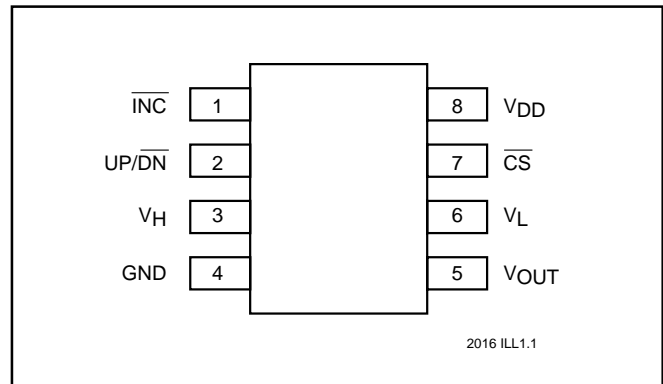
**Analog Section**
The S9318 is an 8-bit, voltage output digital-to-analog converter (DAC). The DAC consists of a resistor network that converts an 8-bit value into equivalent analog output voltages in proportion to the applied reference voltage.

**Reference Inputs**
The voltage differential between the $V_L$ and $V_H$ inputs sets the full-scale output voltage range. $V_L$ must be equal to or greater than ground (i.e. a positive voltage). $V_H$ must be greater than $V_L$ and less than or equal to $V_{DD}$. See table on page 3 for guaranteed operating limits.

**Output Buffer Amplifier**
The voltage output is a precision unity-gain follower that can slew up to 1V/$\mu$s.

**Digital Interface**
The interface is designed to emulate a simple up/down counter, but instead of a parallel count output, a ratiometric voltage output is provided.

**Chip Select ($\overline{\text{CS}}$)** is an active low input. Whenever $\overline{\text{CS}}$ is high the S9318 is in standby mode and consumes the least power. This mode is equivalent to a potentiometer that is adjusted to the required setting. When $\overline{\text{CS}}$ is low the S9318 will recognize transitions on the $\overline{\text{INC}}$ input and will move the $V_{OUT}$ either toward the $V_H$ reference or toward the $V_L$ reference depending upon the state of the UP/$\overline{\text{DN}}$ input.

The host may exit an adjustment routine in two ways: deselecting the S9318 while $\overline{\text{INC}}$ is low will not perform a store operation (a subsequent power cycle will recall the original data); deselecting the S9318 while $\overline{\text{INC}}$ is high will store the current $V_{OUT}$ setting into nonvolatile memory.

**Increment ($\overline{\text{INC}}$)** is an edge triggered input. Whenever $\overline{\text{CS}}$ is low and a high to low transition occurs on the $\overline{\text{INC}}$ input, the $V_{OUT}$ voltage will either move toward $V_H$ or $V_L$ depending upon the state of the UP/$\overline{\text{DN}}$ input.

**UP/Down (UP/$\overline{\text{DN}}$)** is an input that will determine the $V_{OUT}$ movement relative to $V_H$ and $V_L$. When $\overline{\text{CS}}$ is low, UP/$\overline{\text{DN}}$ is high and there is a high to low transition on $\overline{\text{INC}}$, the $V_{OUT}$ voltage will move (1/256$^{th}$ x $V_H$-$V_L$) toward $V_H$. When $\overline{\text{CS}}$ and UP/$\overline{\text{DN}}$ are low, and there is a high to low transition on $\overline{\text{INC}}$, the $V_{OUT}$ will move (1/256$^{th}$ x $V_H$-$V_L$) toward $V_L$.

## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Temperature Under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on pins with reference to GND: | |
| Analog Inputs | -0.5V to $V_{DD}$+.5V |
| Digital Inputs | -0.5V to $V_{DD}$+.5V |
| Analog Outputs | -0.5V to $V_{DD}$+.5V |
| Digital Outputs | -0.5V to $V_{DD}$+.5V |
| Lead Solder Temperature (10 secs) | 300°C |

**\*COMMENT**

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operation sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

## RECOMMENDED OPERATING CONDITIONS

| Condition | Min | Max |
|---|---|---|
| Temperature | -40°C | +85°C |
| $V_{DD}$ | +2.7V | +5.5V |

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## DAC DC ELECTRICAL CHARACTERISTICS

$V_{DD}$ = +2.7V to +5.5V, $V_{refH}$ = $V_{DD}$, $V_{refL}$ = 0V, $T_A$ = -40°C to +85°C, unless specified otherwise

| | Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| *Accuracy* | INL | Integral Non-Linearity | $I_{LOAD}$ = 100µA, | - | 0.5 | ±1 | LSB |
| | DNL | Differential Non-Linearity | $I_{LOAD}$ = 100µA, Guaranteed but not tested | - | 0.1 | ±0.5 | LSB |
| *References* | $V_H$ | $V_{refH}$ Input Voltage | | $V_{refL}$ | - | $V_{DD}$ | V |
| | $V_L$ | $V_{refL}$ Input Voltage | | Gnd | - | $V_{refH}$ | V |
| | $R_{IN}$ | $V_{refH}$ to $V_{refL}$ Resistance | | - | 38K | - | Ω |
| | $TCR_{IN}$ | Temperature Coefficient of $R_{IN}$ | $V_{refH}$ to $V_{refL}$ | - | 600 | - | ppm/°C |
| *Analog* *Output* | $G_{EFS}$ | Full-Scale Gain Error | DATA = FF | - | - | ±1 | LSB |
| | $V_{OUT}ZS$ | Zero-Scale Output Voltage | DATA = 00 | 0 | | 20 | mV |
| | $TCV_{OUT}$ | $V_{OUT}$ Temperature Coefficient | $V_{DD}$ = +5, $I_{LOAD}$ = 50µA, $V_{refH}$ = +5V, $V_{refL}$ = 0V Guaranteed but not tested | - | - | 50 | µV/°C |
| | $I_L$ | Amplifier Output Load Current | | -200 | | +1000 | µA |
| | $R_{OUT}$ | Amplifier Output Resistance | $I_L$ = 100µA $V_{DD}$ = +5V $V_{DD}$ = +3V | - - | 10 20 | | Ω Ω |
| | PSRR | Power Supply Rejection | $I_{LOAD}$ = 10µA | - | - | 1 | LSB/V |
| | $e_N$ | Amplifier Output Noise | f = 1KHz, $V_{DD}$ = +5V | - | 90 | - | nV/$\sqrt{Hz}$ |
| | THD | Total Harmonic Distortion | $V_{IN}$ = 1V rms, f = 1KHz | - | 0.08 | - | % |
| | BW | Bandwidth - 3dB | $V_{IN}$ = 100mV rms | - | 300 | - | kHz |

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**RELIABILITY CHARACTERISTICS**

| Symbol | Parameter | Min | Max | Unit | Test Method |
|--------|-----------|-----|-----|------|-------------|
| $V_{ZAP}$ | ESD Susceptibility | 2000 | | V | MS-883, TM 3015 |
| $I_{LTH}$ | Latch-Up | 100 | | mA | JEDEC Standard 17 |
| $T_{DR}$ | Data Retention | 100 | | Years | MS-883, TM 1008 |
| $N_{END}$ | Endurance | 1,000,000 | | Stores | MS-883, TM 1033 |

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**DC ELECTRICAL CHARACTERISTICS** $V_{DD}$ = +2.7V to +5.5V, $V_H$ = $V_{DD}$, $V_L$ = 0V, Unless otherwise specified

| Symbol | Parameter | Conditions | Min | Max | Units |
|--------|-----------|-----------|-----|-----|-------|
| $I_{DD}$ | Supply Current during store, note 1 | CS = $V_{IL}$ | | 1.2 | mA |
| $I_{SB}$ | Supply Standby Current | CS = $V_{IH}$ | | 200 | µA |
| $I_{IH}$ | Input Leakage Current | $V_{IN}$ = $V_{DD}$ | | 10 | µA |
| $I_{IL}$ | Input Leakage Current, note 2 | $V_{IN}$ = 0V | | -25 | µA |
| $V_{IH}$ | High Level Input Voltage | | 2 | $V_{DD}$ | V |
| $V_{IL}$ | Low Level Input Voltage | | 0 | 0.8 | V |

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**Notes:**

1. $I_{DD}$ is the supply current drawn while the EEPROM is being updated. $I_{DD}$ does not include the current that flows through the Reference resistor chain.

2. $\overline{CS}$, UP/$\overline{DN}$ and $\overline{INC}$ have internal pull-up resistors of approximately 200kΩ. When the input is pulled to ground the resulting output current will be $V_{DD}$/200kΩ.
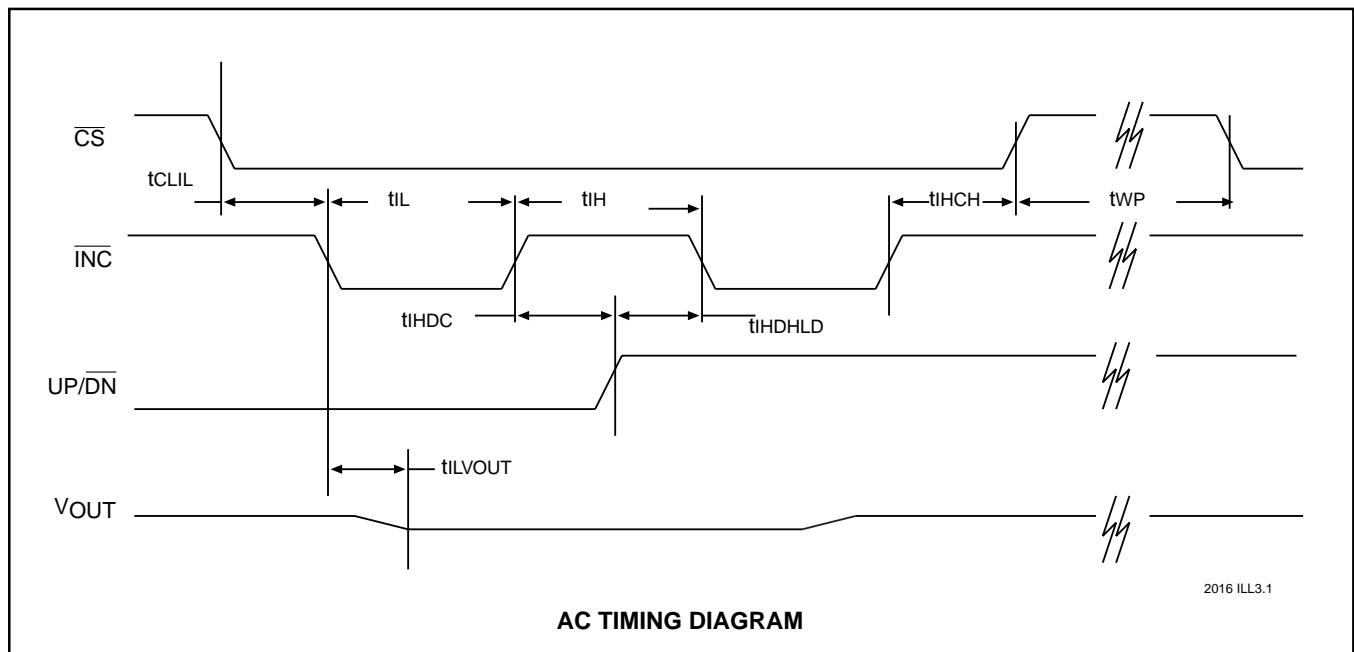
## OPERATIONAL TRUTH TABLE

| $\overline{\text{INC}}$ | $\overline{\text{CS}}$ | UP/$\overline{\text{DN}}$ | Operation |
|---|---|---|---|
| HI$_{\text{TO}}$LO | L | H | $V_{\text{OUT}}$ toward $V_H$ |
| HI$_{\text{TO}}$LO | L | L | $V_{\text{OUT}}$ toward $V_L$ |
| H | LO$_{\text{TO}}$HI | X | Store Setting |
| L | LO$_{\text{TO}}$HI | X | Maintain Setting, NO Store |
| $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | Standby |

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## AC TIMING CHARACTERISTICS  $V_{DD}$ = +4.5V to +5.5V

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $t_{CLIL}$ | $\overline{\text{CS}}$ to $\overline{\text{INC}}$ Setup | 100 | | ns |
| $t_{IHDC}$ | $\overline{\text{INC}}$ High to UP/$\overline{\text{DN}}$ Change | 100 | | ns |
| $t_{DCIL}$ | UP/$\overline{\text{DN}}$ to $\overline{\text{INC}}$ Setup | 100 | | ns |
| $t_{IL}$ | $\overline{\text{INC}}$ Low Period | 200 | | ns |
| $t_{IH}$ | $\overline{\text{INC}}$ High Period | 200 | | ns |
| $t_{IHCH}$ | $\overline{\text{INC}}$ Inactive to $\overline{\text{CS}}$ Inactive | 100 | | ns |
| $t_{WP}$ | $\overline{\text{Write}}$ Cycle Time | | 5 | ms |
| $t_{ILVOUT}$ | $\overline{\text{INC}}$ to $V_{OUT}$ Delay | | 5 | µs |

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**AC TIMING DIAGRAM**

2016 ILL3.1

2016-04 4/24/99

**8 Pin SOIC (Type S) Package JEDEC (150 mil body width)**

.157 (4.00)
.150 (3.80)

.196 (5.00)
.189 (4.80)

1

.061 (1.75)
.053 (1.35)

.0192 (.49)
.0138 (.35)

.0098 (.25)
.004 (.127)

.05 (1.27) TYP.

.050 (1.27) TYP.

.050 (1.270) TYP.
8 Places

.275 (6.99) TYP.

.030 (.762) TYP.
8 Places

FOOTPRINT

.020 (.50)
.010 (.25) x45°

.035 (.90)
.016 (.40)

.244 (6.20)
.228 (5.80)

8pn JEDEC SOIC ILL.2

**ORDERING INFORMATION**

S9318        S

**Base Part Number**

**Package**
S = 8 Pin SOIC
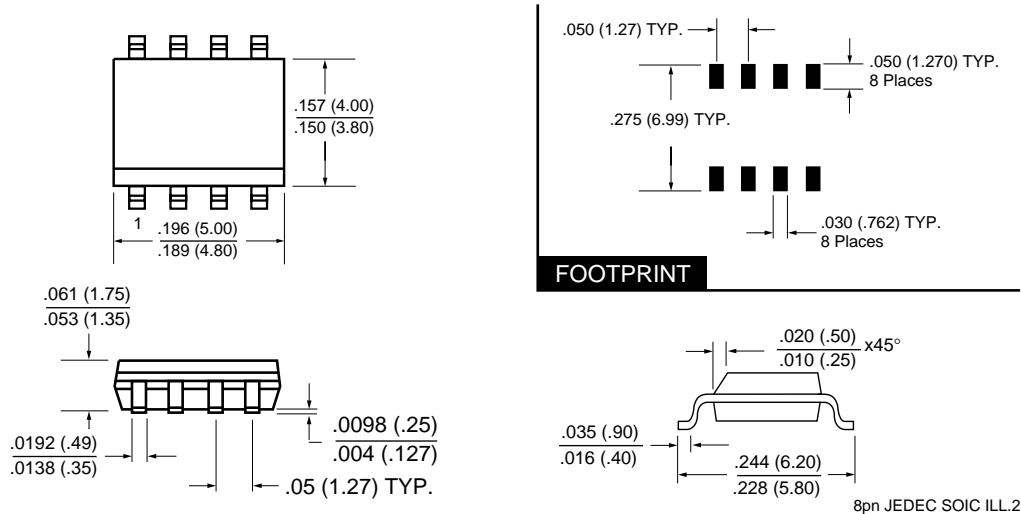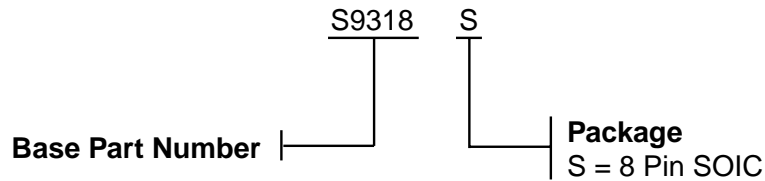
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