NEC
NEC Electronics Inc.

μPD7514
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTER WITH LCD CONTROLLER/DRIVER

Description

The μPD7514 is a 4-bit single-chip microcomputer with a 4-bit ALU, a 4K × 8-bit program memory (ROM), a 256 × 4-bit data memory (RAM), an 8-bit serial interface, a programmable 8-bit timer/event counter, an LCD controller/driver, and 31 general purpose I/O lines.

The LCD controller/driver supervises all of the timing required by 32 segment drivers and 4 common drivers, for biplexed/triplexed LCD (1/2 bias method) or triplexed/quadriplexed LCD (1/3 bias method).

The instruction set includes transfer and increment/decrement instructions to directly address memory, memory bit manipulation instructions, test instructions for bit test and data comparison, memory reference instructions with automatic register increment/decrement functions, table look-up instructions, load instructions with a string effect, and multi-branch instructions.

The μPD7514 allows the organization of any system with the least additional circuitry. It is suited for the following applications:

- Telephones
- Personal radio equipment
- Automobile equipment (electric)
- High-grade electronic calculators
- Electronic games
- VCRs

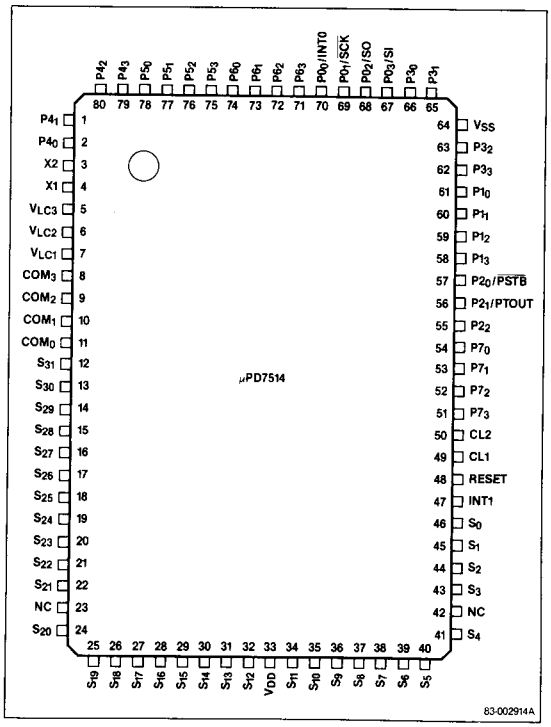
Features

- ☐ 92 powerful instructions
- ☐ Instruction cycle 5 μs at 400 kHz, 5 V
- ☐ Interrupts
  - 2 external: INT0, INT1
  - 2 internal: INTT (timer/event counter)
    INTS (serial interface)
- ☐ Programmable 8-bit timer/event counter
  - Time base count operation
  - External event count operation
- ☐ 8-bit serial interface (three serial clocks)
- ☐ LCD controller/driver
  - Static method
  - Biplexed/triplexed LCD (1/2 bias method)
  - Triplexed/quadriplexed LCD (1/3 bias method)
  - Common outputs (strobe): 4 lines (COM_0–COM_3)
  - Segment outputs (data): 32 lines (S_0–S_{31})
- ☐ Standby operation
  - Stop and halt modes
- ☐ I/O ports
  - 4-bit input port ($P0_0$/INT0, $P0_1$/$\overline{SCK}$, $P0_2$/SO, $P0_3$/SI)
  - Strobed 4-bit I/O port ($P1_0$–$P1_3$)
  - 3-bit output port ($P2_0$/$\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$)
  - 4-bit output port ($P3_0$–$P3_3$)
  - 4-bit I/O ports ($P4_0$–$P4_3$, $P5_0$–$P5_3$, $P6_0$–$P6_3$, $P7_0$–$P7_3$)
- ☐ On-chip RC oscillator for system clock
- ☐ Crystal oscillator input pins
- ☐ CMOS technology
- ☐ Low power consumption
- ☐ Single power supply (2.7 V to 6.0 V)

Ordering Information

Part No.	Package Type	Max Frequency of Operation
μPD7514G-12	80-pin plastic miniflat	500 kHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1, 2, 79, 80	$P4_0$-$P4_3$	I/O port 4
3, 4	X1, X2	Crystal clock
5-7	V_{LC1}-V_{LC3}	LCD bias voltage input
8-11	COM_0-COM_3	LCD common output
12-22, 24-32, 34-41, 43-46	S_0-S_{31}	LCD segment output
33	V_{DD}	Power supply positive
47	INT1	External interrupt input
48	RESET	Reset input
49, 50	CL1, CL2	System clock
51-54	$P7_0$-$P7_3$	I/O port 7
55 56 57	$P2_2$ $P2_1$/PTOUT $P2_0$/$\overline{PSTB}$	3-bit output port 2. PTOUT is the timer F/F output. $\overline{PSTB}$ is the strobe output.
58-61	$P1_0$-$P1_3$	I/O port 1
62, 63, 65, 66	$P3_0$-$P3_3$	I/O port 3
64	VSS	Ground
67 68 69 70	$P0_3$/SI $P0_2$/SO $P0_1$/$\overline{SCK}$ $P0_0$/INT0	4-bit input port 0. Serial input. Serial output. Serial clock I/O. Interrupt request input.
71-74	$P6_0$-$P6_3$	I/O port 6
75-78	$P5_0$-$P5_3$	I/O port 5

Status of Unused Pins

Name	Pin Connection
CL2	Open
X1	V_{SS}
X2	Open
INT1 $P0_0$/INT0	V_{SS}
$P0_1$/$\overline{SCK}$ $P0_2$/SO $P0_3$/SI $P1_0$-$P1_3$	V_{SS} or V_{DD}
$P2_0$/$\overline{PSTB}$ $P2_1$/PTOUT $P2_2$ $P3_0$-$P3_3$	Open
$P4_0$-$P4_3$ $P5_0$-$P5_3$ $P6_0$-$P6_3$ $P7_0$-$P7_3$	Input mode: V_{SS} or V_{DD} Output mode: Open
S_0-S_{31} COM_0-COM_3 V_{LC1}-V_{LC3}	Open

Pin Functions

$P0_0$-$P0_3$ (Port 0)

This is the 4-bit input port 0. The pins also operate as the interrupt input (INT0/$P0_0$), serial clock I/O ($\overline{SCK}$/$P0_1$), and serial data output (SO/$P0_2$) and input (SI/$P0_3$).

$P1_0$-$P1_3$ (Port 1)

This is the 4-bit I/O port 1. Data on these lines is loaded into the accumulator by execution of a port input instruction (IP, IP1, IPL). The contents of the accumulator are output by the execution of a port output instruction (OP, OPL). Port 1 does not have an output latch. When a port output instruction is executed, the strobe signal, which is used for latching output data externally, is automatically output from $\overline{PSTB}$. The $\overline{PSTB}$ signal is suitable for data output to memory or peripheral circuits requiring write strobe signals. Port 1 is usually held high impedance, and is driven for output with a port output instruction.

$P2_0$-$P2_2$ (Port 2)

This is the three-state 3-bit latched output port 2. Following RESET, these pins become high impedance.

When port 1 is outputting data, $P2_0$ operates as the write strobe output ($P2_0$/$\overline{PSTB}$). $P2_1$ is the output ($P2_1$/PTOUT) for the timer flip-flop signal (TOUT).

$P3_0$-$P3_3$ (Port 3)

This is the 4-bit latched output port 3. On RESET, the contents of the output latches become undefined and the output goes high impedance.

$P4_0$-$P4_3$ (Port 4), $P5_0$-$P5_3$ (Port 5)

Ports 4 and 5 are both 4-bit latched I/O ports. Ports 5 and 4 can be treated as a pair, and can input or output 8-bit data (by an IP54 or OP54 instruction) between the accumulator and memory (addressed by the HL register).

A RESET or input instruction will place these ports in input mode (high impedance). On RESET, the output latch contents become undefined.

If data is input to an I/O port just after changing it from output to input mode, data on the line at the execution of the first input instruction may be unstable. Accordingly, the first input data just after the modification should be ignored. Executing the input instruction again will insure the data is stable.

$P6_0$-$P6_3$ (Port 6)

This is the 4-bit latched I/O port 6. Each line can be set as an input or output using the port 6 mode register (PM_3-PM_0). Port 6 performs data I/O to and from the accumulator in 4-bit units. An output instruction will cause the output latches to latch the contents of the accumulator. Then the contents of the output latch at the bit position that the PMR designates as being in the output mode are output from the pins via the output buffers. The other pins are high impedance (input).

$P7_0$-$P7_3$ (Port 7)

This is the 4-bit latched I/O port 7. An input instruction reads port data into the accumulator. An output instruction latches and outputs the accumulator contents. A RESET or input instruction will place port 7 in input mode (high impedance).

INT0 (Interrupt 0)

This input is the rising-edge-triggered external interrupt. It has a Schmidt-trigger input in order to decrease noise. Setting bit 3 of the shift mode register (SM_3) low level selects INTS; setting it high selects INT0. INT0 can be used in both stop and halt modes.

INT1 (Interrupt 1)

INT1 is the rising-edge-triggered external interrupt input.

X1, X2 (Crystal Clock)

X1 and X2 are the crystal connection pins for the count clock generator. An external clock may be input to X1 directly, in which case X2 must be open.

CL1, CL2 (System Clock)

CL1 and CL2 are the resistor and capacitor connection pins for the system clock generator. An external clock may be input to CL1 directly, in which case CL2 must be open.

S_0-S_{31} (Segment)

These segment signal outputs directly drive the LCD segment lines. They are used for biplexed/triplexed LCD (1/2 bias method) and triplexed/quadriplexed LCD (1/3 bias method).

COM_0-COM_3 (Common)

These outputs directly drive common (backplane) LCD lines via the following strobe signals:

- 1/2 bias method: biplexed (COM_0, COM_1), triplexed (COM_0-COM_2)
- 1/3 bias method: triplexed (COM_0-COM_2), quadriplexed (COM_0-COM_3)

V_{LC1}, V_{LC2}, V_{LC3} (LCD Power Supply)

These pins are the LCD bias voltage supply. Based on applied voltages to these pins, the on-chip LCD controller/driver generates segment and common signals to the LCD. The bias voltage configuration for the 1/2 bias method is different from that for the 1/3 bias method.

RESET

A high level input to this pin resets the μPD7514.

VDD

Positive power supply.

VSS

Ground.

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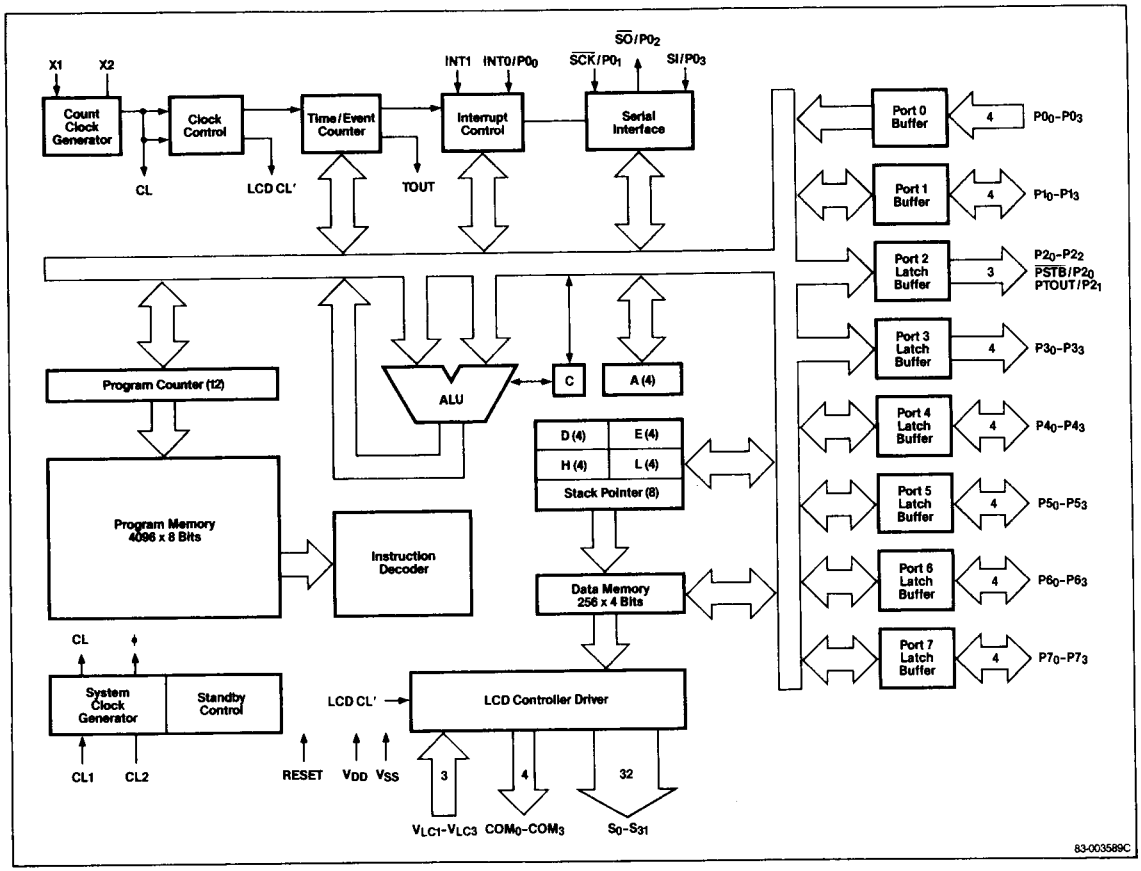
Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$

Supply voltage, V_{DD}	−0.3 V to +7 V
Input voltage, V_I	−0.3 V to V_{DD} +0.3 V
Output voltage, V_O	−0.3 V to V_{DD} +0.3 V
Output current high, I_{OH}	
Per pin	−5 mA
Total, all output ports	−50 mA
Output current low, I_{OL}	
Per pin	15 mA
Total, Ports 0, 4, 5, 6, $P3_0$, $P3_1$	40 mA
Total, Ports 1, 2, 7, $P3_2$, $P3_3$	40 mA
Operating temperature, T_{OPT}	−10°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{DD} = 2.7$ V to 6 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except X1, CL1, RES, INT0, INT1, SI, $\overline{SCK}$
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	RES, INT0, INT1, SI, $\overline{SCK}$
	V_{IH3}	$V_{DD}-0.5$		V_{DD}	V	X1, CL1
Input voltage low	V_{IL1}	0		0.3 V_{DD}	V	Except X1, CL1, RES, INT0, INT1, SI, $\overline{SCK}$
	V_{IL2}	0		0.2 V_{DD}	V	RES, INT0, INT1, SI, $\overline{SCK}$
	V_{IL3}	0		0.5	V	X1, CL1
Output voltage high	V_{OH}	$V_{DD}-1.0$			V	V_{DD} = 4.5 to 6.0 V; $I_{OH} = -1.0$ mA
		$V_{DD}-0.5$			V	$I_{OH} = -100$ μA
Output voltage low	V_{OL}			0.4	V	V_{DD} = 4.5 to 6.0 V; I_{OL} = 1.6 mA
				0.5	V	I_{OL} = 400 μA
Input leakage current high	I_{LIH1}			3	μA	$V_I = V_{DD}$ except X1, CL1
	I_{LIH2}			10	μA	$V_I = V_{DD}$; X1, CL1
Input leakage current low	I_{LIL1}			−3	μA	V_I = 0 V except X1, CL1
	I_{LIL2}			−10	μA	X1, CL1
Output leakage current high / low	I_{LOH}			3	μA	$V_O = V_{DD}$
	I_{LOL}			−3	μA	V_O = 0 V

DC Characteristics (cont)

$T_A = -10°C$ to $+70°C$, $V_{DD} = 2.7$ V to 6 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Common output impedance	R_{COM}		3	5	kΩ	V_{DD} = 4.5 to 6.0 V
			5	15	kΩ	
Segment output impedance	R_S		15	20	kΩ	V_{DD} = 4.5 to 6.0 V
			20	60	kΩ	
Supply current	I_{DD1}		600	1800	μA	Operating mode V_{DD} = 5 V ±10%; R = 39 kΩ ±2%; C = 33 pF ±5%
			70	210	μA	Operating mode V_{DD} = 3 V ±10%; R = 160 kΩ ±2%; C = 33 pF ±5%
	I_{DD2}		300	900	μA	Halt mode X1 = 0 V; V_{DD} = 5 V ±10%; R = 39 kΩ ±2%; C = 33 pF ±5%
			35	100	μA	Halt mode X1 = 0 V; V_{DD} = 3 V ±10%; R = 160 kΩ ±2%; C = 33 pF ±5%
	I_{DD3}		1.0	20	μA	Stop mode X1 = 0 V; V_{DD} = 5 V ±10%
			0.3	10	μA	Stop mode X1 = 0 V; V_{DD} = 3 V ±10%

Capacitance

$T_A = 25°C$; $V_{DD} = 0$ V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			15	pF	(Note 1)
Output capacitance	C_O			15	pF	(Note 1)
I/O capacitance	C_{IO}			15	pF	(Note 1)

Note:
(1) f_C = 1 MHz. Return unmeasured pins to 0 V.

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AC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{DD} = 3$ V to 6 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock oscillation (CL1, CL2)	f_{cc}	300	400	500	kHz	C = 33 pF ±5%, |ΔC/°C| ≤ 60 ppm R = 39 kΩ ±2%, V_{DD} = 5 V ±10%
		75	100	120	kHz	C = 33 pF ±5%, |ΔC/°C| ≤ 60 ppm R = 160 kΩ ±2%, V_{DD} = 3 V ±10%
System clock input frequency (CL1)	f_c	10		510	kHz	V_{DD} = 4.5 V to 6.0 V, Duty = 50%
		10		150	kHz	Duty = 50%
CL1 input rise time	t_{CR}			0.2	μs	
CL1 input fall time	t_{CF}			0.2	μs	
CL1 input pulse width high	t_{CH}	0.9		50	μs	V_{DD} − 4.5 V to 6.0 V
		3.2		50	μs	
CL1 input pulse width low	t_{CL}	0.9		50	μs	V_{DD} = 4.5 V to 6.0 V
		3.2		50	μs	
Count clock oscillation frequency (X1, X2)	f_{xx}	25	32	50	kHz	C1 = 20 pF C2 = 30 pF R = 220 kΩ (Note 1)
Count clock input frequency (X1)	f_x	0		500	kHz	V_{DD} = 4.5 to 6.0 V, Duty = 50%
		0		150	kHz	
X1 input rise time	t_{XR}			0.2	μs	
X1 input fall time	t_{XF}			0.2	μs	
X1 input pulse width high	t_{XH}	0.9			μs	V_{DD} = 4.5 V to 6.0 V
		3.2			μs	V_{DD} = 2.7 V
X1 input pulse width low	t_{XL}	0.9			μs	V_{DD} = 4.5 V to 6.0 V
		3.2			μs	V_{DD} = 2.7 V
Port 1 output set-up time to $\overline{PSTB}$↑	t_{PST}	(2)			μs	V_{DD} = 4.5 V to 6.0 V
		(3)			μs	
Port 1 output hold after $\overline{PSTB}$↑	t_{STP}	0.1			μs	V_{DD} = 4.5 V to 6.0 V
		0.1			μs	

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{PSTB}$ pulse width low	t_{STL}	(2)			ns	V_{DD} = 4.5 V to 6.0 V
		(3)			μs	
$\overline{SCK}$ cycle time	t_{KCY}	3.0			μs	Input V_{DD} = 4.5 V to 6.0 V
		4.0			μs	Output
		8.0			μs	Input
		13.0			μs	Output
$\overline{SCK}$ pulse width high	t_{KH}	1.3			μs	Input V_{DD} = 4.5 V to 6.0 V
		1.8			μs	Output
		3.8			μs	Input
		6.3			μs	Output
$\overline{SCK}$ pulse width low	t_{KL}	1.3			μs	Input V_{DD} = 4.5 V to 6.0 V
		1.8			μs	Output
		3.8			μs	Input
		6.3			μs	Output
SI set-up time (to $\overline{SCK}$↑)	t_{SIK}	300			ns	
SI hold time (after $\overline{SCK}$↑)	t_{KSI}	450			ns	
SO output delay time (after $\overline{SCK}$↓)	t_{KSO}			850	ns	V_{DD} = 4.5 V to 6.0 V
				1200	ns	
INT0 pulse width high	t_{I0H}	10			μs	
INT0 pulse width low	t_{I0L}	10			μs	
INT1 pulse width high	t_{I1H}	(4)			μs	
INT1 pulse width low	t_{I1L}	(4)			μs	
RESET pulse width high	t_{RSH}	10			μs	
RESET pulse width low	t_{RSL}	10			μs	

Note:

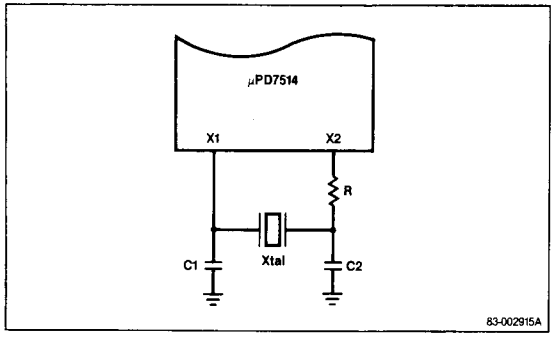
(1) See recommended clock circuit on next page.

(2) $1/2\ f_{cc} - 0.8$ or $1/2\ f_c - 0.8$

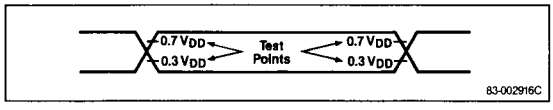
(3) $1/2\ f_{cc} - 2.0$ or $1/2\ f_c - 2.0$

(4) $2/f_{cc}$ or $2/f_c$

Recommended Clock Circuit



AC Timing Test Points



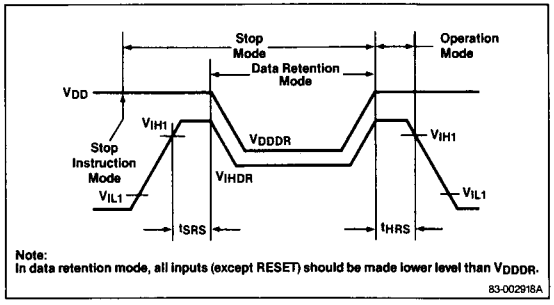
Data Retention Characteristics

$T_A = -10°C$ to $+70°C$

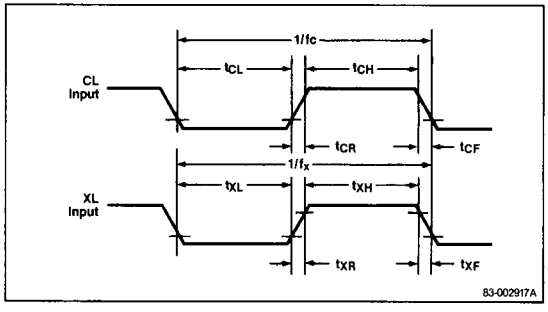
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{DDDR}	2.0			V	
Data retention supply current	I_{DDDR}		0.3	10	μA	$V_{DDDR} = 2$ V
Data retention RESET input voltage high	V_{IHDR}	0.9 × V_{DDDR}		V_{DDDR} +0.2	V	
RESET set-up time	t_{SRS}	0			ns	
RESET hold time	t_{HRS}	0			ns	

Timing Waveforms

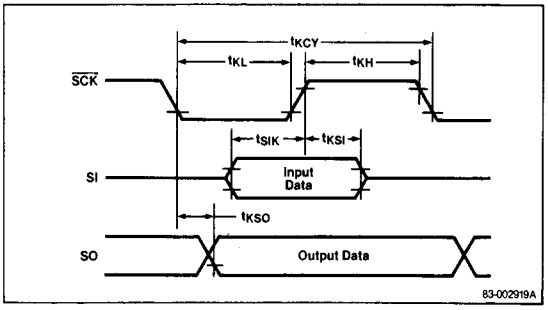
Data Retention Mode Timing



Clock Timing



Serial Transfer Timing



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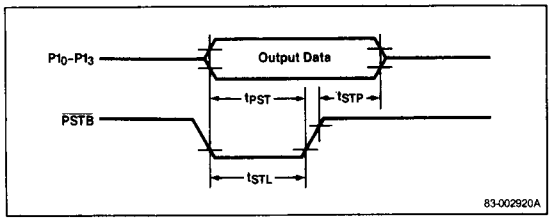
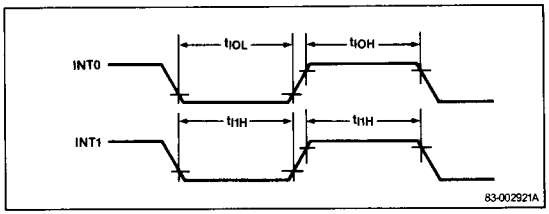
Timing Waveforms (cont)

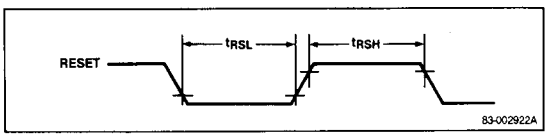
Strobe OutputTiming



Interrupt Input Timing



RESET Input Timing

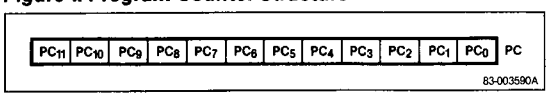


Functional Description

Program Counter (PC)

This 12-bit binary counter, shown in figure 1, holds the address of the current instruction in program memory. When an instruction executes, the PC increments by the number of bytes in the instruction. RESET clears the PC to 0.

Figure 1. Program Counter Structure



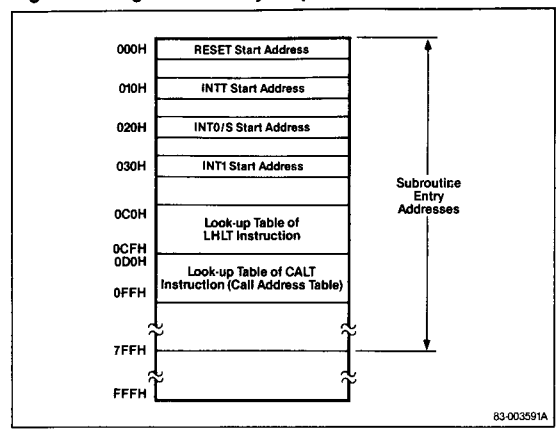
Stack Pointer (SP)

This 8-bit register (SP_7–SP_0) stores the top address of the data memory area used as a LIFO stack. The SP decrements when a call (CALL, CALT) or a push (PSHDE, PSHHL) instruction executes, and at an interrupt generation. It increments when a return (RT, RTS, RTPSW) or POP (POPDE, POPHL) instruction executes.

Program Memory (ROM)

This 4,096-word × 8-bit mask-programmable ROM stores programs and table data and is addressed by the PC. ROM address locations are from 000H to FFFH. Fixed locations are allocated to the RESET and interrupt start addresses, and table areas of the LHLT and CALT instructions. See figure 2.

Figure 2. Program Memory Map

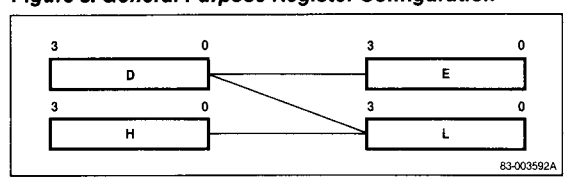


General Purpose Registers

Registers D, E, H, and L operate in units of 4 bits, or they form the 8-bit pair registers DE, DL, and HL for use as a data pointer (D or H is the upper-order 4 bits). See figure 3.

Pair register HL can perform the functions of automatic increment (+1) and automatic decrement (−1) for the L register only. The L register is also used to specify I/O ports and mode registers when the I/O instruction (OPL, IPL) is executed.

Figure 3. General-Purpose Register Configuration



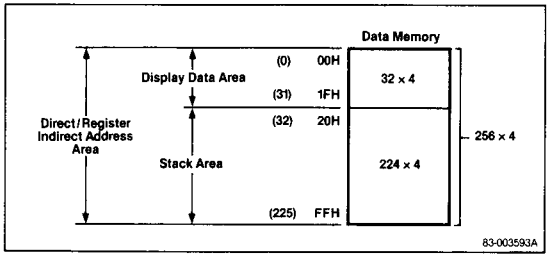
Data Memory (RAM)

This 256-word × 4-bit static RAM stores processing data and display data. It also operates with the accumulator to process data in 8-bit units. There are three types of data memory addressing:

- Direct addressing is made by the second byte of the instruction.
- Register indirect addressing is made indirectly by the contents of the register pair designated by an instruction.
- Stack indirect addressing is made by the contents of the SP.

RAM resides at addresses 00H-FFH. Thirty-two of these locations (00H-1FH) are allocated for the LCD display data area. When display data is written to 00H-1FH, the LCD controller/driver reads it and generates an LCD drive signal. Address locations 00H-1FH cannot be used as stack area. See figure 4.

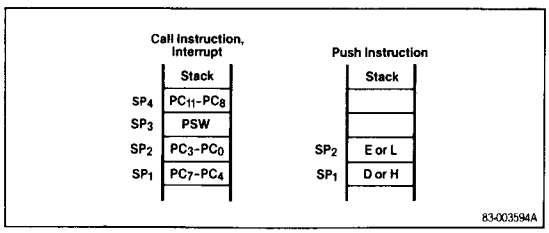
Figure 4. Data Memory Map



Addresses 20H-FFH in data memory can be used as a stack area at execution of a call or return instruction (CALL, CALT, RT, RTS, RTPSW), a push/pop instruction (PSHDE, PSHHL, POPDE, POPHL), or at an interrupt occurrence.

At the execution of a call instruction or an interrupt occurrence, the contents of the PC and PSW are stored in the stack. At the execution of a push instruction, the contents of DE or HL are stored in the stack. The data is stored in the stack as shown in figure 5.

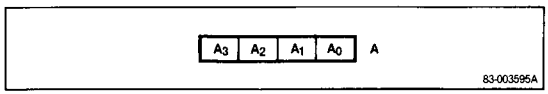
Figure 5. Stack Contents after Call, Interrupt, or Push



Accumulator (A)

The accumulator is a 4-bit register. (See figure 6.) Various arithmetic/logical operations are done mainly by the accumulator. Operating with the data memory addressed by the pair register HL, data processing may be done in 8-bit units (higher-order bits in the accumulator and lower-order bits in the data memory).

Figure 6. Accumulator Configuration



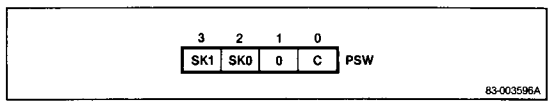
Arithmetic Logic Unit (ALU)

The ALU is a 4-bit arithmetic logic circuit that performs such processes as binary addition, arithmetic/logical operation, comparison, and rotation.

Program Status Word (PSW)

The program status word consists of two skip flags (SK_1, SK_0) and a carry flag (C). (See figure 7.) These are stored in the stack area upon execution of a call instruction (CALL, CALT) or at an interrupt occurrence; they are restored by an RTPSW instruction. At RESET, SK_1 and SK_0 are cleared to 0, and C is undefined.

Figure 7. Structure of Program Status Word



System Clock Generator Circuit

This circuit consists of an RC oscillator circuit and a half-frequency divider circuit, as shown in figure 8. The RC oscillator circuit is controlled by an external resistor (R) and capacitor (C) connected to CL1 and CL2.

An external clock can be input to CL1 without using an RC circuit. CL2 should be left open, in which case the RC oscillator circuit merely operates as an inverted buffer.

In stop mode, the RC oscillator circuit and the half-frequency divider circuit stop, thereby stopping the output of CL and ϕ, respectively. In halt mode, the half-frequency divider circuit stops (ϕ), but CL continues to be supplied.

With an external clock, when the device is in standby mode, the CL1 input clock becomes CL via an inverted buffer; CL continues to be supplied. In this case, both standby modes stop only the half-frequency divider (ϕ).

Figure 8. System Clock Generator Circuits

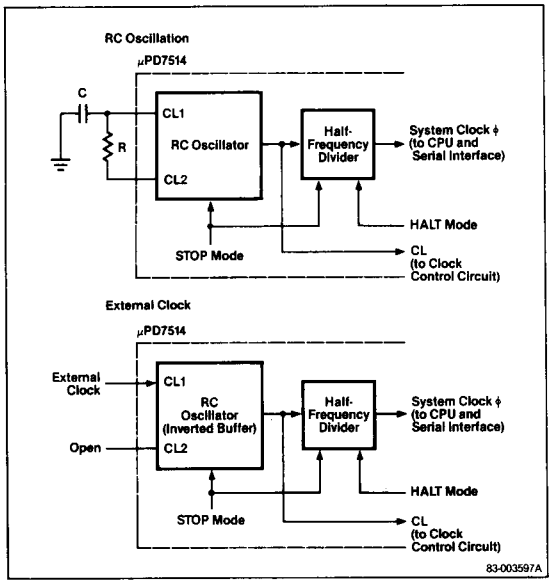
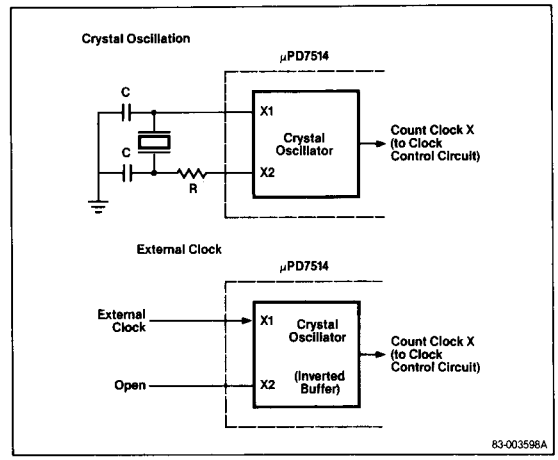


Figure 9. Count Clock Generator Circuits



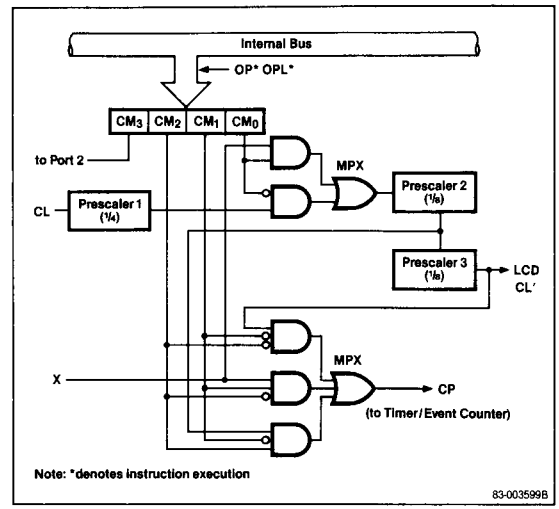
Count Clock Generator Circuit

This crystal oscillator circuit is fed either by the crystal connected to X1 and X2 or by an external clock from X1, in which case it operates as an inverted buffer. Output from this circuit (X) is sent to the clock control circuit to become a count pulse (CP) for the timer/event counter either directly, or after being frequency-divided. The frequency of X equals the crystal oscillation frequency of the X1 external clock. This circuit is unaffected by standby mode. See figure 9.

Clock Control Circuit

The clock control circuit consists of a 4-bit clock mode register (CM_3–CM_0), prescalers 1, 2, 3, and multiplexers. (See figure 10.) The circuit accepts both the system clock generator circuit output (CL) and the count clock generator circuit output (X). The clock mode register selects a clock source and prescaler designation. By so doing, the clock control circuit supplies a count pulse (CP) to the timer/event counter, and the LCD clock source (LCD CL') to the LCD controller/driver.

Figure 10. Clock Control Circuit



A code is sent to the clock mode register by transferring the contents of the accumulator with an OP or OPL instruction.

Bits CM_2–CM_0 specify a clock source and frequency of the timer-out signal. When CM_3 is high, TOUT is output via PTOUT. CM_0 selects a clock source of LCD CL' and a frequency. See table 1.

Table 1. Clock Mode Register

CM_2	CM_1	CM_0	Count Pulse Selection
0	0	0	CL × 1/256
0	0	1	X × 1/64
0	1	0	X
0	1	1	X
1	0	0	CL × 1/32
1	0	1	X × 1/8
1	1	0	Prohibited
1	1	1	Prohibited

CM_3	Output Control of TOUT
0	Output Prohibited
1	TOUT→$P2_1$ / PTOUT

CM_0	LCD CL'
0	CL × 1/256
1	X × 1/64

Timer/Event Counter

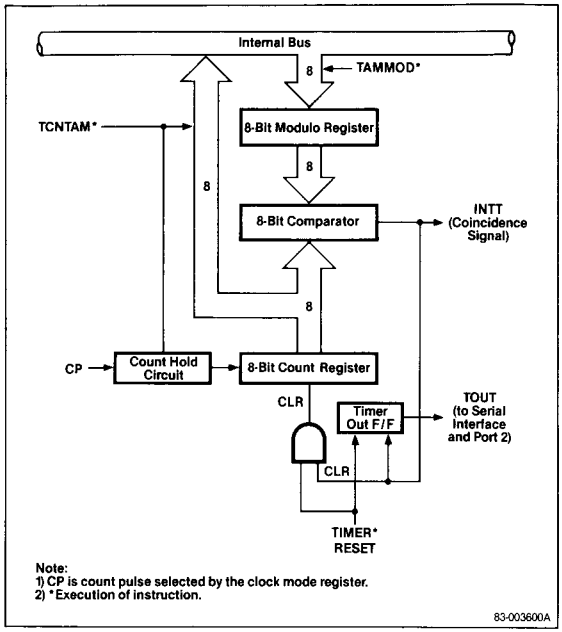
This counter consists of an 8-bit count register, an 8-bit modulo register, an 8-bit comparator, and a timer flip flop (F/F), as shown in figure 12.

The 8-bit register, a binary upcounter that increments at every input of the counter pulse (CP), is cleared to 0 by the execution of a TIMER instruction, RESET input, or a coincidence signal from the comparator.

The 8-bit modulo register determines the count register's maximum count. Its contents are set by the TAMMOD instruction. It is initialized to FFH by RESET.

The 8-bit comparator compares the contents of the count and modulo registers; it outputs the timer interrupt signal (INTT) one CP after they are found to be coincident.

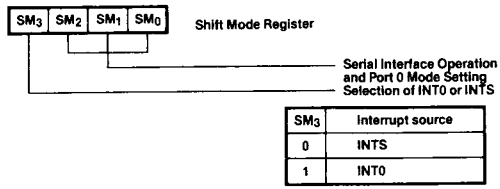
Figure 11. Timer/Event Counter Configuration



Serial Interface

The serial interface consists of an 8-bit shift register, a 4-bit shift mode register (figure 12) and a 3-bit octal counter, as shown in figure 13. This interface performs serial data I/O, which is controlled by the serial clock ($\overline{SCK}$). At the falling edge of $\overline{SCK}$, the MSB of the shift register (bit 7) is output via the SO line. At the next rising edge of $\overline{SCK}$, the register's contents shift one bit and the data on SI is loaded into the LSB. The 3-bit counter counts each $\overline{SCK}$, generates an internal interrupt (INTS) at every count of 8 clocks (at the end of a 1-byte serial data transfer), and sets the interrupt request flag (INT0/S RQF).

Figure 12. Format of Shift Mode Register

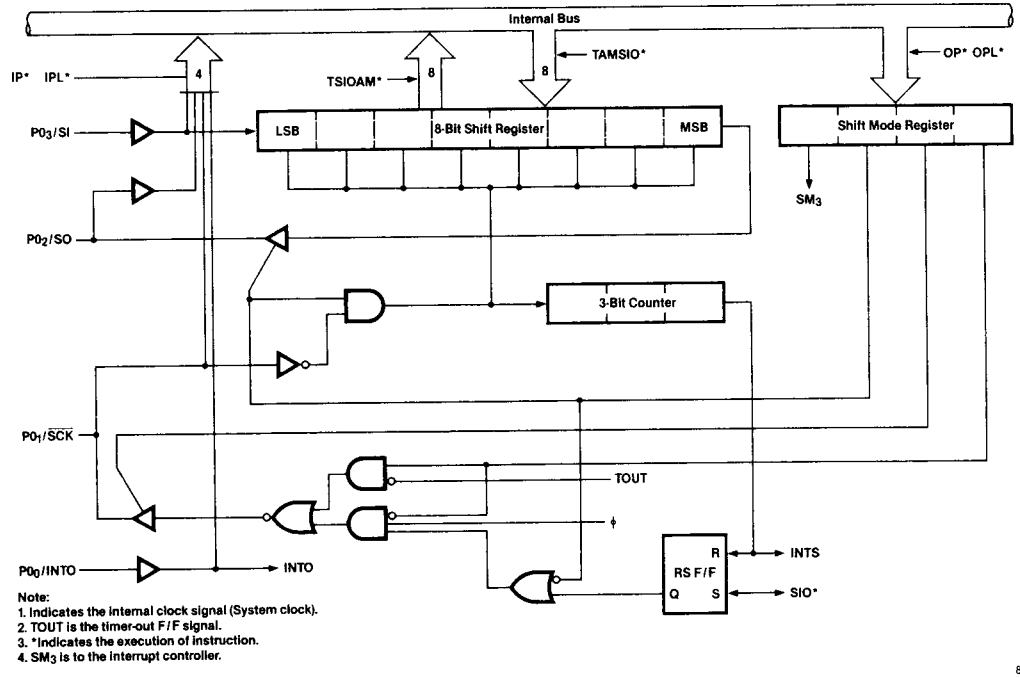


SM3	Interrupt source
0	INTS
1	INT0

SM_2	SM_1	SM_0	PO_3/SI	PO_2/SO	PO_1/SCK	Serial Operation
0	0	0	Port input	Port input	Port input	Stop
0	1	0	Port input	Port input	To output 0	Stop
0	1	1	Port input	Port input	To output TOUT	Stop
1	0	0	SI input	SO input	$\overline{SCK}$ input	To operate with external clock
1	1	0	SI Input	SO input	$\overline{SCK}$ output (0×8)	To operate with 0
1	1	1	SI input	SO input	$\overline{SCK}$ output (TOUT)	To operate with TOUT

83-003601A

Figure 13. Serial Interface Block Diagram



Note:
1. Indicates the internal clock signal (System clock).
2. TOUT is the timer-out F/F signal.
3. *Indicates the execution of instruction.
4. SM_3 is to the interrupt controller.

83-003602B

LCD Controller/Driver

This controller/driver directly drives an LCD with static, 1/2 bias voltage (biplexed, triplexed) and 1/3 bias voltage (triplexed, quadriplexed) configurations. Thirty-two segment lines (S_0-S_{31}) and 4 common lines (COM_0-COM_3) serve as the LCD driver outputs. See tables 2 and 3, and figure 14.

To supply the proper voltage to the segment and common lines, supply the voltages listed in table 4 to pins V_{LC1}, V_{LC2}, and V_{LC3}. See also figure 15.

Table 2. Maximum Segment Number

Bias	Multiplexing	COM Lines	Maximum Segment Number
1/2	biplexed	COM0, 1	64 (32 Segments × 2 Commons)
1/2	triplexed	COM0, 1, 2	96 (32 Segments × 3 Commons)
1/3	triplexed	COM0, 1, 2	96 (32 Segments × 3 Commons)
1/3	quadriplexed	COM0, 1, 2, 3	128 (32 Segments × 4 Commons)

Note:
In the following cases, LCD driving waveform stops operation and DC potential is applied between LCD electrodes. This will considerably reduce the life span of the LCD.

LCD Clock Source	Primary Causes
CL Channel 0 (System Clock)	1. STOP instruction is executed. 2. External clock is stopped.
X Channel (Count Clock)	1. External clock is stopped.

Table 3. Display Mode Register

					CMO = 0		MCO = 1	
DM_3	DM_2	DM_0	Multiplexing	Bias Voltage	LCD CL	Frame Frequency	LCD CL	Frame Frequency
0	0	0	Quadriplexed	1/3	CL/256	CL/1024	X/164	X256
		1	Triplexed			CL/768		X192
	1	0	Biplexed	1/2	CL/512	CL/1024	X/128	X256
		1	Triplexed			CL/1536		X384
0	0	0	Quadriplexed	1/3	CL/512	CL/2048	X/128	X512
		1	Triplexed			CL/1536		X584
	1	0	Biplexed	1/2	CL/1024	CL/2048	X/256	X1512
		1	Triplexed			CL/3072		X768

DM_1	Display output control	DM_1	Display output control
0	T0 deselect all segments signal	1	To enable display outs

Table 4. LCD Supply Voltage

Pin Name	1/2 Bias	1/3 Bias
V_{LC1}	V_{DD}-(1/2) V_{LCD}	V_{DD}-(1/3) V_{LCD}
V_{LC2}	V_{DD}-(1/2) V_{LCD}	V_{DD}-(2/3) V_{LCD}
V_{LC3}	V_{DD}-V_{LCD}	V_{DD}-V_{LCD}

3

Figure 14. LCD Controller/DriverBlock Diagram

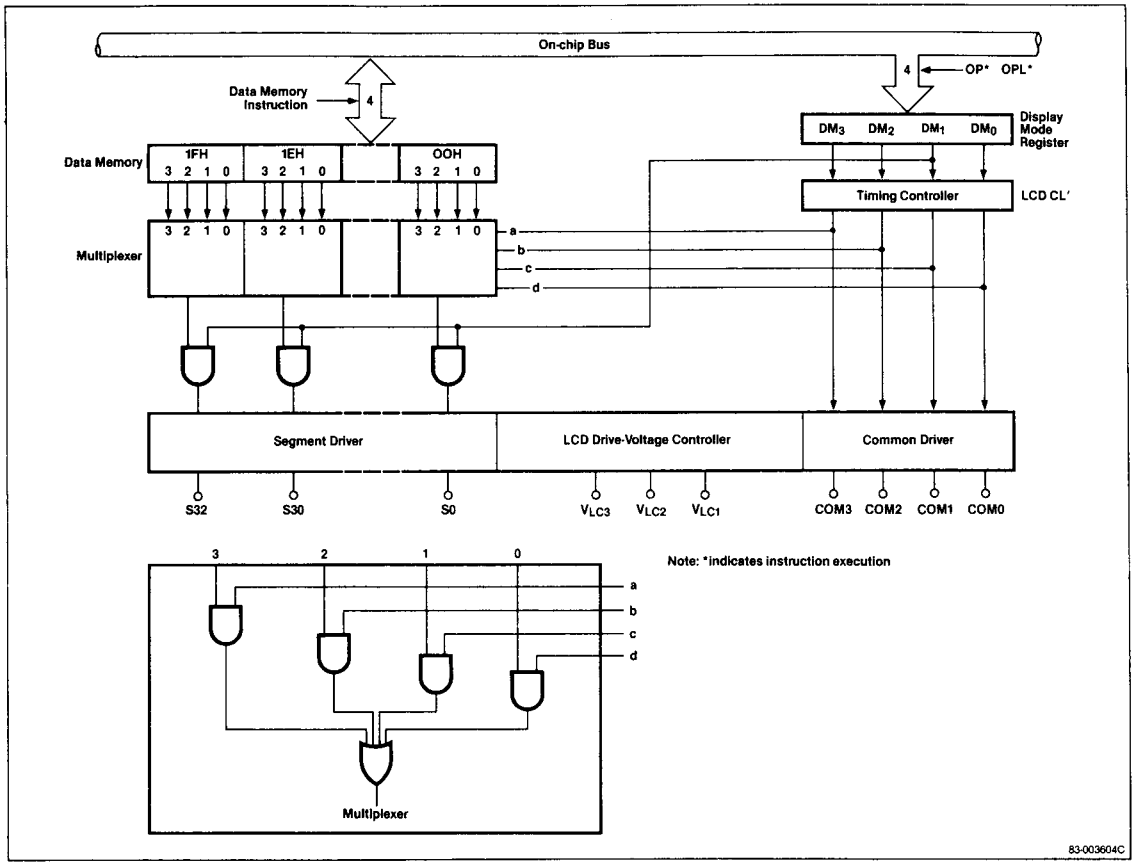
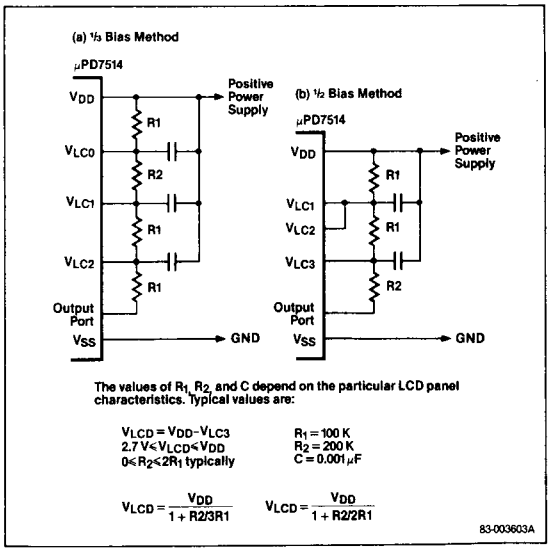


Figure 15. Configuration of LCD Power Supply by Voltage Dividing Method



Interrupt Function

There are two external (INT0, INT1) and two internal (INTT, INTS) interrupts. Interrupt INT0 and pin $P0_0$ share one line; figure 12 shows how to select between these. When INT0 is selected, either INT0 or INTS may be specified. The interrupt process (interrupt address and priority) for INT0 and INTS is the same. See table 5 and figure 16.

Interrupt Enable Register (IE_2-IE_0). This register permits or inhibits individual interrupt requests of INTT, INT0/S and INT1; it allows the interrupt if the respective bit of each interrupt is set to 1, and inhibits the interrupt if 0. See figure 17.

Figure 16. Interrupt Controller Block Diagram

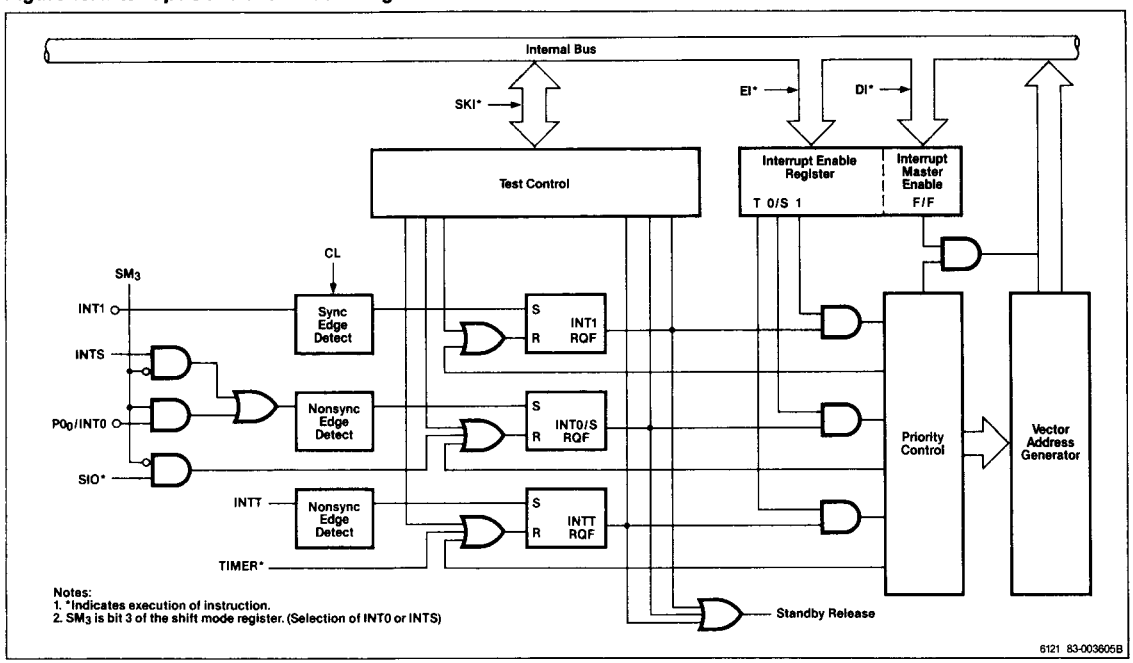
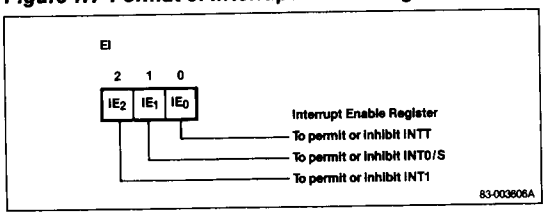


Table 5. Source of Interrupts

Interrupt	Int/Ext	Priority	Interrupt Address
INTT (coincidence signal from timer / event counter)	Int	1	10H (16)
INT0 (interrupt signal from $P0_0$ pin)	Ext	2	20H (32)
INTS (transfer end signal from serial interface)	Int	2	20H (32)
INT1 (interrupt signal from INT1 pin)	Ext	3	30H (48)

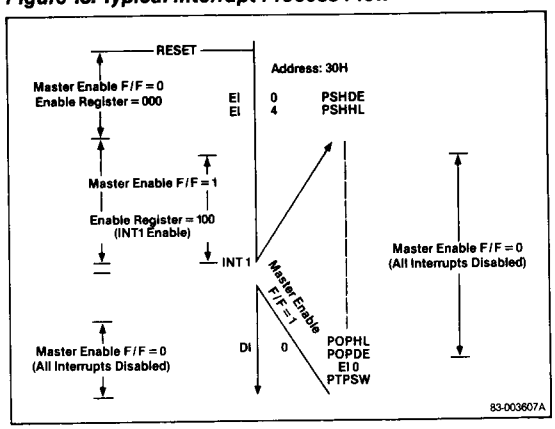
Figure 17. Format of Interrupt Enable Register



Interrupt Master Enable F/F (IME). This F/F permits or inhibits the acceptance of all interrupts (INTT, INT0, INTS, and INT1); after accepting an interrupt, it is reset to inhibit subsequent interrupts. The F/F is set by the EI 0 instruction to permit all interrupts not individually disabled, or it is reset by the DI 0 instruction to inhibit all interrupts. In either case, the interrupt enable register is unaffected.

Typical Interrupts. Figure 18 is an example of the interrupt process for the INT1 interrupt.

Figure 18. Typical Interrupt Process Flow



Standby Function

Two standby modes, stop and halt, are provided to reduce power consumption during a program standby state. The STOP and HALT instructions select these modes.

In standby mode, program execution ceases and the contents of data memory and all internal registers are held. The shift register and timer/event counter still operate.

A RESET or interrupt generation releases standby mode; if an interrupt request flag is set, stop/halt mode cannot be set in spite of the STOP/HALT instruction execution. Consequently, when setting standby mode when there is a possibility of a request flag being set, it is necessary to have the interrupt request flag reset either by processing the interrupt in advance or by executing a SKI instruction.

Differences between stop and halt modes are shown in table 6. The main difference lies in that RC oscillation output (CL) either stops (stop mode), or does not stop (halt mode), when the system clock is being supplied by RC oscillation.

Table 6. Comparing Stop and Halt Modes

Mode	Instruction	CL	0	X	CPU	SIO	CNT	Interrupt used for release
Stop	STOP	X	X	0	X	*	*	INTT, INT0/S
Halt	HALT	0	X	0	X	*	0	INTT, INT0/S, INT1

Note:
0 Operation possible
* Operation possible with a mode selected
X Operation disabled

Reset Function

A high level RESET input initializes the μPD7514. The sequence of events is as follows:

(1) The PC is cleared to 0.

(2) PSW flags SK_1 and SK_0 are cleared to 0.

(3) The timer/event counter as reset as follows:
Count register = 00H
Modulo register = FFH
Timer out F/F = 0

(4) The clock control circuit is reset as follows:
Clock mode register (CM_3–CM_0) is cleared to 0
CP = LCD CL' = CL × 1/256
TOUT is disabled.
Prescalers 1, 2, 3 = 0

(5) Shift mode register (SM_3–SM_0) is cleared to 0.
Serial interface shift operation stops.
Port 0 is placed in input mode (high impedance).
INTS is selected for the interrupt source of INT0/S.

(6) Display mode register (DM_3–DM_0) is cleared to 0.
1/3 bias, quadriplexed
Frame frequency = CL/1024, LCD drive deselected

(7) Interrupt control circuit becomes as follows:
Interrupt request flags = 0
Interrupt master enable F/F = 0
Interrupt enable register = 0
All pending interrupts cancelled.
All interrupts disabled.

(8) Port 6 mode register (PM_3–PM_0) is cleared to 0.

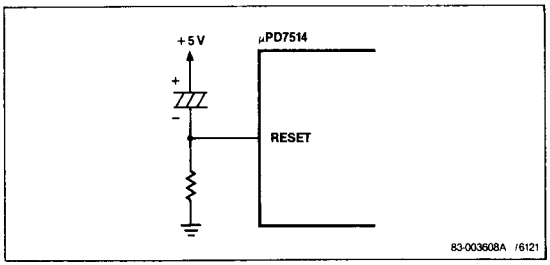
(9) All output buffers of ports 0–7 are turned off, and become high impedance, I/O ports are set to input mode.

(10) The contents of data memory and the following registers are undefined:
Stack pointer (SP)
Accumulator (A)
Carry flag (C)
General-purpose registers (D, E, H, L)
Output latch of each port
Shift register

After RESET, program execution starts from address 00H. The contents of each register must be initialized as needed.

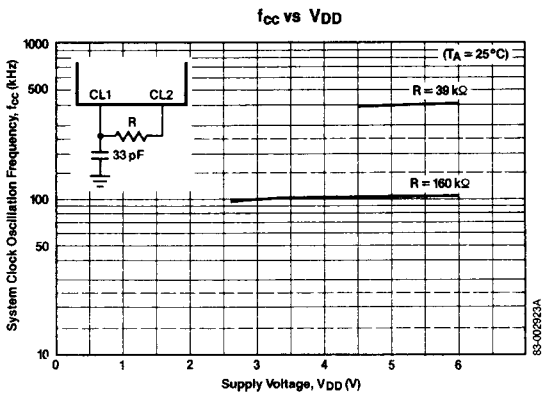
Power-On-Reset Circuit. The simplest example is shown in figure 19.

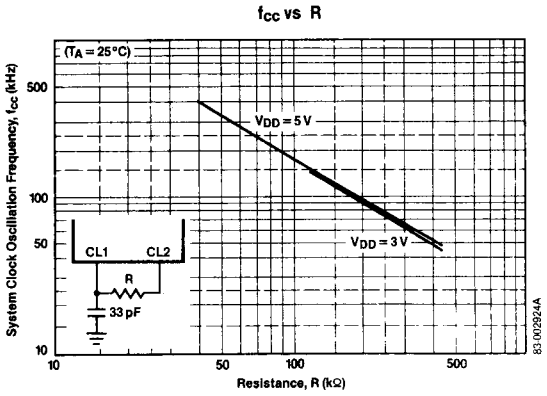
Figure 19. Power-On-Reset Circuit



3

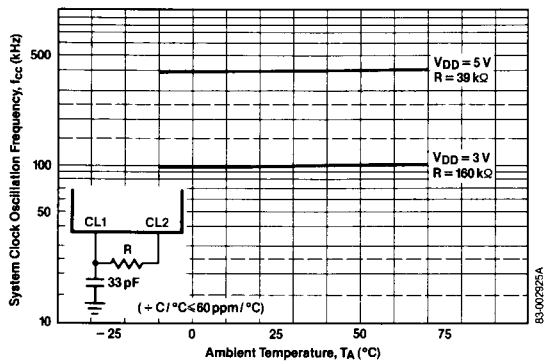
Operating Characteristics



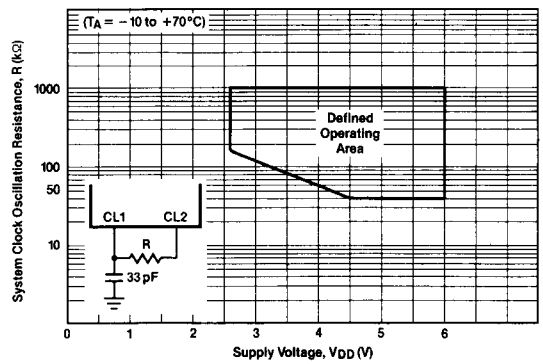


Operating Characteristics (cont)

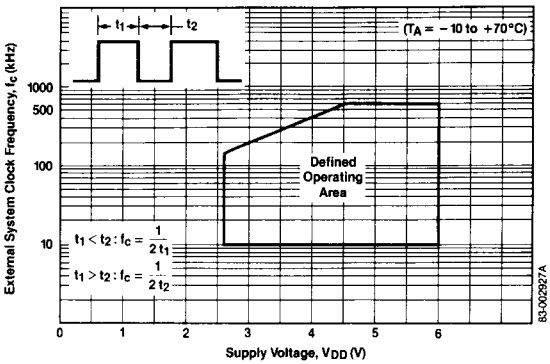
f_{CC} vs T_A



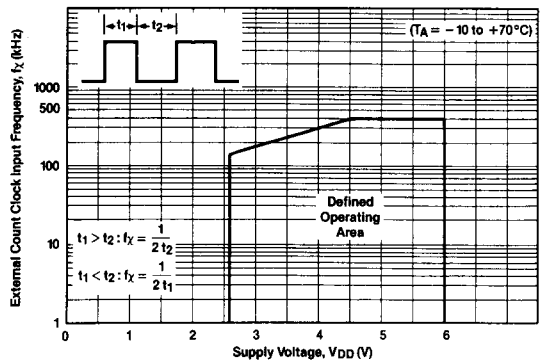
R vs V_{DD}



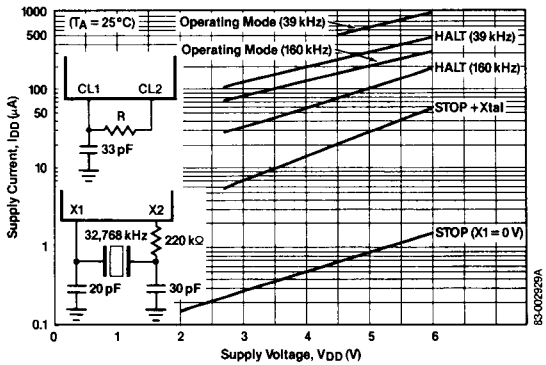
f_C vs V_{DD}



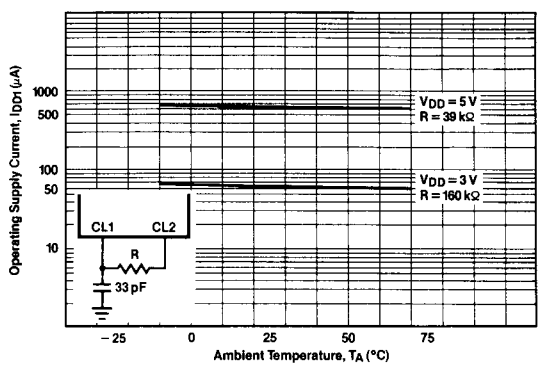
f_X vs V_{DD}



I_{DD} vs V_{DD}

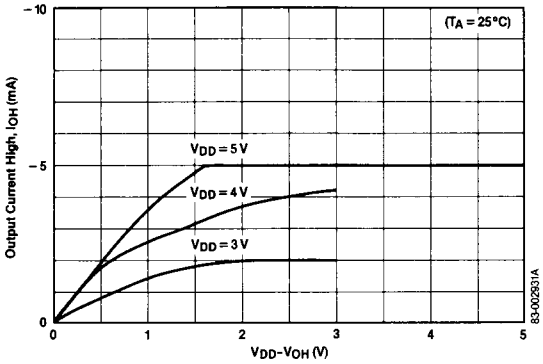


I_{DD1} vs T_A

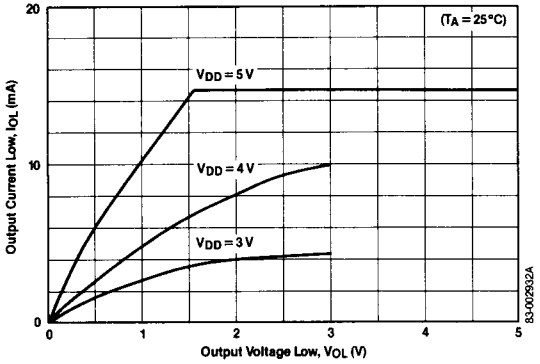


Operating Characteristics (cont)

V_{OH} vs I_{OH}



V_{OL} vs I_{OL}



Differences Between the μPD7514, μPD7508, and μPD7503

The μPD7514 integrates the features of the μPD7508 and the strengthened LCD controller/driver of the μPD7503. Differences are shown in table 7.

Table 7. Difference Between μPD7514, μPD7508, and μPD7503

	μPD7514	μPD7508C/G	μPD7503G
On-chip RAM	256×4	226×4	224×4
Input ports	Port 0 ($P0_0$–$P0_3$)	Port 0 ($P0_1$–$P0_3$) Port 1 ($P1_1$–$P1_3$)	Port 0 ($P0_1$–$P0_3$) Port 1 ($P1_1$–$P1_3$)
Output ports	Port 2 ($P2_0$–$P2_2$)	Port 2 ($P2_0$–$P2_3$)	—
I/O ports	Port 1 ($P1_0$–$P1_3$) Port 7 ($P7_0$–$P7_3$)	Port 1 ($P1_0$–$P1_3$) Port 7 ($P7_0$–$P7_3$)	—
Number of ports	31	32	23
LCD controller/driver Multiplexing	Biplexed Triplexed Quadriplexed	—	Triplexed Quadriplexed
LCD controller/driver Segments	32		24
Package	80-pin flat	40-pin DIP/ 52-pin flat	64-pin flat

3