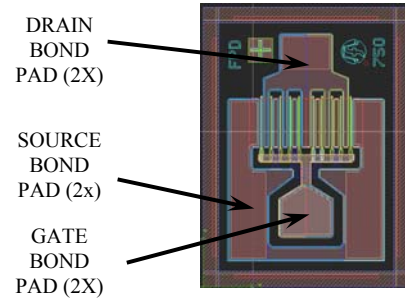


- FEATURES**

- ◆ 27 dBm Linear Output Power at 12 GHz
- ◆ 11.5 dB Power Gain at 12 GHz
- ◆ 14.5 dB Maximum Stable Gain at 12 GHz
- ◆ 38 dBm Output IP3
- ◆ 50% Power-Added Efficiency



DIE SIZE ( $\mu\text{m}$ ): 340 x 470  
 DIE THICKNESS: 75  $\mu\text{m}$   
 BONDING PADS ( $\mu\text{m}$ ): >60 x 60

- DESCRIPTION AND APPLICATIONS**

The FPD750 is an AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (PHEMT), featuring a 0.25  $\mu\text{m}$  by 750  $\mu\text{m}$  Schottky barrier gate, defined by high-resolution stepper-based photolithography. The recessed and offset Gate structure minimizes parasitics to optimize performance. The epitaxial structure and processing have been optimized for reliable high-power applications. The FPD750 also features Si<sub>3</sub>N<sub>4</sub> passivation and is available in a P100 flanged ceramic package and in the low cost plastic SOT89 and SOT343 plastic packages.

Typical applications include commercial and other narrowband and broadband high-performance amplifiers, including SATCOM uplink transmitters, PCS/Cellular low-voltage high-efficiency output amplifiers, and medium-haul digital radio transmitters.

- ELECTRICAL SPECIFICATIONS AT 22°C**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>RF SPECIFICATIONS MEASURED AT <math>f = 12</math> GHz USING CW SIGNAL</b>						
Power at 1dB Gain Compression	P <sub>1dB</sub>	V <sub>DS</sub> = 8 V; I <sub>DS</sub> = 50% I <sub>DSS</sub>	26.5	27.0		dBm
Maximum Stable Gain (S <sub>21</sub> /S <sub>12</sub> )	SSG	V <sub>DS</sub> = 8 V; I <sub>DS</sub> = 50% I <sub>DSS</sub>	13.5	14.5		dB
Power Gain at P <sub>1dB</sub>	G <sub>1dB</sub>	V <sub>DS</sub> = 8 V; I <sub>DS</sub> = 50% I <sub>DSS</sub>	10.5	11.5		dB
Power-Added Efficiency	PAE	V <sub>DS</sub> = 8 V; I <sub>DS</sub> = 50% I <sub>DSS</sub> ; P <sub>OUT</sub> = P <sub>1dB</sub>		45		%
Output Third-Order Intercept Point (from 15 to 5 dB below P <sub>1dB</sub> )	IP3	V <sub>DS</sub> = 10V; I <sub>DS</sub> = 50% I <sub>DSS</sub> Matched for optimal power Tuned for best IP3		38 40		dBm
Saturated Drain-Source Current	I <sub>DSS</sub>	V <sub>DS</sub> = 1.3 V; V <sub>GS</sub> = 0 V	185	230	280	mA
Maximum Drain-Source Current	I <sub>MAX</sub>	V <sub>DS</sub> = 1.3 V; V <sub>GS</sub> $\cong$ +1 V		370		mA
Transconductance	G <sub>M</sub>	V <sub>DS</sub> = 1.3 V; V <sub>GS</sub> = 0 V		200		mS
Gate-Source Leakage Current	I <sub>GSO</sub>	V <sub>GS</sub> = -5 V		10		$\mu\text{A}$
Pinch-Off Voltage	V <sub>p</sub>	V <sub>DS</sub> = 1.3 V; I <sub>DS</sub> = 0.75 mA		1.0		V
Gate-Source Breakdown Voltage	V <sub>BDGS</sub>	I <sub>GS</sub> = 0.75 mA	12.0	14.0		V
Gate-Drain Breakdown Voltage	V <sub>BDGD</sub>	I <sub>GD</sub> = 0.75 mA	14.5	16.0		V
Thermal Resistivity (see Notes)	$\theta_{\text{JC}}$	V <sub>DS</sub> > 6V		65		°C/W

- **ABSOLUTE MAXIMUM RATINGS\***

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	$V_{DS}$	$-3V < V_{GS} < +0V$		8	V
Gate-Source Voltage	$V_{GS}$	$0V < V_{DS} < +8V$		-3	V
Drain-Source Current	$I_{DS}$	For $V_{DS} > 2V$		$I_{DSS}$	mA
Gate Current	$I_G$	Forward or reverse current		7.5	mA
RF Input Power	$P_{IN}$	Under any acceptable bias state		175	mW
Channel Operating Temperature	$T_{CH}$	Under any acceptable bias state		175	°C
Storage Temperature	$T_{STG}$	Non-Operating Storage	-40	150	°C
Total Power Dissipation	$P_{TOT}$	See De-Rating Note below		2.3	W
Gain Compression	Comp.	Under any bias conditions		5	dB
Simultaneous Combination of Limits**		2 or more Max. Limits		80	%

\* $T_{Ambient} = 22^{\circ}C$  unless otherwise noted

\*\*Users should avoid exceeding 80% of 2 or more Limits simultaneously

Notes:

- Operating conditions that exceed the Absolute Maximum Ratings could result in permanent damage to the device.
- Thermal Resistivity specification assumes a Au/Sn eutectic die attach onto a Au-plated copper heatsink or rib.
- Power Dissipation defined as:  $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$ , where  
 $P_{DC}$ : DC Bias Power  
 $P_{IN}$ : RF Input Power  
 $P_{OUT}$ : RF Output Power
- Absolute Maximum Power Dissipation to be de-rated as follows above  $22^{\circ}C$ :  
 $P_{TOT} = 2.3W - (0.015W/^{\circ}C) \times T_{HS}$   
where  $T_{HS}$  = heatsink or ambient temperature above  $22^{\circ}C$

Example: For a  $85^{\circ}C$  heatsink temperature:  $P_{TOT} = 2.3W - (0.015 \times (85 - 22)) = 1.4W$

- **HANDLING PRECAUTIONS**

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A per ESD-STM5.1-1998, Human Body Model. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

- **ASSEMBLY INSTRUCTIONS**

The recommended die attach is gold/tin eutectic solder under a nitrogen atmosphere. Stage temperature should be  $280-290^{\circ}C$ ; maximum time at temperature is one minute. The recommended wire bond method is thermo-compression wedge bonding with 0.7 or 1.0 mil (0.018 or 0.025 mm) gold wire. Stage temperature should be  $250-260^{\circ}C$ .

- **APPLICATIONS NOTES & DESIGN DATA**

Applications Notes are available from your local Filtronic Sales Representative or directly from the factory. Complete design data, including S-parameters, noise data, and large-signal models are available on the Filtronic web site.

**All information and specifications are subject to change without notice.**