Arithmetic logic unit | 74F181

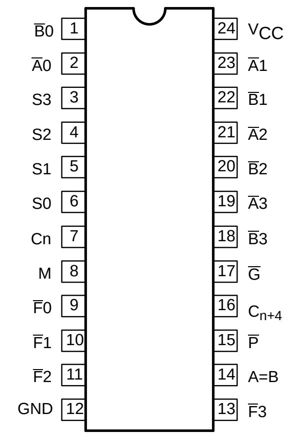
FEATURES

- Provides 16 arithmetic operation: add, subtract, compare, and double; plus 12 other arithmetic operations
- Provides all 16 logic operations of two variables: Exclusive-OR, Compare, AND, NAND, NOR, OR, plus 10 other logic operations
- Full look-ahead carry for high speed arithmetic operation on long words
- 40% faster than 'S181 with only 30% 'S181 power consumption
- Available in 300mil-wide Slim 24-pin Dual In-Line package

DESCRIPTION

The 74F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S0–S3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active-High or active-Low operands. The Function Table lists these operations.

PIN CONFIGURATION



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TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F181	7.0ns	43mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F181N
24-Pin Plastic SOL	N74F181D

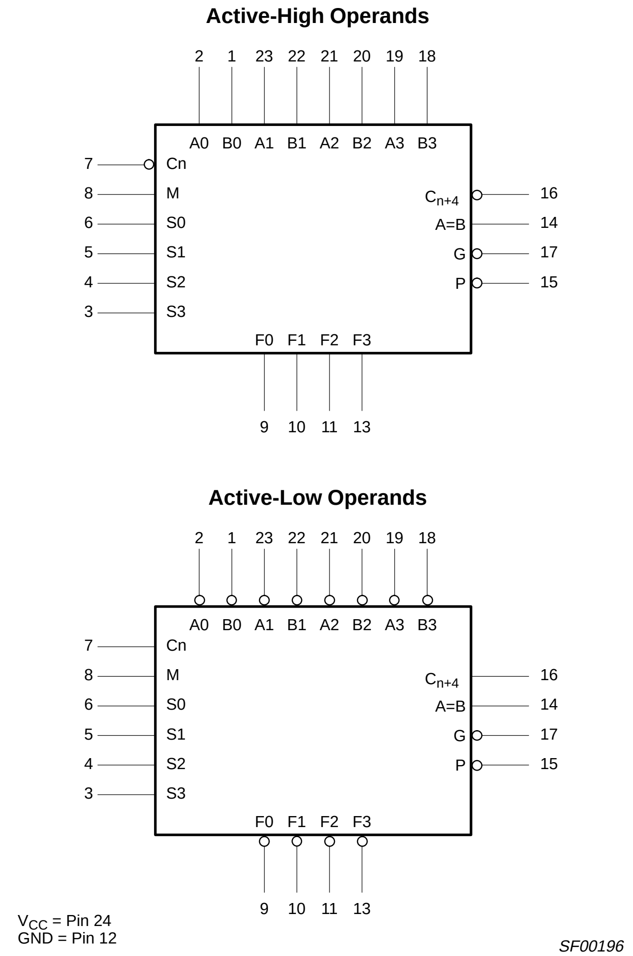
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{A}0$–$\overline{A}3$	A operand inputs	1.0/3.0	20µA/1.8mA
$\overline{B}0$–$\overline{B}3$	B operand inputs	1.0/3.0	20µA/1.8mA
M	Mode control input	1.0/1.0	20µA/0.6mA
S0–S3	Function select input	1.0/4.0	20µA/2.4mA
Cn	Carry input	1.0/5.0	20µA/3.0mA
C_{n+4}	Carry output	50/33	1.0mA/20mA
$\overline{P}$	Carry Propagate output	50/33	1.0mA/20mA
$\overline{G}$	Carry Generate output	50/33	1.0mA/20mA
A=B	Compare output	OC/33	OC/20mA
$\overline{F}0$–$\overline{F}3$	Outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC = Open Collector

Arithmetic logic unit 74F181

LOGIC SYMBOL



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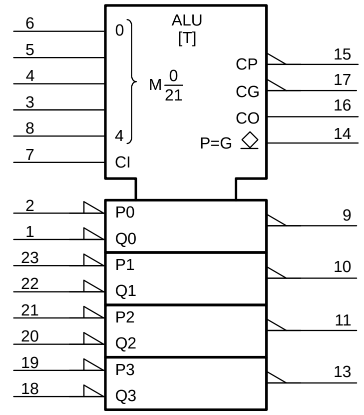
IEC/IEEE SYMBOL



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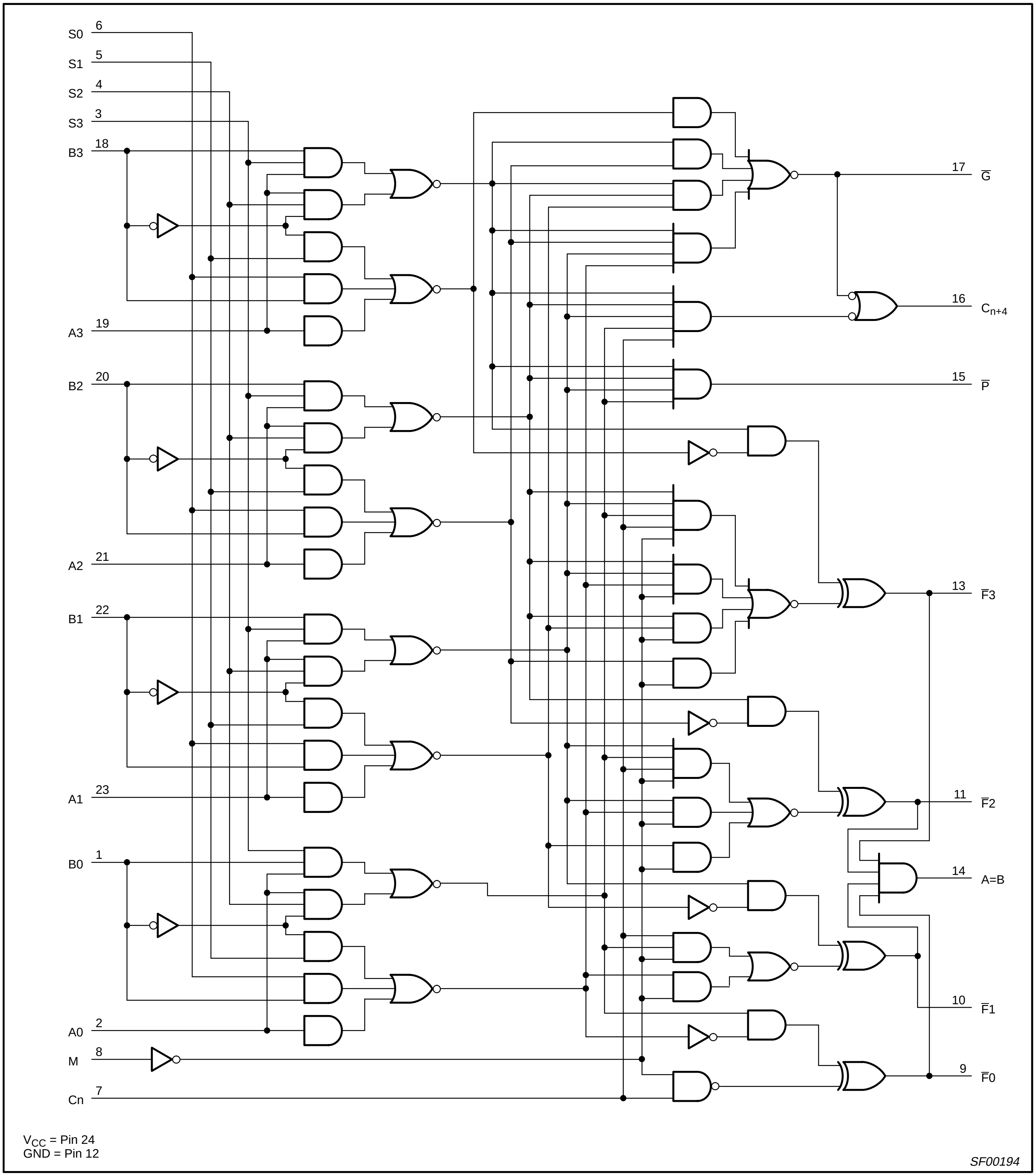
LOGIC DIAGRAM



When the Mode Control input (M) is High, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode control input is Low, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry look-ahead and provides for either ripple carry between device using the C_{n+4} output, or for carry look-ahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (Cn) of the next unit. For high-speed operation, the device is used in conjunction with the 74F182 carry look-ahead circuit. One carry look-ahead package is required for each group of four 74F181 devices. Carry look-ahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A=B output from the device goes High when all four F outputs are High and can be used to indicate logic equivalence over 4-bits when the unit is in the subtract mode. The A=B output is open-collector and can be wired-AND with other A=B outputs to give a comparison for more than 4 bits. The A=B signal can also be used with the C_{n+4} signal to indicate A>B and A<B. The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus select code LHHL generates A minus B minus 1 (two's complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (one's complement), a carry out means borrow; thus, a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active-Low inputs producing active-Low outputs or with active-High inputs producing active-High outputs. For either case, the table lists the operations that are performed to the operands labeled inside the logic symbol.

MODE-SELECT FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE HIGH INPUTS & OUTPUTS		ACTIVE LOW INPUTS & OUTPUTS	
S3	**S2**	**S1**	**S0**	**Logic (M=H)**	**Arithmetic** (M=L) (Cn=H)**	**Logic (M=H)**	**Arithmetic** (M=L) (Cn=L)**
L	L	L	L	$\overline{A}$	A	$\overline{A}$	A minus 1
L	L	L	H	$\overline{A+B}$	A+B	$\overline{AB}$	AB minus 1
L	L	H	L	$\overline{A}B$	$A+\overline{B}$	$\overline{A}+B$	$A\overline{B}$ minus 1
L	L	H	H	Logical 0	minus 1	Logical 1	minus 1
L	H	L	L	$\overline{AB}$	A plus $A\overline{B}$	$\overline{A+B}$	A plus $(A+\overline{B})$
L	H	L	H	$\overline{B}$	(A+B) plus $A\overline{B}$	$\overline{B}$	AB plus $(A+\overline{B})$
L	H	H	L	$A \oplus B$	A minus B minus 1	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	$A\overline{B}$	AB minus 1	$A+\overline{B}$	$A+\overline{B}$
H	L	L	L	$\overline{A}+B$	A plus AB	$\overline{A}B$	A plus (A+B)
H	L	L	H	$\overline{A \oplus B}$	A plus B	$A \oplus B$	A plus B
H	L	H	L	B	$(A+\overline{B})$ plus AB	B	$A\overline{B}$ plus (A+B)
H	L	H	H	AB	AB minus 1	A+B	A+B
H	H	L	L	Logical 1	A plus A*	Logical 0	A plus A*
H	H	L	H	$A+\overline{B}$	(A+B) plus A	$A\overline{B}$	AB plus A
H	H	H	L	A+B	$(A+\overline{B})$ plus A	AB	$A\overline{B}$ plus A
H	H	H	H	A	A minus 1	A	A

H = High voltage level
L = Low voltage level
* = Each bit is shifted to the next more significant position.
** = Arithmetic operations expressed in two's complement notation.

Table 1. Sum Mode Test

Function Inputs: S0 = S3 = 4.5V, S1 = S2 = M = 0V

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	Cn	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	Cn	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, Cn	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, Cn	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, Cn	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, Cn	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, Cn	C_{n+4}
t_{PLH}, t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, Cn	C_{n+4}
t_{PLH}, t_{PHL}	Cn	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

Table 2. Diff Mode Test

Function Inputs: S1 = S2 = 4.5V, S0 = S3 = M = 0V

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, Cn	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, Cn	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$, $\overline{B}$, Cn	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, Cn	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, Cn	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$, $\overline{B}$, Cn	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, Cn	A=B
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, Cn	A=B
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, Cn	C_{n+4}
t_{PLH}, t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$, $\overline{B}$, Cn	C_{n+4}
t_{PLH}, t_{PHL}	Cn	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}

Table 3. Logic Mode Test

Function Inputs: S1 = S2 = 4.5V, S0 = S3 = 0V

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, Cn	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, Cn	$\overline{F}_i$

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

Arithmetic logic unit — 74F181

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS MIN	LIMITS NOM	LIMITS MAX	UNIT
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
V_{OH}	High level output voltage	A=B only			4.5	V
I_{OH}	High-level output current	Any output except A=B			–1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free-air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT
I_{OH}	High-level output current	A=B only	V_{CC} = MIN, V_{IL} = MAX; V_{IH} = MIN, V_{OH} = MAX					250	µA
V_{OH}	High-level output voltage	Any output except A=B	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	M	V_{CC} = MAX, V_I = 0.5V					–0.6	mA
		$\overline{A}0$–$\overline{A}3$, $\overline{B}0$–$\overline{B}3$						–1.8	mA
		S0–S3						–2.4	mA
		Cn						–3.0	mA
I_{OS}	Short-circuit output current[3]	Any output except A=B	V_{CC} = MAX			–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	S0–S3=M=$\overline{A}0$–$\overline{A}3$=4.5V, $\overline{B}0$–$\overline{B}3$=Cn=GND			43	65	mA
		I_{CCL}		S0–S3=M=4.5V, $\overline{B}0$–$\overline{B}3$=Cn=$\overline{A}0$–$\overline{A}3$=GND			43	65	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS				LIMITS					UNIT
						V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF R_L = 500Ω		
		Mode	Table	Waveform	Condition	MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Cn to C_{n+4}	Sum Diff	1 2	1	M=0V	3.0 2.5	5.0 5.0	8.0 8.0	3.0 2.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$n or $\overline{B}$n to C_{n+4}	Sum	1	2	M=S1=S2=0V, S0=S3=4.5V	5.0 5.0	9.0 8.0	12.0 12.0	5.0 5.0	13.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$n or $\overline{B}$n to C_{n+4}	Diff	2	2	M=S0=S3=0V, S1=S2=4.5V	5.0 5.0	9.5 8.0	13.0 12.0	5.0 5.0	14.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay Cn to $\overline{F}$n	Diff Sum	2 1	1	M=0V	3.0 3.0	5.0 5.0	8.0 8.0	3.0 2.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$n or $\overline{B}$n to $\overline{G}$	Sum	1	1	M=S1=S2=0V, S0=S3=4.5V	3.0 3.0	5.0 5.0	7.5 7.5	2.5 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$n or $\overline{B}$n to $\overline{G}$	Diff	2	2	M=S0=S3=0V, S1=S2=4.5V	3.0 3.0	4.5 5.0	8.0 8.5	2.5 2.5	9.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$n or $\overline{B}$n to $\overline{P}$	Sum	1	2	M=S1=S2=0V, S0=S3=4.5V	2.5 3.0	4.0 4.5	7.0 7.5	2.0 2.5	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$n or $\overline{B}$n to $\overline{P}$	Diff	2	1, 2	M=S0=S3=0V, S1=S2=4.5V	2.5 3.0	4.0 5.0	7.5 8.5	2.0 2.5	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Sum	1	1, 2	M=S1=S2=0V, S0=S3=4.5V	3.0 3.0	4.5 4.5	7.5 7.5	2.5 3.0	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Diff	2	1, 2	M=S0=S3=0V, S1=S2=4.5V	3.0 3.0	4.5 5.0	8.5 8.5	2.5 3.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$n or $\overline{B}$n to Fn	Sum		1, 2		3.5 3.5	6.0 5.5	10.0 9.5	3.0 3.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$n or $\overline{B}$n to Fn	Diff		1, 2		4.0 4.5	6.5 7.0	10.5 10.5	3.5 4.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Logic	3	1, 2	M=4.5V	3.5 3.5	5.5 5.5	9.0 10.0	3.0 3.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$n or $\overline{B}$n to A=B	Diff	2	1, 2	M=S0=S3=0V, S1=S2=4.5V	10.0 6.0	14.0 8.5	19.0 12.5	9.5 5.5	20.5 12.5	ns

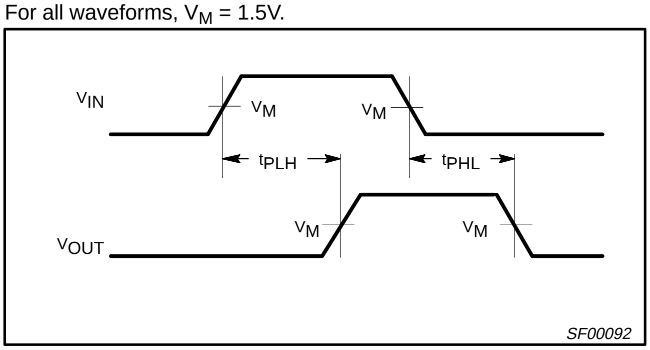
NOTES:
"$\overline{A}$n or $\overline{B}$n to Fn" means any $\overline{A}$ or any $\overline{B}$ to any $\overline{F}$; "$\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$" means $\overline{A}$1, $\overline{B}$1 to $\overline{F}$1; $\overline{A}$2, $\overline{B}$2 to $\overline{F}$2 (the identifying number must be the same).

AC ELECTRICAL CHARACTERISTICS

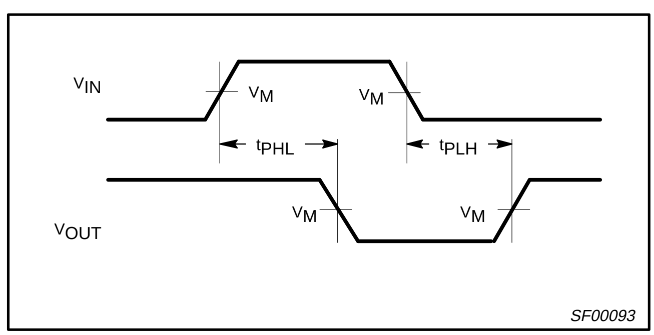
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF R_L = 500Ω		
		Mode	Waveform	MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{F}_i$ (Inverting)		1	3.5 3.5	5.5 5.0	8.0 8.0	3.0 3.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{F}_i$ (Non-Inverting)		2	3.0 3.0	5.5 5.5	8.5 8.5	3.0 3.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_i to A=B (Inverting)		1	10.5 6.0	16.5 8.0	22.5 11.0	10.5 6.0	24.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay S_i to A=B (Non-Inverting)		2	10.0 5.5	15.0 8.5	19.0 12.5	10.0 5.0	21.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay S_i to C_{n+4} (Inverting)		1	3.5 3.0	7.0 5.5	11.0 10.0	3.0 2.5	12.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{G}$ (Non-Inverting)		2	2.5 2.5	5.0 4.0	7.5 7.5	2.5 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{P}$ (Non-Inverting)		2	2.5 2.5	4.0 4.5	6.5 7.0	2.5 2.5	7.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_i$ (Inverting)	Sum	1	3.5 3.5	6.0 6.0	8.5 8.5	3.5 3.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_i$ (Non-Inverting)	Sum	2	4.5 4.0	7.0 6.0	10.0 9.5	4.5 4.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_i$ (Inverting)	Diff	1	3.5 3.5	6.0 6.0	8.5 8.5	3.5 3.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_i$ (Non-Inverting)	Diff	2	4.0 4.0	7.0 6.0	10.0 9.5	4.0 4.0	11.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B (Inverting)	Sum	1	12.0 6.5	16.0 8.0	20.0 11.0	11.0 6.0	22.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B (Non-Inverting)	Sum	2	13.0 6.5	17.0 8.0	21.0 10.5	12.0 6.0	24.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B (Inverting)	Diff	1	11.5 6.0	16.0 8.0	20.0 10.5	10.5 6.0	22.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B (Non-Inverting)	Diff	2	13.0 6.0	17.0 8.0	21.5 11.0	12.5 6.0	24.0 11.5	ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V.



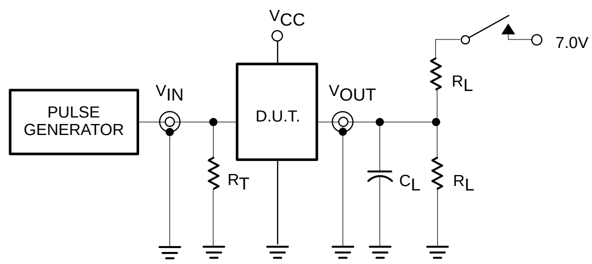
Waveform 1. Propagation Delay for Non-Inverting Paths



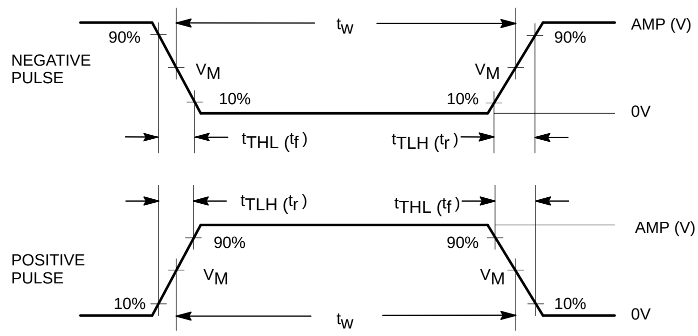
Waveform 2. Propagation Delay for Inverting Paths

Arithmetic logic unit　　74F181

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
Open Collector	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00195