

6.3A, 30V, Avalanche Rated, Single N-Channel LittleFET™ Enhancement Mode Power MOSFET

January 1997

Features

- 6.3A, 30V
- $r_{DS(ON)} = 0.030\Omega$
- *Temperature Compensating PSPICE Model*
- *Peak Current vs Pulse Width Curve*
- *UIS Rating Curve*

Ordering Information

PART NUMBER	PACKAGE	BRAND
RF1K49157	MS-012AA	RF1K49157

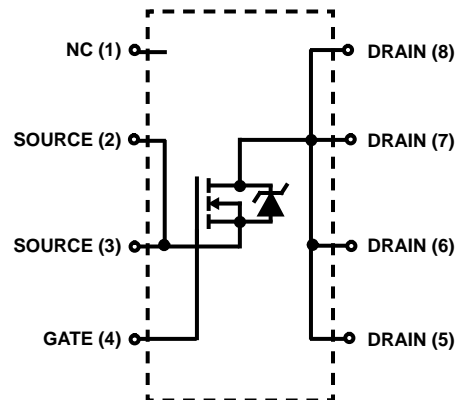
NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e., RF1K4915796.

Description

The RF1K49157 Single N-Channel power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It was designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low voltage bus switches. This device can be operated directly from integrated circuits.

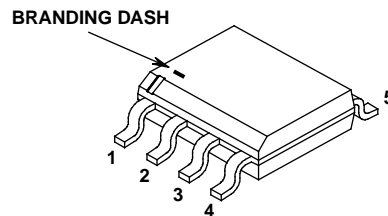
Formerly developmental type TA49157.

Symbol



Packaging

JEDEC MS-012AA



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RF1K49157

Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ Unless Otherwise Specified

	RF1K49157	UNITS
Drain to Source Voltage	30	V
Drain to Gate Voltage	30	V
Gate to Source Voltage	± 20	V
Drain Current		
Continuous (Pulse width = 1s)	6.3	A
Pulsed	I _{DM}	Refer to Peak Current Curve
Pulsed Avalanche Rating	E _{AS}	Refer to UIS Curve
Power Dissipation		
$T_A = 25^\circ\text{C}$	2	W
Derate Above 25°C	0.016	W/ $^\circ\text{C}$
Operating and Storage Temperature	T_{STG}, T_J	-55 to 150
Soldering Temperature of Leads for 10s	T_L	260

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_A = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250 μ A, V _{GS} = 0V	30	-	-	V	
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μ A	1	-	3	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V	T _A = 25 $^\circ\text{C}$	-	-	1	μ A
			T _A = 150 $^\circ\text{C}$	-	-	50	μ A
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ± 20 V	-	-	100	nA	
On Resistance	r _{DS(ON)}	I _D = 6.3A	V _{GS} = 10V	-	-	0.030	Ω
			V _{GS} = 4.5V	-	-	0.060	Ω
Turn-On Time	t _{ON}	V _{DD} = 15V, I _D = 6.3A, R _L = 2.38 Ω , V _{GS} = 10V, R _{GS} = 25 Ω	-	-	85	ns	
Turn-On Delay Time	t _{d(ON)}		-	22	-	ns	
Rise Time	t _r		-	43	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	125	-	ns	
Fall Time	t _f		-	85	-	ns	
Turn-Off Time	t _{OFF}		-	-	-	265	ns
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 20V	V _{DD} = 24V, I _D = 6.3A, R _L = 3.81 Ω	-	70	88	nC
Gate Charge at 10V	Q _{g(10)}	V _{GS} = 0V to 10V		-	38	48	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 2V		-	2.8	3.5	nC
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz	-	1575	-	pF	
Output Capacitance	C _{OSS}		-	700	-	pF	
Reverse Transfer Capacitance	C _{RSS}		-	200	-	pF	
Thermal Resistance Junction-to-Ambient	R $_{\theta JA}$	Pulse width = 1s Device mounted on FR-4 material	-	-	62.5	$^\circ\text{C}/\text{W}$	

Source to Drain Diode Ratings and Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V _{SD}	I _{SD} = 6.3A	-	-	1.25	V
Reverse Recovery Time	t _{rr}	I _{SD} = 6.3A, dI _{SD} /dt = 100A/ μ s	-	-	60	ns

Typical Performance Curves

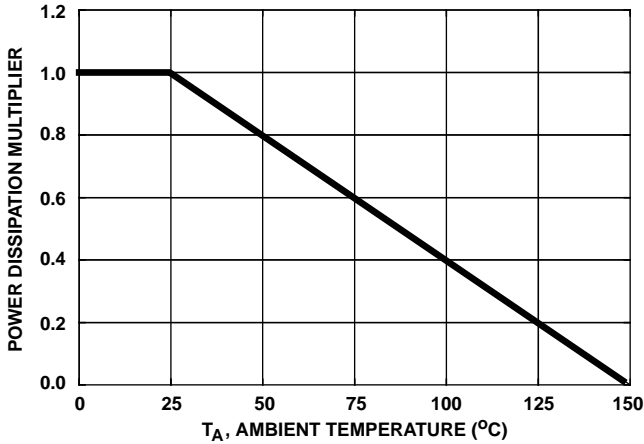


FIGURE 1. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

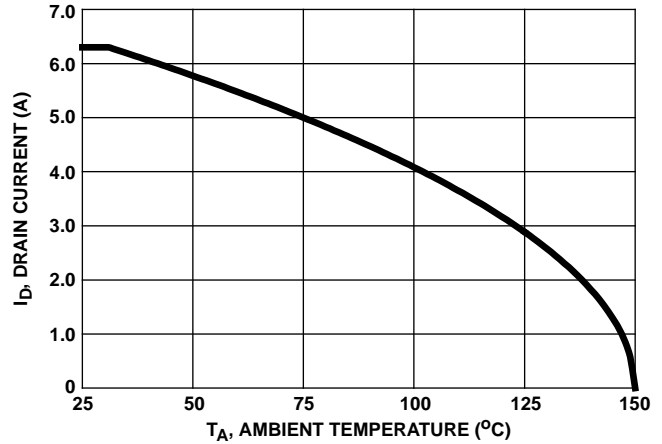


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

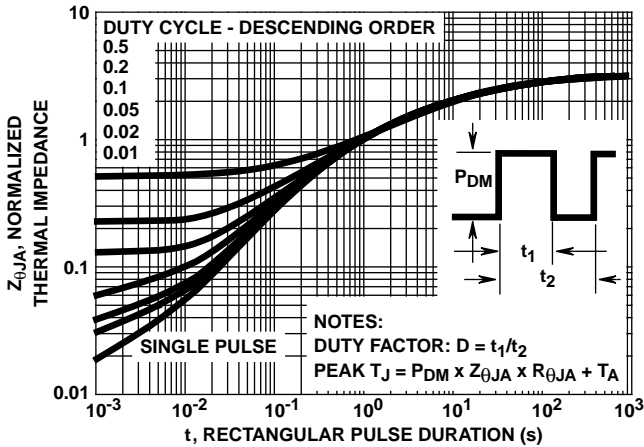


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

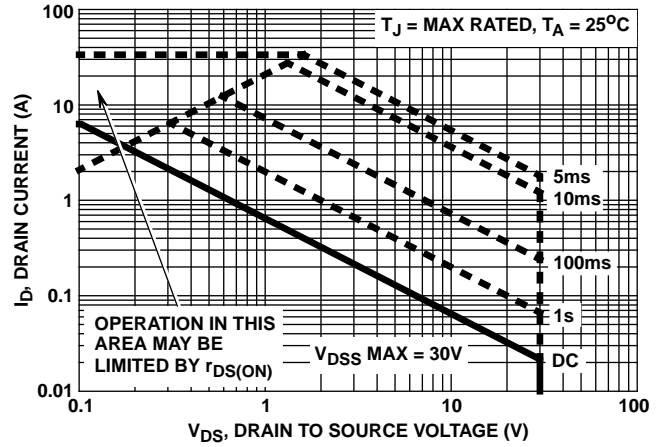


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

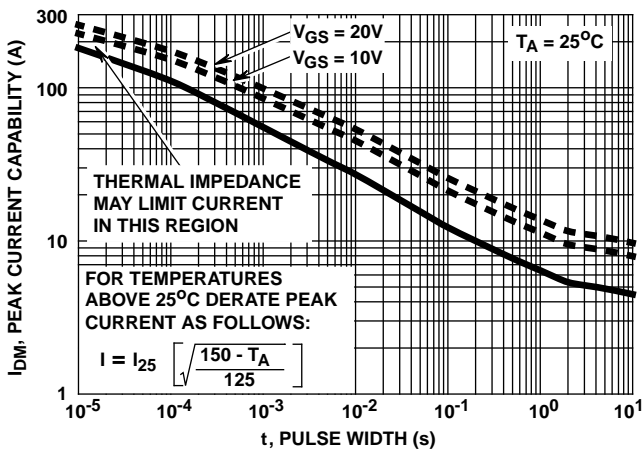
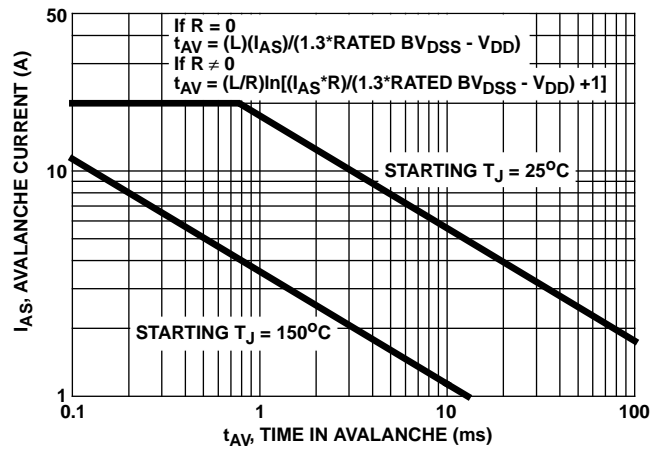


FIGURE 5. PEAK CURRENT CAPABILITY



NOTE: Refer to Harris Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

Typical Performance Curves (Continued)

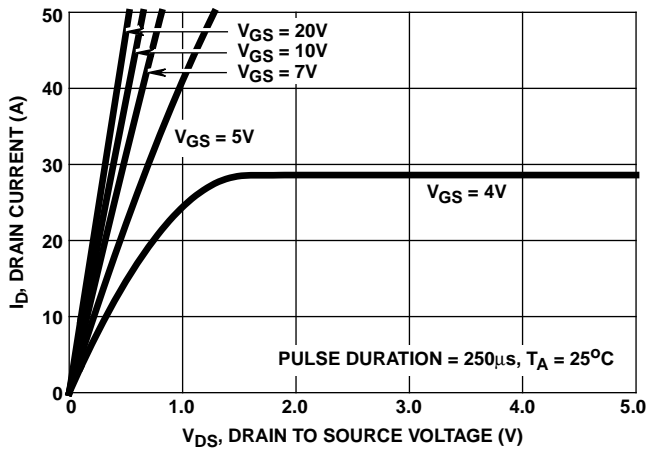


FIGURE 7. SATURATION CHARACTERISTICS

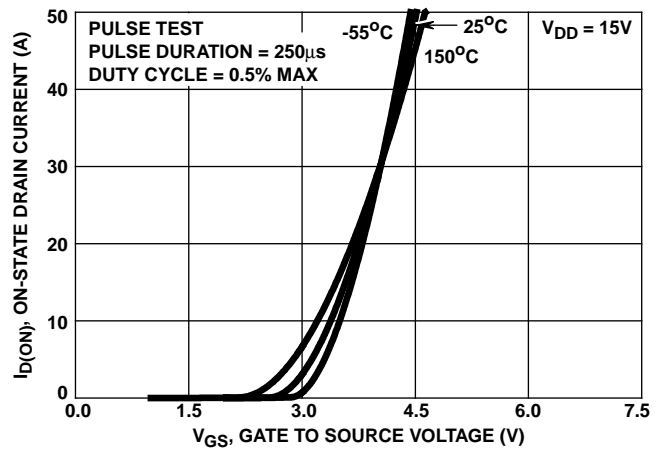


FIGURE 8. TRANSFER CHARACTERISTICS

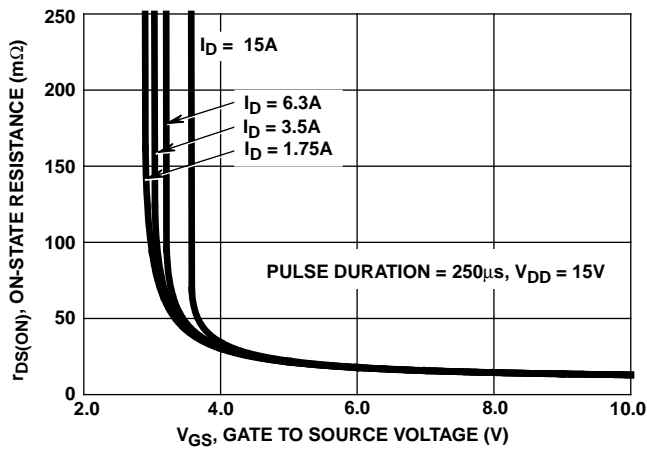


FIGURE 9. $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

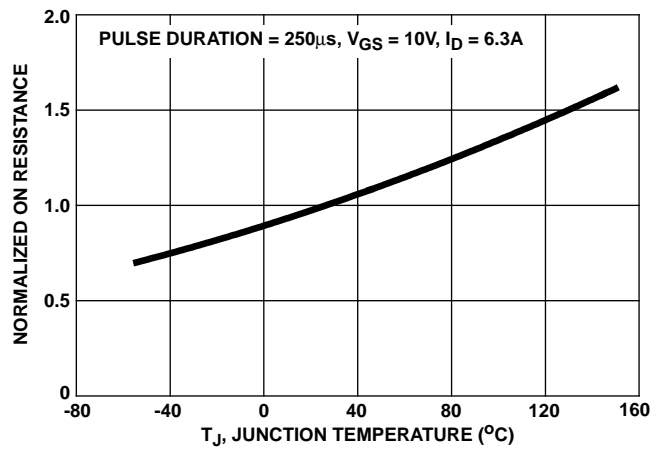


FIGURE 10. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

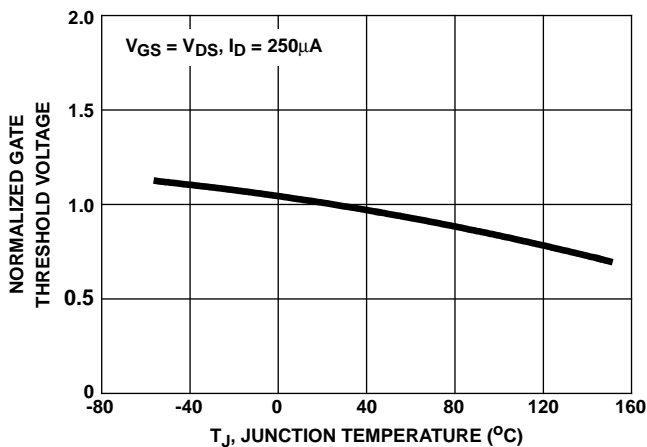


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

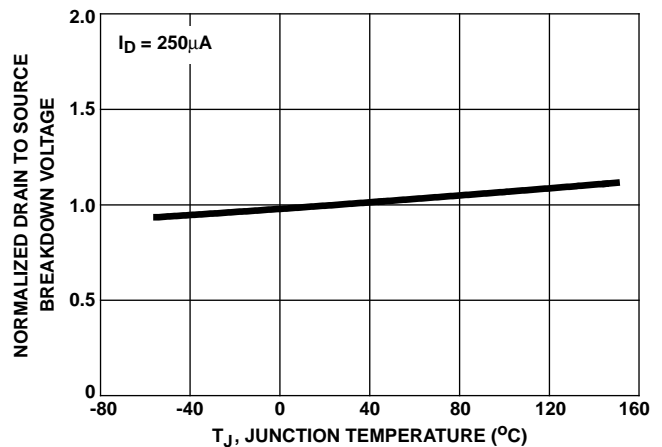


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

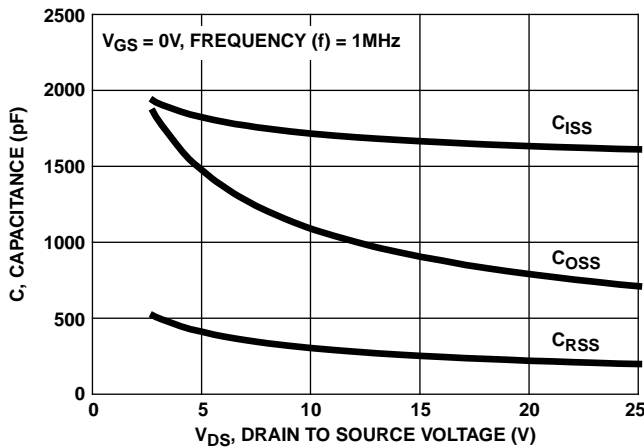
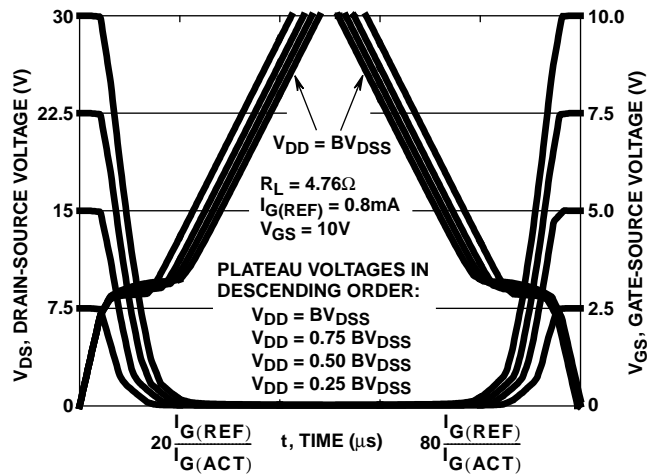


FIGURE 13. CAPACITANCE vs VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 14. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

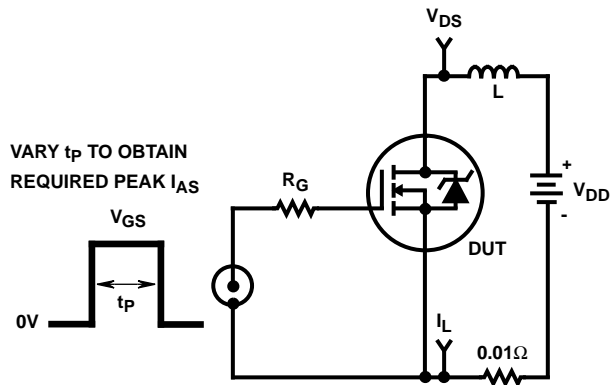


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

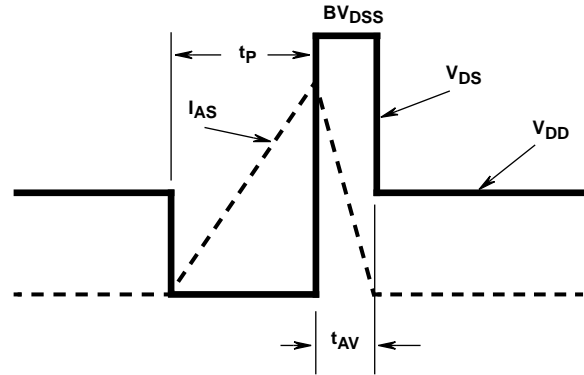


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

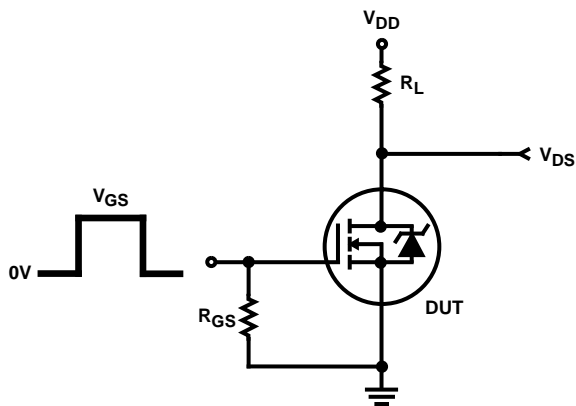


FIGURE 17. RESISTIVE SWITCHING TEST CIRCUIT

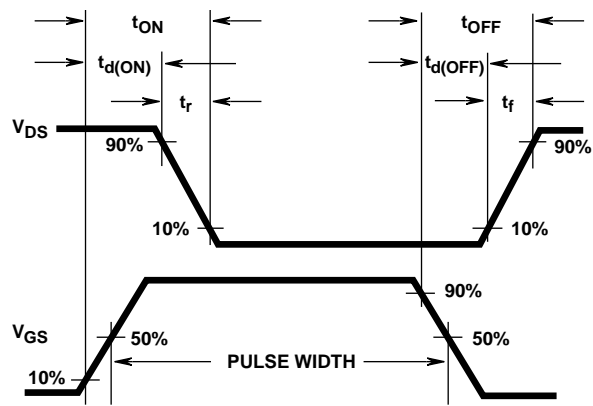


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

Soldering Precautions

The soldering process creates a considerable thermal stress on any semiconductor component. The melting temperature of solder is higher than the maximum rated temperature of the device. The amount of time the device is heated to a high temperature should be minimized to assure device reliability. Therefore, the following precautions should always be observed in order to minimize the thermal stress to which the devices are subjected.

1. Always preheat the device.
2. The delta temperature between the preheat and soldering should always be less than 100°C. Failure to preheat the device can result in excessive thermal stress which can damage the device.
3. The maximum temperature gradient should be less than 5°C per second when changing from preheating to soldering.
4. The peak temperature in the soldering process should be at least 30°C higher than the melting point of the solder chosen.
5. The maximum soldering temperature and time must not exceed 260°C for 10 seconds on the leads and case of the device.
6. After soldering is complete, the device should be allowed to cool naturally for at least three minutes, as forced cooling will increase the temperature gradient and may result in latent failure due to mechanical stress.
7. During cooling, mechanical stress or shock should be avoided.

RF1K49157

Temperature Compensated PSPICE Model for the RF1K49157

SUBCKT RF1K49157 2 1 3 ; rev 3/14/95

CA 12 8 1.834e-9
 CB 15 14 1.72e-9
 CIN 6 8 1.416e-9

DBODY 7 5 DBDMOD
 DBREAK 5 11 DBREAKMOD
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 34.89
 EDS 14 8 5 8 1
 EGS 13 8 6 8 1
 ESG 6 10 6 8 1
 EVTHRESH 6 21 19 8 1
 EZTEMPCO 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1.0e-9
 LGATE 1 9 1.04e-9
 LSOURCE 3 7 0.237e-9

MOS1 16 6 8 8 MSTRONG M = 0.99
 MOS2 16 21 8 8 MWEAK M = 0.01

RBREAK 17 18 RBREAKMOD 1
 RDRAIN 5 16 RDRAINMOD 4.39e-3
 RGATE 9 20 1.53
 RIN 6 8 1e9
 RLDRAIN 2 5 1.0
 RLGATE 1 9 10.4
 RLSOURCE 3 7 0.237
 RSOURCE 8 7 RSOURCEMOD 4.44e-3
 RTHRESH 22 8 RTHRESHMOD 1
 RZTEMPCO 18 19 RZTEMPCOMOD 1

S1A 6 12 13 8 S1AMOD
 S1B 13 12 13 8 S1BMOD
 S2A 6 15 14 13 S2AMOD
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

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.MODEL DBDMOD D (IS = 1.14e-12 RS = 6.01e-3 TRS1 = 1.05e-4 TRS2 = -2.46e-5 CJO = 2.62e-9 TT = 2.44e-8)
.MODEL DBREAKMOD D (RS = 4.89e-1 TRS1 = 2.11e-3 TRS2 = -3.19e-6)
.MODEL DPLCAPMOD D (CJO = 1.007e-9 IS = 1e-30 N = 10)
.MODEL MSTRONG NMOS (VTO = 2.567 KP = 33.21 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAK NMOS (VTO = 2.0225 KP = 33.21 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBREAKMOD RES (TC1 = 9.59e-4 TC2 = -2.87e-7)
.MODEL RDRAINMOD RES (TC1 = 8.08e-3 TC2 = 1.6e-5)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RTHRESHMOD RES (TC1 = -6.4e-4 TC2 = -8.1e-6)
.MODEL RZTEMPCOMOD RES (TC1 = -2.43e-3 TC2 = 1.57e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.47 VOFF = -4.47)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.47 VOFF = -6.47)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.3 VOFF = 1.7)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.7 VOFF = -3.3)
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.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991.

