

Features

- Single chip solution with only a few external components
- Stand-alone fixed-frequency transceiver operation modes
- Programmable multi-channel transceiver operation modes
- Low current consumption in active mode and very low standby current
- PLL-stabilized RF VCO (LO) with external varactor diode
- Lock detection in programmable channel applications
- 3wire bus serial control interface
- FSK/ASK modulation selection
- FSK for digital data and FM for analog signal reception
- RSSI allows signal strength indication and ASK detection
- Switchable LNA gain for improved dynamic range
- Automatic PA turn-on after PLL lock
- FM possible with external varactor
- ASK modulation achieved by on/off keying
- AFC option for extended input frequency acceptance range
- Surface mount package LQFP32

Ordering Information

| Part No. (Engineering Samples) | Temperature Code | Package Code |
|---------------------------------------|-------------------------|---------------------|
| TH7121 (TH7120-02) | E (-40 °C to 85 °C) | NE (LQFP32) |

Application Examples

- General bi-directional half duplex digital data transmission or analog signal transmission
- Low-power telemetry
- Alarm and security systems
- Keyless car and central locking
- Domotics
- Model control

Technical Data Overview

- Frequency range: 300 MHz to 930 MHz for programmable channel applications
- 315 MHz, 433 MHz, 868 MHz or 915 MHz fixed-frequency single-channel variants
- Power supply range: 2.5 V to 5.5 V
- Temperature range: -40 °C to +85 °C
- Standby current: 50 nA
- Operating current: 6.0 mA in receive mode at low gain
- Operating current 9.0 mA in transmit mode at 0 dBm output power
- Adjustable output power range from -15 dBm to +6 dBm
- Sensitivity: -103 dBm at FSK with 150 kHz IF filter BW
- Sensitivity: -105 dBm at ASK with 150 kHz IF filter BW
- Maximum data rate for FSK and ASK: 60 kbit/s NRZ
- Maximum input level: -10 dBm at FSK and -20 dBm at ASK
- Input frequency acceptance: ± 50 kHz (with AFC option)
- Frequency deviation range: ± 5 kHz to ± 100 kHz
- Maximum analog modulation frequency: 20 kHz
- 3 MHz to 12 MHz crystal reference

General Description

The TH7120 is a single chip FSK/FM/ASK transceiver IC. It is designed to operate in low-power multi-channel programmable or single-channel stand-alone, half-duplex data transmission systems. It can be used for ISM, SRD or any other application operating in the frequency ranging of 300 MHz to 930 MHz.

The TH7120 transceiver IC consists of the following building blocks:

- Low-noise amplifier (LNA) for high-sensitivity RF signal reception with switchable gain
- Mixer (MIX) for RF-to-IF down-conversion
- IF amplifier (IFA) to amplify and limit the IF signal and for RSSI generation
- Phase-coincidence demodulator with external ceramic discriminator (FSK Demodulator)
- Operational amplifier, connected to demodulator output (OA1)
- Operational amplifier, integrator circuit at FSK-AFC mode (OA2)
- Control logic with 3wire bus serial control interface (SCI)
- Reference oscillator (RO) with external crystal
- Reference divider (R counter)
- Programmable divider (N/A counter)
- Phase-frequency detector (PFD)
- Charge pump (CP)
- Voltage control oscillator (VCO) with internal varactor
- Power amplifier (PA) with adjustable output power

The transceiver can be used either as a 3wire-bus-controlled programmable or as a stand-alone fixed-frequency device. After power up, the transceiver is set to fixed-frequency mode. In this mode, pins FS0/SDEN and FS1/LD must be connected to V_{EE} or V_{CC} in order to set the desired frequency of operation. The logic levels at pins FS0/SDEN and FS1/LD must not be changed after power up in order to remain in fixed-frequency mode.

| Channel frequency | 433.92 MHz | 868.3 MHz | 315.0 MHz | 915.0 MHz |
|-------------------|------------|-----------|-----------|-----------|
| FS0/SDEN | 1 | 0 | 1 | 0 |
| FS1/LD | 0 | 0 | 1 | 1 |

After the first logic level change at pin FS0/SDEN, the transceiver enters into programmable mode while pin FS1/LD is now a PLL lock detector output. In this mode, the user can set any PLL frequency or mode of operation by the SCI.

In the fixed-frequency mode, the user can set the transceiver to Standby, Receive, Transmit or Idle (only PLL synthesizer active) mode via control pins RE/SCLK and TE/SDTA.

| Operation mode | Standby | Receive | Transmit | Idle |
|----------------|---------|---------|----------|------|
| RE/SCLK | 0 | 1 | 0 | 1 |
| TE/SDTA | 0 | 0 | 1 | 1 |

Block Diagram

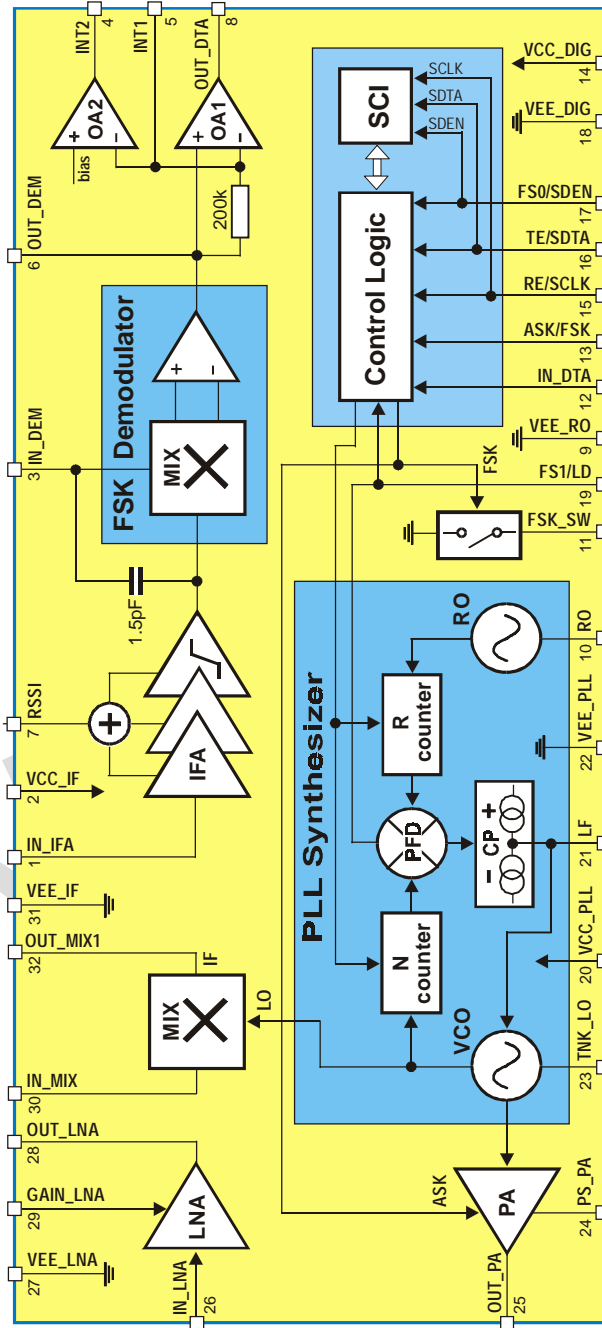
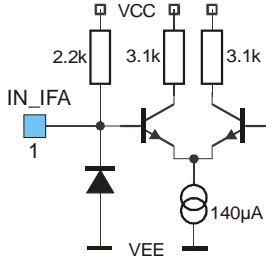
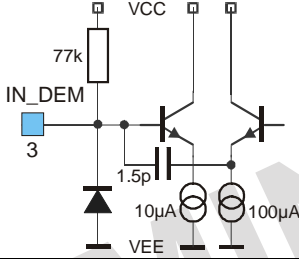
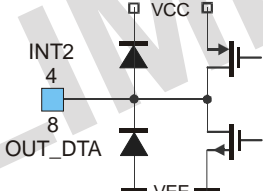
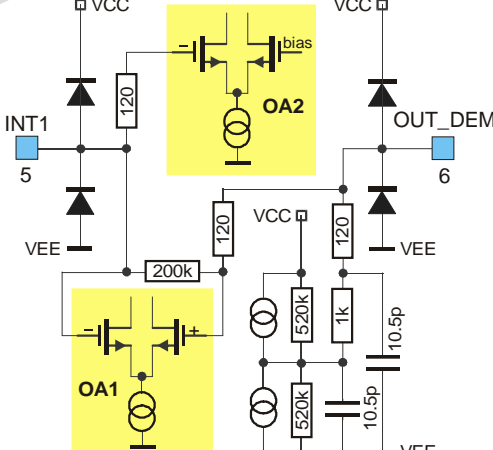
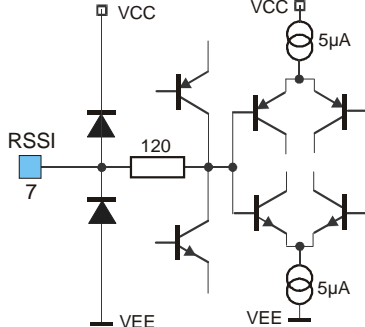
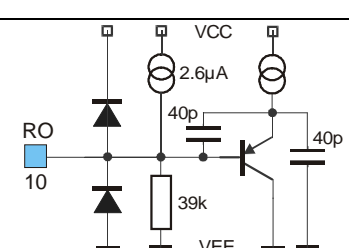
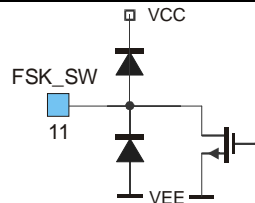
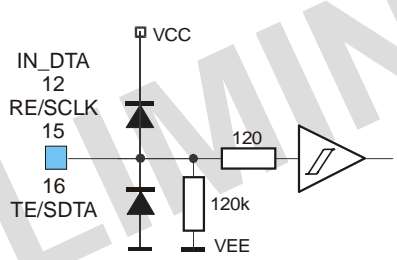
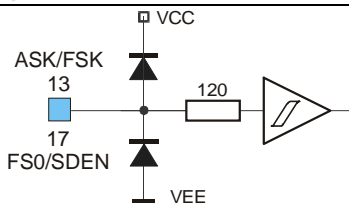
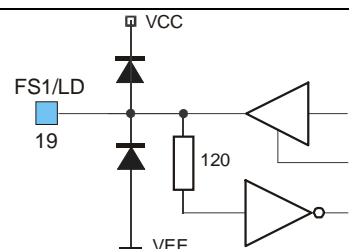
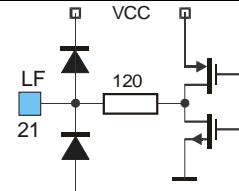
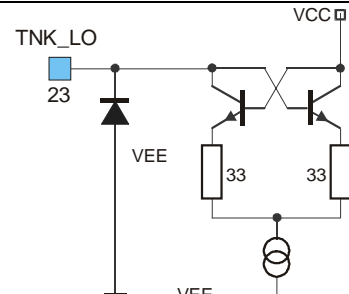
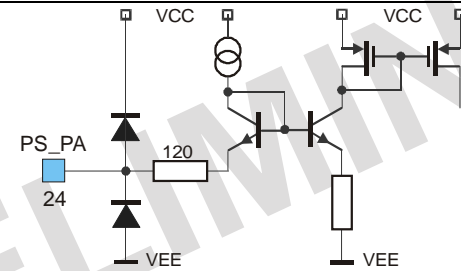
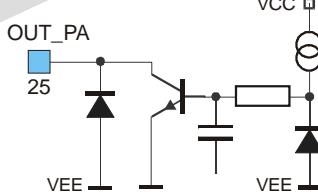
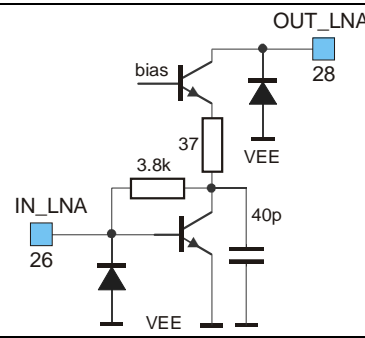
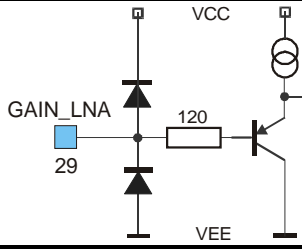


Figure 1: TH7121 block diagram

Pin Definition and Description

| Pin No. | Name | I/O Type | Functional Schematic | Description |
|---------|---------|------------|--|---|
| 1 | IN_IFA | input |  | IF amplifier input, approx. 2 kΩ single-ended |
| 2 | VCC_IF | supply | | positive supply of LNA, MIX, IFA, FSK Demodulator, PA, OA1 and OA2 |
| 3 | IN_DEM | analog I/O |  | IF amplifier output and demodulator input, connection to external ceramic discriminator |
| 4 | INT2 | output |  | integrator output OA2 |
| 8 | OUT_DTA | output | | output OA1 |
| 5 | INT1 | input |  | inverting inputs OA1 and OA2 |
| 6 | OUT_DEM | analog I/O | | demodulator output and non-inverting input OA1 |
| 7 | RSSI | output |  | RSSI output |

| Pin No. | Name | I/O Type | Functional Schematic | Description |
|---------|----------|------------|---|--|
| 9 | VEE_RO | ground | | ground of RO |
| 10 | RO | analog I/O |  | RO input, base of bipolar transistor |
| 11 | FSK_SW | analog I/O |  | FSK pulling pin, switch to ground or OPEN |
| 12 | IN_DTA | input |  | ASK/FSK modulation data input, pull down resistor 120kΩ |
| 15 | RE/SCLK | input | | receiver enable input / clock input for the shift register, pull down resistor 120kΩ |
| 16 | TE/SDTA | input | | transmitter enable input / serial data input, pull down resistor 120kΩ |
| 13 | ASK/FSK | input |  | ASK/FSK mode select input |
| 17 | FS0/SDEN | input | | frequency select input / serial data enable input |
| 14 | VCC_DIG | supply | | positive supply of serial port and control logic |
| 18 | VEE_DIG | ground | | ground of serial port and control logic |
| 19 | FS1/LD | input |  | frequency select input / lock detector output |
| 20 | VCC_PLL | supply | | positive supply of PLL frequency synthesizer |
| 22 | VEE_PLL | ground | | ground of PLL frequency synthesizer |

| Pin No. | Name | I/O Type | Functional Schematic | Description |
|---------|----------|------------|--|---|
| 21 | LF | analog I/O |  | charge pump output, connection to external loop filter |
| 23 | TNK_LO | analog I/O |  | VCO open-collector output, connection to external LC tank |
| 24 | PS_PA | analog I/O |  | power-setting input |
| 25 | OUT_PA | output |  | power amplifier open-collector output |
| 27 | VEE_LNA | ground | | ground of LNA and PA |
| 28 | OUT_LNA | output |  | LNA open-collector output, connection to external LC tank at RF |
| 26 | IN_LNA | input | | LNA input, approx. 50Ω single-ended |
| 29 | GAIN_LNA | input |  | LNA gain control input |

| Pin No. | Name | I/O Type | Functional Schematic | Description |
|---------|---------|----------|----------------------|---|
| 30 | IN_MIX | input | | mixer input, approx. 200Ω single-ended |
| 31 | VEE_IF | ground | | ground of IFA, Demodulator, OA1 and OA2 |
| 32 | OUT_MIX | output | | mixer output, approx. 330Ω single-ended |

PRELIMINARY

Stand-Alone Fixed-Frequency Operation

After power up the transceiver is set to fixed-frequency mode. In this mode, pins FS0/SDEN and FS1/LD must be connected to V_{EE} or V_{CC} to set the desired frequency of operation. The logic levels at pins FS0/SDEN and FS1/LD must not be changed after power up in order to remain in fixed-frequency mode. The default settings of the control word bits in stand-alone mode are described in the frequency selection table.

Frequency Selection

| Channel frequency | 433.92 MHz | 868.3 MHz | 315 MHz | 915 MHz |
|--------------------------------|------------|------------|------------|------------|
| FS0/SDEN | 1 | 0 | 1 | 0 |
| FS1/LD | 0 | 0 | 1 | 1 |
| Reference oscillator frequency | 7.1505 MHz | | | |
| R counter ratio in RX mode | 16 | 16 | 18 | 30 |
| PFD frequency in RX mode | 446.91 kHz | 446.91 kHz | 397.25 kHz | 238.35 kHz |
| N/A counter ratio in RX mode | 947 | 1919 | 766 | 3794 |
| VCO frequency in RX mode | 423.22 MHz | 857.60 MHz | 304.30 MHz | 904.30 MHz |
| RX frequency | 433.92 MHz | 868.30 MHz | 315.00 MHz | 915.00 MHz |
| R counter ratio in TX mode | 16 | 16 | 18 | 30 |
| PFD frequency in TX mode | 446.91 kHz | 446.91 kHz | 397.25 kHz | 238.35 kHz |
| N/A counter ratio in TX mode | 971 | 1943 | 793 | 3839 |
| VCO frequency in TX mode | 433.92 MHz | 868.30 MHz | 315.00 MHz | 915.00 MHz |
| TX frequency | 433.92 MHz | 868.30 MHz | 315.00 MHz | 915.00 MHz |
| IF frequency in RX mode | 10.7 MHz | 10.7 MHz | 10.7 MHz | 10.7 MHz |

Default Register Settings After Power-up

| Bits | A-word symbols | Channel '00' 868.3 MHz | Channel '01' 433.92 MHz | Channel '10' 915.0 MHz | Channel '11' 315.0 MHz | B-word symbols | Channel '00' 868.3 MHz | Channel '01' 433.92 MHz | Channel '10' 915.0 MHz | Channel '11' 315.0 MHz |
|------|----------------|------------------------|-------------------------|------------------------|------------------------|----------------|------------------------|-------------------------|------------------------|------------------------|
| 21 | not used | 0 | | | | not used | 0 | | | |
| 20 | DI_MODE | 0 | | | | not used | 0 | | | |
| 19 | MODUL | 0 | | | | EnDelPLL | 1 | | | |
| 18 | HighCur | 0 | | | | LNAHYST | 1 | | | |
| 17 | LOCK_MODE | 0 | | | | EnAdj | 0 | | | |
| 16 | PA_AUTO | 0 | | | | EnFM | 0 | | | |
| 15 | Pow1 | 1 | | | | Max2 | 1 | | | |
| 14 | Pow0 | 1 | | | | Max1 | 1 | | | |
| 13 | MIXG | 1 | | | | Max0 | 1 | | | |
| 12 | LNAG | 1 | | | | Min2 | 0 | | | |
| 11 | TE | 0 | | | | Min1 | 1 | | | |
| 10 | RE | 0 | | | | Min0 | 1 | | | |
| 9 | RR9 | 0 | 0 | 0 | 0 | RT9 | 0 | 0 | 0 | 0 |
| 8 | RR8 | 0 | 0 | 0 | 0 | RT8 | 0 | 0 | 0 | 0 |
| 7 | RR7 | 0 | 0 | 0 | 0 | RT7 | 0 | 0 | 0 | 0 |
| 6 | RR6 | 0 | 0 | 0 | 0 | RT6 | 0 | 0 | 0 | 0 |
| 5 | RR5 | 0 | 0 | 0 | 0 | RT5 | 0 | 0 | 0 | 0 |
| 4 | RR4 | 1 | 1 | 1 | 1 | RT4 | 1 | 1 | 1 | 1 |
| 3 | RR3 | 0 | 0 | 1 | 0 | RT3 | 0 | 0 | 1 | 0 |
| 2 | RR2 | 0 | 0 | 1 | 0 | RT2 | 0 | 0 | 1 | 0 |
| 1 | RR1 | 0 | 0 | 1 | 1 | RT1 | 0 | 0 | 1 | 1 |
| 0 | RR0 | 0 | 0 | 0 | 0 | RT0 | 0 | 0 | 0 | 0 |

| Bits | C-word symbols | Channel '00' 868.3 MHz | Channel '01' 433.92 MHz | Channel '10' 915.0 MHz | Channel '11' 315.0 MHz | B-word symbols | Channel '00' 868.3 MHz | Channel '01' 433.92 MHz | Channel '10' 915.0 MHz | Channel '11' 315.0 MHz |
|------|----------------|------------------------|-------------------------|------------------------|------------------------|----------------|------------------------|-------------------------|------------------------|------------------------|
| 21 | LNAGI_E | 0 | | | | MODUL_CTR | 0 | | | |
| 20 | POLAR | 0 | | | | LD_TM1 | 1 | | | |
| 19 | High2 | 0 | 0 | 0 | 0 | LD_TM0 | 0 | | | |
| 18 | High1 | 1 | 1 | 1 | 1 | ER_TM1 | 0 | | | |
| 17 | UP | 1 | 0 | 1 | 0 | ER_TM0 | 0 | | | |
| 16 | NR16 | 0 | 0 | 0 | 0 | NT16 | 0 | 0 | 0 | 0 |
| 15 | NR15 | 0 | 0 | 0 | 0 | NT15 | 0 | 0 | 0 | 0 |
| 14 | NR14 | 0 | 0 | 0 | 0 | NT14 | 0 | 0 | 0 | 0 |
| 13 | NR13 | 0 | 0 | 0 | 0 | NT13 | 0 | 0 | 0 | 0 |
| 12 | NR12 | 0 | 0 | 0 | 0 | NT12 | 0 | 0 | 0 | 0 |
| 11 | NR11 | 0 | 0 | 1 | 0 | NT11 | 0 | 0 | 1 | 0 |
| 10 | NR10 | 1 | 0 | 1 | 0 | NT10 | 1 | 0 | 1 | 0 |
| 9 | NR9 | 1 | 1 | 1 | 1 | NT9 | 1 | 1 | 1 | 1 |
| 8 | NR8 | 1 | 1 | 0 | 0 | NT8 | 1 | 1 | 0 | 1 |
| 7 | NR7 | 0 | 1 | 1 | 1 | NT7 | 1 | 1 | 1 | 0 |
| 6 | NR6 | 1 | 0 | 1 | 1 | NT6 | 0 | 1 | 1 | 0 |
| 5 | NR5 | 1 | 1 | 0 | 1 | NT5 | 0 | 0 | 1 | 0 |
| 4 | NR4 | 1 | 1 | 1 | 1 | NT4 | 1 | 0 | 1 | 1 |
| 3 | NR3 | 1 | 0 | 0 | 1 | NT3 | 0 | 1 | 1 | 1 |
| 2 | NR2 | 1 | 0 | 0 | 1 | NT2 | 1 | 0 | 1 | 0 |
| 1 | NR1 | 1 | 1 | 1 | 1 | NT1 | 1 | 1 | 1 | 0 |
| 0 | NR0 | 1 | 1 | 0 | 0 | NT0 | 1 | 1 | 1 | 1 |

Programmable Channel Operation

Serial Control Interface Description

A 3-wire (SCLK, SDTA, SDEN) Serial Control Interface (SCI) is used to program the transceiver in multi-channel mode (see Fig. 2). At each rising edge of the SCLK signal, the logic value on the SDTA pin is written into a 24-bit shift register. The data stored in the shift register are loaded into one of the 4 appropriate latches on the rising edge of SDEN. The control words are 24 bits lengths: 2 address bits and 22 data bits. The first two bits (bit 23 and 22) are latch address bits. As additional leading bits are ignored, only the least significant 24 bits are serial-clocked into the shift register. The first incoming bit is the most significant bit (MSB). To program the transceiver in multi-channel application, four 24-bit words may be sent: A-word, B-word, C-word and D-word. If individual bits within a word have to be changed, then it is sufficient to program only the appropriate 24-bit word. The serial data input timing and the structure of the control words are illustrated in Fig. 2 and 3. Table REGISTER SETTINGS describes the function of each bit.

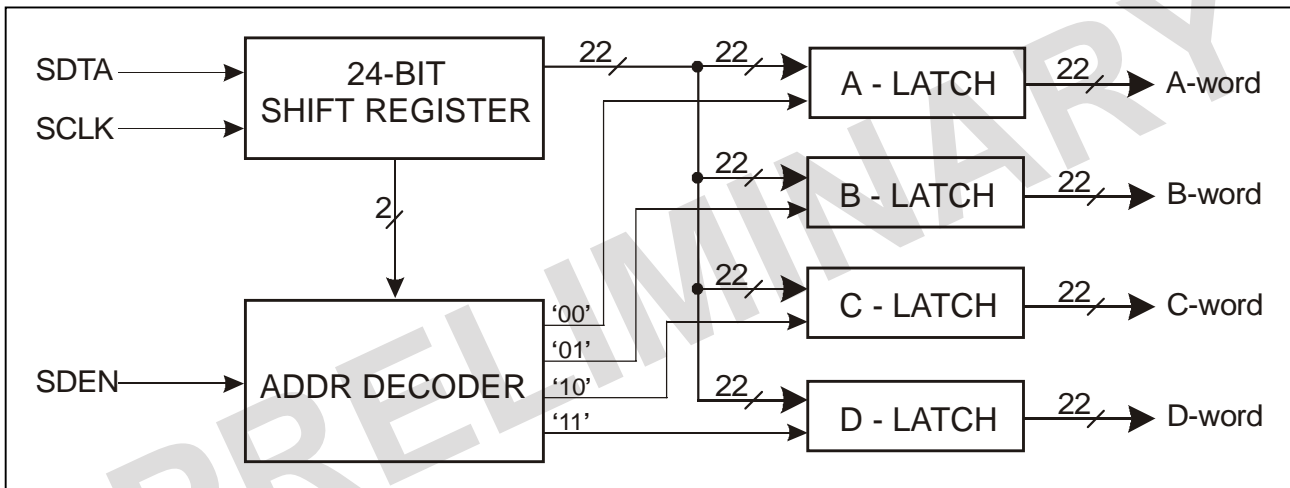


Figure 2: SCI block diagram

Due to the static CMOS design, the SCI consumes virtually no current and it can be programmed in active as well as in standby mode.

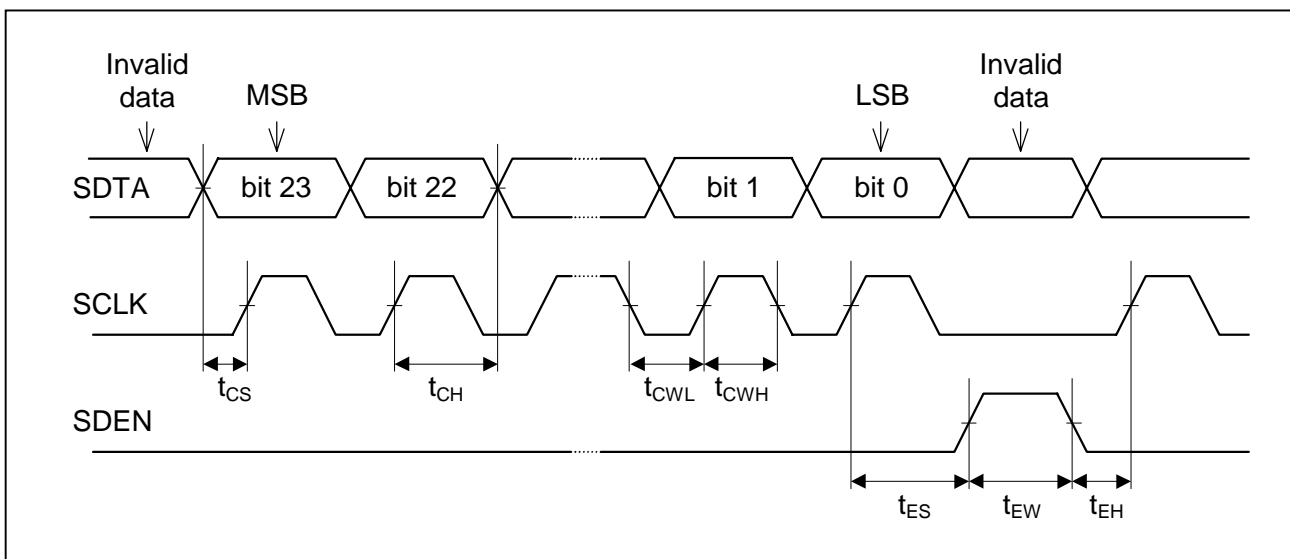


Figure 3: Serial data input timing

SCI Words

A-word

| MSB | | | | | | | | | | | | | | | | | | | | LSB | | | |
|-------------|----|----------|---------|-------|---------|-----------|---------|------|------|------|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| ADDR | | not used | DI_MODE | MODUL | HighCur | LOCK_MODE | PA_AUTO | Pow1 | Pow0 | MIXG | LNAG | TE | RE | RR9 | RR8 | RR7 | RR6 | RR5 | RR4 | RR3 | RR2 | RR1 | RR0 |

B-word

| MSB | | | | | | | | | | | | | | | | | | | | LSB | | | |
|-------------|----|----------|----------|----------|---------|-------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 1 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| ADDR | | not used | not used | EnDelPLL | LNAHYST | EnAdj | EnFm | Max2 | Max1 | Max0 | Min2 | Min1 | Min0 | RT9 | RT8 | RT7 | RT6 | RT5 | RT4 | RT3 | RT2 | RT1 | RT0 |

C-word

| MSB | | | | | | | | | | | | | | | | | | | | LSB | | | |
|-------------|----|--------|-------|-------|-------|----|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1 | 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| ADDR | | LNAG_E | POLAR | High2 | High1 | UP | NR16 | NR15 | NR14 | NR13 | NR12 | NR11 | NR10 | NR9 | NR8 | NR7 | NR6 | NR5 | NR4 | NR3 | NR2 | NR1 | NR0 |

D-word

| MSB | | | | | | | | | | | | | | | | | | | | LSB | | | |
|-------------|----|-----------|--------|--------|--------|--------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1 | 1 | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| ADDR | | MODUL_CTR | LD_TM1 | LD_TM0 | ER_TM1 | ER_TM0 | NT16 | NT15 | NT14 | NT13 | NT12 | NT11 | NT10 | NT9 | NT8 | NT7 | NT6 | NT5 | NT4 | NT3 | NT2 | NT1 | NT0 |

Register Settings

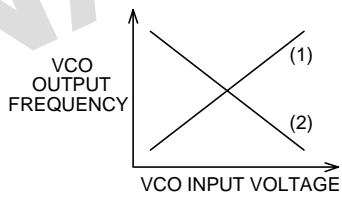
A-word

| Symbol | Bits | No. | Description |
|------------------------|---------|-----|---|
| Software button | | | |
| RR9:RR0 | [9:0] | 10 | Reference divider ratio in RX mode |
| RR9:RR0 | | | |
| TE:RE | [11:10] | 2 | Select active mode at programmable-channel application: |
| OPMODE | | | '00' Standby mode |
| | | | '11' Idle mode |
| | | | '10' Transmit mode |
| | | | '01' Receive mode |
| LNAG | [12] | 1 | Select LNA gain at internal gain control: |
| LNAGAIN | | | '0' low LNA gain |
| | | | '1' high LNA gain |
| MIXG | [13] | 1 | Select mixer conversion gain at programmable-channel application: |
| MIXGAIN | | | '0' low gain |
| | | | '1' high gain |
| Pow1:Pow0 | [15:14] | 2 | Select output power at programmable-channel application: |
| TXPOWER | | | '00' P_{max} - 20 dBm |
| | | | '01' P_{max} - 12 dBm |
| | | | '10' P_{max} - 6 dBm |
| | | | '11' P_{max} |
| PA_AUTO | [16] | 1 | Disable automatic PA turn-on after PLL lock: |
| PA_AUTO | | | '0' enabled |
| | | | '1' disabled |
| LOCK_MODE | [17] | 1 | Select PFD output analyse mode of lock detecting: |
| LOCK_MODE | | | '0' before lock only |
| | | | '1' before and after lock. |
| HighCur | [18] | 1 | Select Charge Pump output current: |
| CPCUR | | | '0' ± 260 µA |
| | | | '1' ±1300 µA |
| MODUL | [19] | 1 | Select modulation mode at internal modulation control: |
| ASK/FSK | | | '0' ASK |
| | | | '1' FSK |
| DI_MODE | [20] | 1 | Select mode for input data: |
| DI_MODE | | | '0' normal |
| | | | '0' for space at ASK or f _{min} at FSK, '1' for mark at ASK or f _{max} at FSK |
| | | | '1' inverse |
| | | | '1' for space at ASK or f _{min} at FSK, '0' for mark at ASK or f _{max} at FSK |
| not used | [21] | 1 | 'X' |

B-word

| Symbol | Bits | No. | Description | | | | | | | | | | | | | | | | |
|------------------------|-----------------------|-----|---|-------|-----------------------|-------|------------|-------|-------------|-------|-------------|-------|-------------|-------|-------------|-------|-------------|-------|-------------|
| Software button | | | | | | | | | | | | | | | | | | | |
| RT9:RT0 | [9:0] | 10 | Reference divider ratio in TX mode | | | | | | | | | | | | | | | | |
| RT9:RT0 | | | | | | | | | | | | | | | | | | | |
| Min2:Min0 | [12:10] | 3 | Select minimum value of RO active current: | | | | | | | | | | | | | | | | |
| ROMIN | | | <table style="width: 100%; border-collapse: collapse;"> <tr><td style="width: 15%;">'000'</td><td>0 μA</td></tr> <tr><td>'001'</td><td>50 μA</td></tr> <tr><td>'010'</td><td>100 μA</td></tr> <tr><td>'011'</td><td>150 μA</td></tr> <tr><td>'100'</td><td>200 μA</td></tr> <tr><td>'101'</td><td>250 μA</td></tr> <tr><td>'110'</td><td>300 μA</td></tr> <tr><td>'111'</td><td>350 μA</td></tr> </table> | '000' | 0 μ A | '001' | 50 μ A | '010' | 100 μ A | '011' | 150 μ A | '100' | 200 μ A | '101' | 250 μ A | '110' | 300 μ A | '111' | 350 μ A |
| '000' | 0 μ A | | | | | | | | | | | | | | | | | | |
| '001' | 50 μ A | | | | | | | | | | | | | | | | | | |
| '010' | 100 μ A | | | | | | | | | | | | | | | | | | |
| '011' | 150 μ A | | | | | | | | | | | | | | | | | | |
| '100' | 200 μ A | | | | | | | | | | | | | | | | | | |
| '101' | 250 μ A | | | | | | | | | | | | | | | | | | |
| '110' | 300 μ A | | | | | | | | | | | | | | | | | | |
| '111' | 350 μ A | | | | | | | | | | | | | | | | | | |
| Max2:Max0 | [15:13] | 3 | Select maximum value of RO active current: | | | | | | | | | | | | | | | | |
| ROMAX | | | <table style="width: 100%; border-collapse: collapse;"> <tr><td style="width: 15%;">'000'</td><td>0 μA (RO is off)</td></tr> <tr><td>'001'</td><td>50 μA</td></tr> <tr><td>'010'</td><td>100 μA</td></tr> <tr><td>'011'</td><td>150 μA</td></tr> <tr><td>'100'</td><td>200 μA</td></tr> <tr><td>'101'</td><td>250 μA</td></tr> <tr><td>'110'</td><td>300 μA</td></tr> <tr><td>'111'</td><td>350 μA</td></tr> </table> | '000' | 0 μ A (RO is off) | '001' | 50 μ A | '010' | 100 μ A | '011' | 150 μ A | '100' | 200 μ A | '101' | 250 μ A | '110' | 300 μ A | '111' | 350 μ A |
| '000' | 0 μ A (RO is off) | | | | | | | | | | | | | | | | | | |
| '001' | 50 μ A | | | | | | | | | | | | | | | | | | |
| '010' | 100 μ A | | | | | | | | | | | | | | | | | | |
| '011' | 150 μ A | | | | | | | | | | | | | | | | | | |
| '100' | 200 μ A | | | | | | | | | | | | | | | | | | |
| '101' | 250 μ A | | | | | | | | | | | | | | | | | | |
| '110' | 300 μ A | | | | | | | | | | | | | | | | | | |
| '111' | 350 μ A | | | | | | | | | | | | | | | | | | |
| EnFm | [16] | 1 | Test bit. Forced '0' for correct functioning. | | | | | | | | | | | | | | | | |
| EnAdj | [17] | 1 | Test bit. Forced '0' for correct functioning. | | | | | | | | | | | | | | | | |
| LNAHYST | [18] | 1 | Enable LNA hysteresis: | | | | | | | | | | | | | | | | |
| LNAHYST | | | <table style="width: 100%; border-collapse: collapse;"> <tr><td style="width: 15%;">'1'</td><td>disabled</td></tr> <tr><td>'0'</td><td>enabled</td></tr> </table> | '1' | disabled | '0' | enabled | | | | | | | | | | | | |
| '1' | disabled | | | | | | | | | | | | | | | | | | |
| '0' | enabled | | | | | | | | | | | | | | | | | | |
| EnDelPLL | [19] | 1 | Enable delayed start of the PLL: | | | | | | | | | | | | | | | | |
| EnDelPLL | | | <table style="width: 100%; border-collapse: collapse;"> <tr><td style="width: 15%;">'1'</td><td>disabled</td></tr> <tr><td>'0'</td><td>enabled.</td></tr> </table> | '1' | disabled | '0' | enabled. | | | | | | | | | | | | |
| '1' | disabled | | | | | | | | | | | | | | | | | | |
| '0' | enabled. | | | | | | | | | | | | | | | | | | |
| not used | [20] | 1 | 'X' | | | | | | | | | | | | | | | | |
| not used | [21] | 1 | 'X' | | | | | | | | | | | | | | | | |

C-word

| Symbol | Bits | No. | Description | |
|------------------------|---------|-----|--|--------------------------------|
| Software button | | | | |
| NR16:NR0 | [16:0] | 17 | Feedback divider ratio in RX mode | |
| NR16:NR0 | | | | |
| UP | [17] | 1 | Select frequency band: | |
| BAND | | | '1' | up to 500 MHz |
| | | | '0' | 500 to 1000MHz |
| High2:High1 | [19:18] | 2 | Select VCO active current: | |
| VCOCUR | | | '00' | low current (250 μ A) |
| | | | '01' | standard current (350 μ A) |
| | | | '10' | high1 current (450 μ A) |
| | | | '11' | high2 current (550 μ A) |
| POLAR | [20] | 1 | Select Phase Detector polarity: | |
| PFDPOL | | | '1' | positive (1) |
| | | | '0' | negative (2) |
| | | |  | |
| LNAGI_E | [21] | 1 | Select LNA gain control mode: | |
| LNACTRL | | | '0' | external LNA gain control |
| | | | '1' | internal LNA gain control |

D-word

| Symbol | Bits | No. | Description | | | | | | | | |
|-----------------|-----------------------------|-----|---|------|-----------------------------|------|-----------------------------|------|-----------|------|------------|
| Software button | | | | | | | | | | | |
| NT16:NT0 | [16:0] | 17 | Feedback divider ratio in TX mode | | | | | | | | |
| NT16:NT0 | | | | | | | | | | | |
| ER_TM1:ER_TM0 | [18:17] | 2 | Select maximum enabled PFD output error for lock detecting (in reference frequency clocks): | | | | | | | | |
| ER_TM1:ER_TM0 | | | <table border="0"> <tr> <td>'00'</td> <td>2 clocks</td> </tr> <tr> <td>'01'</td> <td>4 clocks</td> </tr> <tr> <td>'10'</td> <td>8 clocks</td> </tr> <tr> <td>'11'</td> <td>16 clocks</td> </tr> </table> | '00' | 2 clocks | '01' | 4 clocks | '10' | 8 clocks | '11' | 16 clocks |
| '00' | 2 clocks | | | | | | | | | | |
| '01' | 4 clocks | | | | | | | | | | |
| '10' | 8 clocks | | | | | | | | | | |
| '11' | 16 clocks | | | | | | | | | | |
| LD_TM1:LD_TM0 | [20:19] | 2 | Select minimum number of PFD reference frequency clocks before lock detecting: | | | | | | | | |
| LD_TM1:LD_TM0 | | | <table border="0"> <tr> <td>'00'</td> <td>4 clocks</td> </tr> <tr> <td>'01'</td> <td>16 clocks</td> </tr> <tr> <td>'10'</td> <td>64 clocks</td> </tr> <tr> <td>'11'</td> <td>256 clocks</td> </tr> </table> | '00' | 4 clocks | '01' | 16 clocks | '10' | 64 clocks | '11' | 256 clocks |
| '00' | 4 clocks | | | | | | | | | | |
| '01' | 16 clocks | | | | | | | | | | |
| '10' | 64 clocks | | | | | | | | | | |
| '11' | 256 clocks | | | | | | | | | | |
| MODUL_CTR | [21] | 1 | Select mode of modulation control: | | | | | | | | |
| MODCTRL | | | <table border="0"> <tr> <td>'0'</td> <td>external modulation control</td> </tr> <tr> <td>'1'</td> <td>internal modulation control</td> </tr> </table> | '0' | external modulation control | '1' | internal modulation control | | | | |
| '0' | external modulation control | | | | | | | | | | |
| '1' | internal modulation control | | | | | | | | | | |

Technical Data

Absolute Maximum Ratings

| Parameter | Symbol | Condition / Note | Min | Max | Unit |
|-------------------------|------------|----------------------|------|--------------|------|
| Supply voltage | V_{CC} | | 0 | 7.0 | V |
| Input voltage | V_{IN} | | -0.3 | $V_{CC}+0.3$ | V |
| Input current | I_{IN} | | -1 | 1 | mA |
| Input RF level | P_{imax} | no damage | | 10 | dBm |
| Storage temperature | T_{STG} | | -40 | +125 | °C |
| Electrostatic discharge | V_{ESD1} | human body model, 1) | -1.0 | +1.0 | kV |
| Electrostatic discharge | V_{ESD2} | human body model, 2) | TBD | TBD | kV |

- 1) pins IN_DTA, ASK/FSK, RE/SCLK; TE/SDTA, FS0/SDEN, FS1/LD
 2) all pins, except IN_DTA, ASK/FSK, RE/SCLK; TE/SDTA, FS0/SDEN, FS1/LD

Normal Operating Conditions

| Parameter | Symbol | Condition | Min | Max | Unit |
|-----------------------|------------|--------------|---------|-----------|--------|
| Supply voltage | V_{CC} | | 2.5 | 5.5 | V |
| Operating temperature | T_a | | -40 | +85 | °C |
| Carrier frequency | f_c | | 300 | 930 | MHz |
| VCO frequency | f_{VCO} | | 300 | 930 | MHz |
| RO frequency | f_{RO} | | 3 | 12 | MHz |
| Frequency deviation | Δf | at FM or FSK | ± 5 | ± 120 | kHz |
| FSK data rate | R_{FSK} | NRZ | | 60 | kbit/s |
| FM bandwidth | f_m | | | 20 | kHz |
| ASK data rate | R_{ASK} | NRZ | | 60 | kbit/s |

DC Characteristics

all parameters under normal operating conditions, unless otherwise stated;
 typical values at $T_a = 23\text{ °C}$ and $V_{CC} = 3\text{ V}$

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|--|----------------|--|-----|-----|------|------|
| Standby current | I_{SBY} | TE/SDTA=0, RE/SCLK=0 | | 50 | 100 | nA |
| Idle current | I_{IDLE} | TE/SDTA=1, RE/SCLK=1 @ $f_i = 868.3\text{ MHz}$ | | 2.5 | 3.2 | mA |
| Total supply current in receive mode at low gain | I_{RX_low} | TE/SDTA=0, RE/SCLK=1 $V_{GAIN_LNA} > 1.4\text{ V}$ @ $f_i = 868.3\text{ MHz}$ | | 6.0 | 8.0 | mA |
| Total supply current in receive mode at high gain | I_{RX_high} | TE/SDTA=0, RE/SCLK=1 $V_{GAIN_LNA} < 0.8\text{ V}$ @ $f_i = 868.3\text{ MHz}$ | | 7.0 | 9.0 | mA |
| Total supply current in transmit mode at 0 dBm power | I_{TX_0} | TE/SDTA=1, RE/SCLK=0 ASK/FSK=1 @ $f_i = 868.3\text{ MHz}$, @ $P_o = 0\text{ dBm}$ | | 9.0 | 11.5 | mA |

AC System Characteristics of the Receiver Part

all parameters under normal operating conditions, unless otherwise stated; all parameters based on test circuits for FSK (Fig. 4 to 5), FM and ASK (Fig. 6 to 7), respectively; RF at 868.3 MHz

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|--|--------------------|--|-----|------|-------------------------------|------|
| Input sensitivity – FSK | P_{min_FSK} | $B_{IF} = 150\text{kHz}$ $\Delta f = \pm 50 \text{ kHz (FSK/FM)}$ $BER \leq 3 \cdot 10^{-3}$ | | -103 | | dBm |
| Input sensitivity – ASK | P_{min_ASK} | $B_{IF} = 150\text{kHz}$ $BER \leq 3 \cdot 10^{-3}$ | | -105 | | dBm |
| Maximum input signal – FSK/FM at low gain | $P_{max_FSK_1}$ | $BER \leq 3 \cdot 10^{-3}$ $V_{GAIN_LNA} > 1.4 \text{ V}$ | | 10 | | dBm |
| Maximum input signal – FSK/FM at high gain | $P_{max_FSK_0}$ | $BER \leq 3 \cdot 10^{-3}$ $V_{GAIN_LNA} < 0.8 \text{ V}$ | | -10 | | dBm |
| Maximum input signal – ASK at low gain | $P_{max_ASK_1}$ | $BER \leq 3 \cdot 10^{-3}$ $V_{GAIN_LNA} > 1.4 \text{ V}$ | | -20 | | dBm |
| Maximum input signal – ASK at high gain | $P_{max_ASK_0}$ | $BER \leq 3 \cdot 10^{-3}$ $V_{GAIN_LNA} < 0.8 \text{ V}$ | | 0 | | dBm |
| Image rejection | ΔP_{imag} | | | TBD | | dB |
| Blocking immunity | ΔP_{block} | $\Delta f_{block} > \pm 2\text{MHz}$, note 1 | | TBD | | dB |
| Start-up time – FSK/FM | T_{FSK} | TE/SDTA=0, RE/SCLK=1 valid data at output | | | 1 | ms |
| Start-up time – ASK | T_{ASK} | depends on ASK de- tector time constant and start-up mode, valid data at output | | | T_{FSK} + $200K * C6$ | ms |
| Spurious emission | P_{spur} | | | | -70 | dBm |

Notes: 1. desired signal with FSK/FM or ASK modulation, CW blocking signal

AC System Characteristics of the Transmitter Part

all parameters under normal operating conditions, unless otherwise stated;
typical values at $T_a = 23 \text{ }^\circ\text{C}$ and $V_{cc} = 3 \text{ V}$;

TE/SDTA=1, RE/SCLK=0, ASK/FSK=1, RPS \geq 15 k Ω , $f_c = 868.3 \text{ MHz}$, test circuit shown in Fig. 4 to 7

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|-------------------------|------------------|---|---------|----------|-----------|---------------|
| Output power | P_o | CW mode | 4 | 6 | 8 | dBm |
| FSK deviation | Δf_{FSK} | depends on C_{x1} , C_{x2} and crystal parameter | ± 5 | ± 50 | ± 100 | kHz |
| Data rate FSK | R_{FSK} | | | 60 | | kbit/s |
| FM deviation | Δf_{FM} | adjustable with varactor and V_{FM} | | ± 6 | | kHz |
| Modulation frequency FM | f_{mod} | | | 5 | | kHz |
| Data rate ASK | R_{ASK} | | | 60 | | kbit/s |
| PLL spurs emission | P_{spur} | at all f_c and nominal P_o | | | -36 | dBm |
| Harmonic emission | P_{harm} | at all f_c and power steps | | - | -36 | dBm |
| VCO gain | K_{VCO} | | | 35 | | MHz/V |
| Charge pump current | I_{CP} | | | 260 | | μA |
| Start-up time | T_{TX} | from "standby" to "transmit" mode | | | 1 | ms |

Output Power Selection

typical values at $T_a = 23\text{ }^\circ\text{C}$ and $V_{cc} = 3\text{ V}$:
TE/SDTA = 1, RE/SCLK = 0, ASK/FSK = 1, $f_c = 868.3\text{ MHz}$, CW mode

| RPS / $k\Omega$ | $\geq 15\text{ k}$ | 6.8 k | 3.3 k | 1.0 k |
|------------------|--------------------|------------|------------|------------|
| I_{cc} / mA | TBD | 9.0 | TBD | TBD |
| P_O / dBm | 6 | 0 | -6 | -15 |
| P_{harm} / dBm | ≤ -36 | ≤ -36 | ≤ -36 | ≤ -36 |

Serial Control Interface

| Parameter | Symbol | Condition | Min | Max | Unit |
|----------------------------------|-----------|-----------|-----|-----|------|
| Data to clock set up time | t_{CS} | | 150 | | ns |
| Data to clock hold time | t_{CH} | | 50 | | ns |
| Clock pulse width high | t_{CWH} | | 100 | | ns |
| Clock pulse width low | t_{CWL} | | 100 | | ns |
| Clock to load enable set up time | t_{ES} | | 100 | | |

Crystal Parameters

| Parameter | Symbol | Condition | Min | Max | Unit |
|---------------------|---------------|----------------------|-----|-----|----------|
| Crystal frequency | $f_{crystal}$ | fundamental mode, AT | 3 | 12 | MHz |
| Load capacitance | C_{load} | | 10 | 15 | pF |
| Static capacitance | C_0 | | | 7 | pF |
| Motional resistance | R_m | | | 70 | Ω |

Application Circuit Examples

Programmable Channel FSK Application Circuit

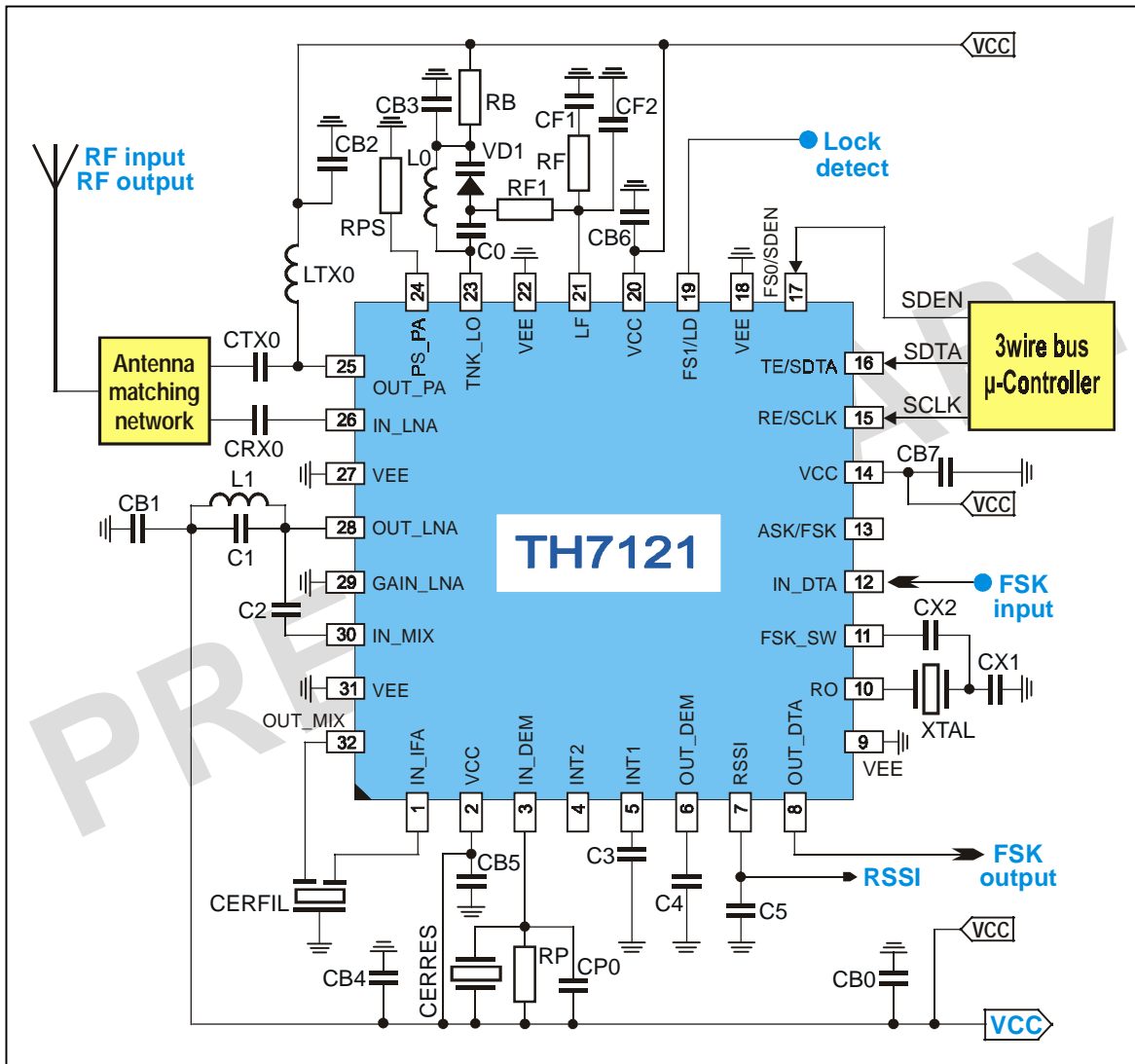


Figure 4: Test circuit for programmable channel FSK operation

Fixed-Frequency FSK Application Circuit

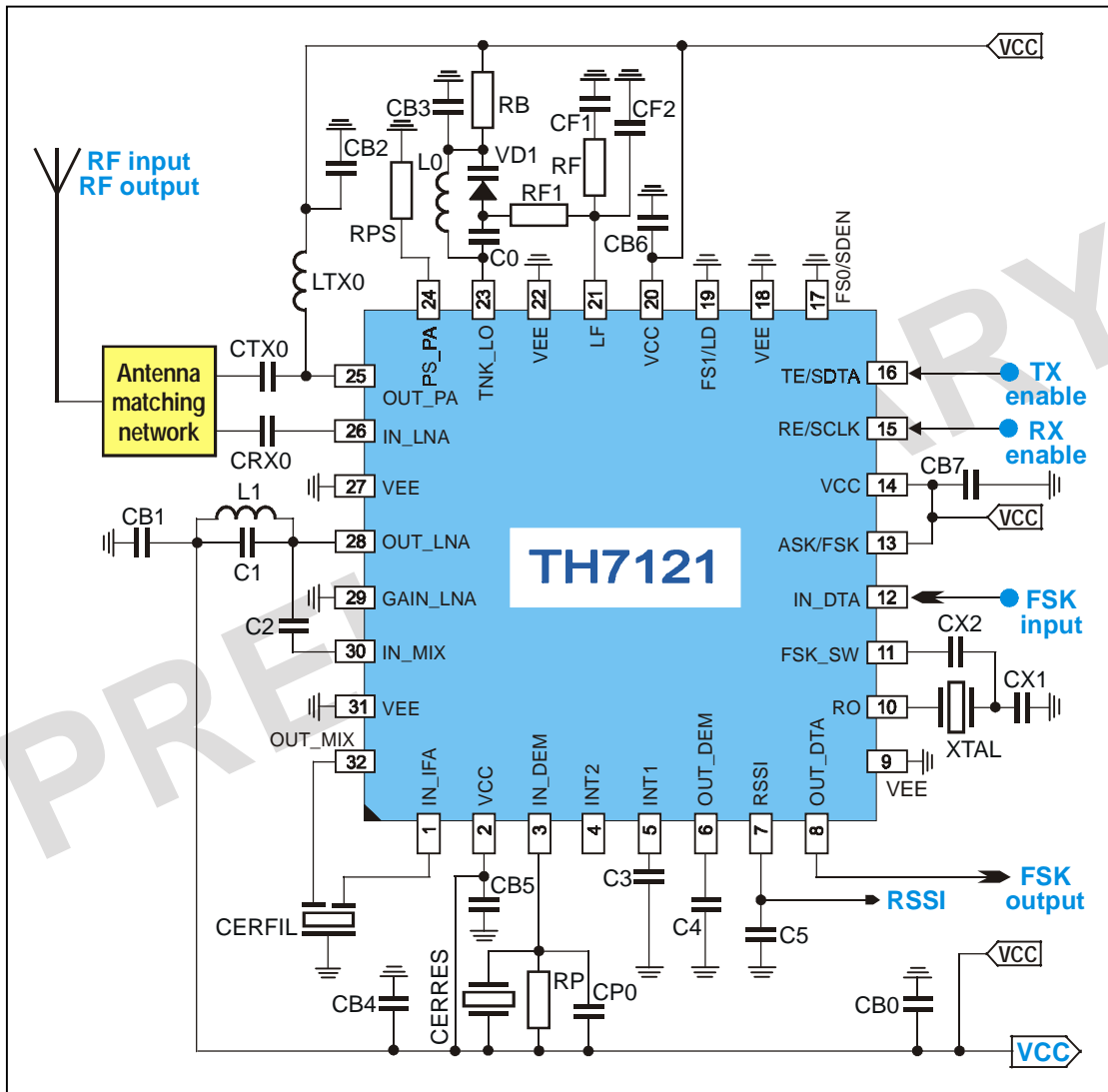


Figure 5: Test circuit for fixed-frequency FSK operation at 868 MHz

FSK test circuit component list to Fig. 4 and Fig. 5

| Part | Size | Value @ 868.3 MHz | Tolerance | Description |
|------------|----------------|---|--------------------------------|--|
| C0 | 0805 | 8.2 pF | ±5% | VCO tank capacitor |
| C1 | 0603 | NIP | ±5% | LNA output tank capacitor |
| C2 | 0603 | 1 pF | ±5% | MIX input matching capacitor |
| C3 | 0805 | 10 nF | ±10% | data slicer capacitor |
| C4 | 0805 | 100 pF | ±10% | demodulator output low-pass capacitor, depending on data rate |
| C5 | 0805 | 330 pF | ±10% | RSSI output low pass capacitor |
| CB0 | 0805 | 100 nF | ±10% | blocking capacitor |
| CB1 to CB4 | 0805 0603 | 330 pF | ±10% | blocking capacitor |
| CB5 | 0603 | 330 pF | ±10% | blocking capacitor |
| CB6 | 0603 | 10 nF | ±10% | blocking capacitor |
| CB7 | 0603 | 330 pF | ±10% | blocking capacitor |
| CF1 | 0805 | 2.2 nF | ±5% | loop filter capacitor |
| CF2 | 0805 | 100 pF | ±5% | loop filter capacitor |
| CX1 | 0805 | 15 pF | ±5% | RO capacitor |
| CX2 | 0805 | 33 pF | ±5% | RO capacitor for FSK ($\Delta f = \pm 20$ kHz) |
| CP0 | 0805 | 10 - 12 pF | ±5% | CERRES parallel capacitor |
| CRX0 | 0603 | 100 pF | ±5% | RX coupling capacitor |
| CTX0 | 0603 | 10 pF | ±5% | TX coupling capacitor |
| RB | 0805 | 10 Ω | ±10% | blocking resistor for VCC |
| RP | 0805 | 3.9 k Ω | ±5% | CERFIL parallel resistor |
| RF | 0805 | 82 k Ω | ±5% | loop filter resistor |
| RF1 | 0805 | 9.1 k Ω | ±5% | loop filter resistor |
| RPS | 0805 | NIP | ±5% | power-select resistor, only required at fixed-frequency operation |
| L0 | 0805 | 2.2 nH | ±5% | VCO tank inductor |
| L1 | 0603 | 10 nH | ±5% | LNA output tank inductor |
| LTX0 | 0805 | 2.2 nH // 2.7 pF | ±5% | TX impedance matching inductor |
| VD1 | SOD-323 | BBY-03W | | varactor diode from Infineon |
| XTAL | HC49-SMD | 7.1505 MHz | ±30ppm calibr. ±30ppm temp. | fundamental-mode crystal, $C_{load} = 10$ pF to 15pF, $C_{0, max} = 7$ pF, $R_{m, max} = 70 \Omega$ |
| CERFIL | Leaded type | SFE10.7MFP @ $B_{IF2} = 40$ kHz | TBD | ceramic filter from Murata |
| | SMD type | SFECV10.7MJS-A @ $B_{IF2} = 150$ kHz | ±40 kHz | ceramic filter from Murata |
| CERRES | SMD type | CDACV10.7MG18-A | | ceramic demodulator tank from Murata |

Notes:

- NIP – not in place, may be used optionally
- Antenna matching network according to Evaluation Board Description EVB7120

Programmable Channel ASK Application Circuit

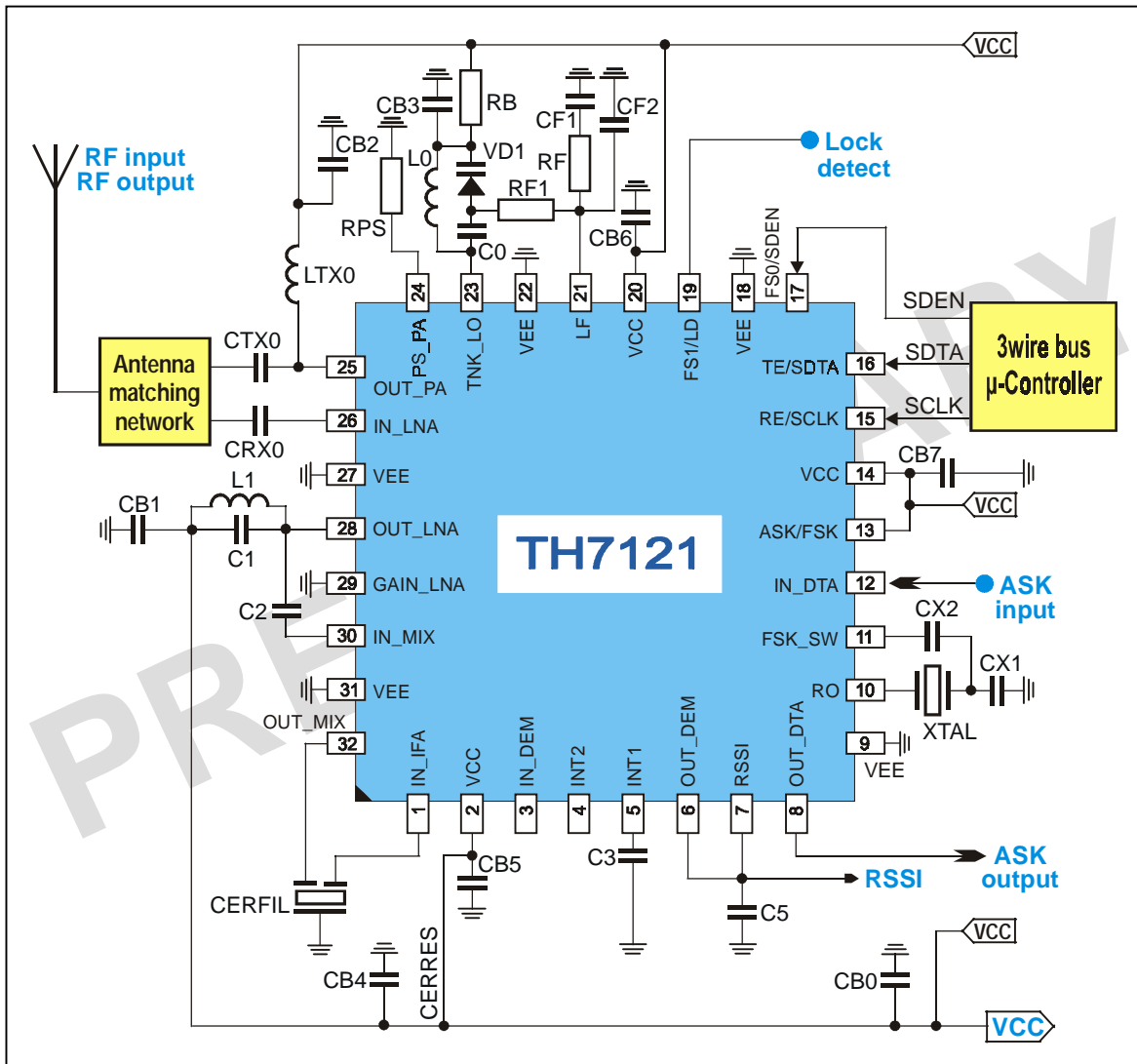


Figure 6: Test circuit for programmable channel ASK operation

Fixed-Frequency ASK Application Circuit

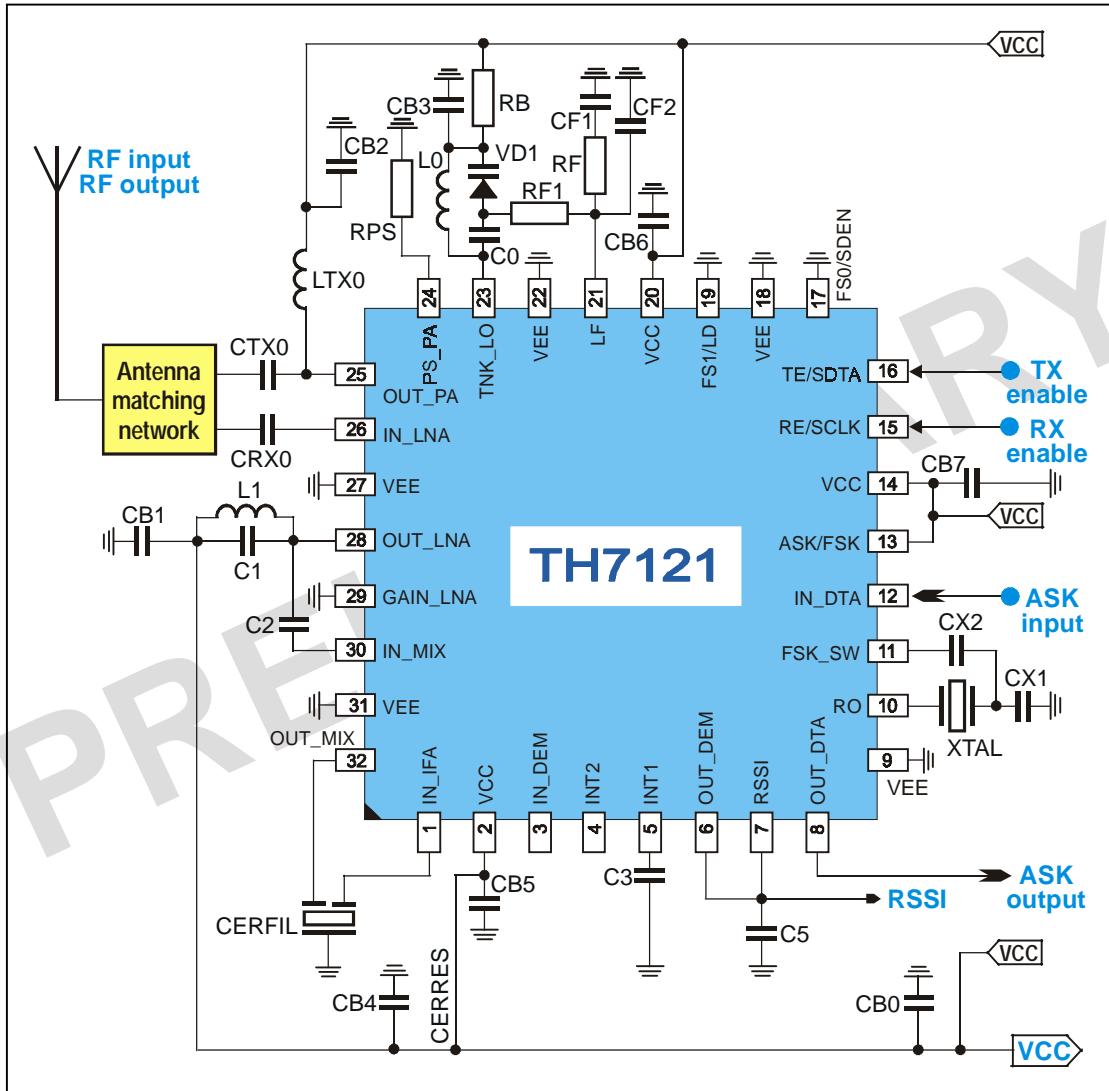


Figure 7: Test circuit for fixed-frequency ASK operation at 868 MHz

ASK test circuit component list to Fig. 6 and Fig. 7

| Part | Size | Value @ 868.3 MHz | Tolerance | Description |
|------------|--------------|---|--------------------------------|---|
| C0 | 0805 | 8.2 pF | ±5% | VCO tank capacitor |
| C1 | 0603 | NIP | ±5% | LNA output tank capacitor |
| C2 | 0603 | 1 pF | ±5% | MIX input matching capacitor |
| C3 | 0805 | 10 nF | ±10% | data slicer capacitor |
| C5 | 0805 | 330 pF | ±10% | RSSI output low pass capacitor |
| CB0 | 0805 | 100 nF | ±10% | blocking capacitor |
| CB1 to CB3 | 0805 0603 | 330 pF | ±10% | blocking capacitor |
| CB5 | 0603 | 330 pF | ±10% | blocking capacitor |
| CB6 | 0603 | 10 nF | ±10% | blocking capacitor |
| CB7 | 0603 | 330 pF | ±10% | blocking capacitor |
| CF1 | 0805 | 2.2 nF | ±5% | loop filter capacitor |
| CF2 | 0805 | 100 pF | ±5% | loop filter capacitor |
| CX1 | 0805 | 15 pF | ±5% | RO capacitor |
| CRX0 | 0603 | 100 pF | ±5% | RX coupling capacitor |
| CTX0 | 0603 | 10 pF | ±5% | TX coupling capacitor |
| RB | 0805 | 10 Ω | ±10% | blocking resistor for VCC |
| RF | 0805 | 9.1 kΩ | ±5% | loop filter resistor |
| RPS | 0805 | NIP | ±5% | power-select resistor, only required at fixed-frequency operation |
| L0 | 0805 | 2.2 nH | ±5% | VCO tank inductor |
| L1 | 0603 | 10 nH | ±5% | LNA output tank inductor |
| LTX0 | 0805 | 82 nH | ±5% | TX impedance matching inductor |
| XTAL | HC49-SMD | 7.1505 MHz | ±30ppm calibr. ±30ppm temp. | fundamental-mode crystal, $C_{load} = 10 \text{ pF to } 15 \text{ pF}$, $C_{0, max} = 7 \text{ pF}$, $R_{m, max} = 70 \text{ } \Omega$ |
| CERFIL | Leaded type | SFE10.7MFP @ $B_{IF2} = 40 \text{ kHz}$ | TBD | ceramic filter from Murata |
| | SMD type | SFECV10.7MJS-A @ $B_{IF2} = 150 \text{ kHz}$ | ±40 kHz | ceramic filter from Murata |

Notes:

- NIP – not in place, may be used optionally
- Antenna matching network according to Evaluation Board Description EVB7120

Programmable Channel FSK Application Circuit with AFC

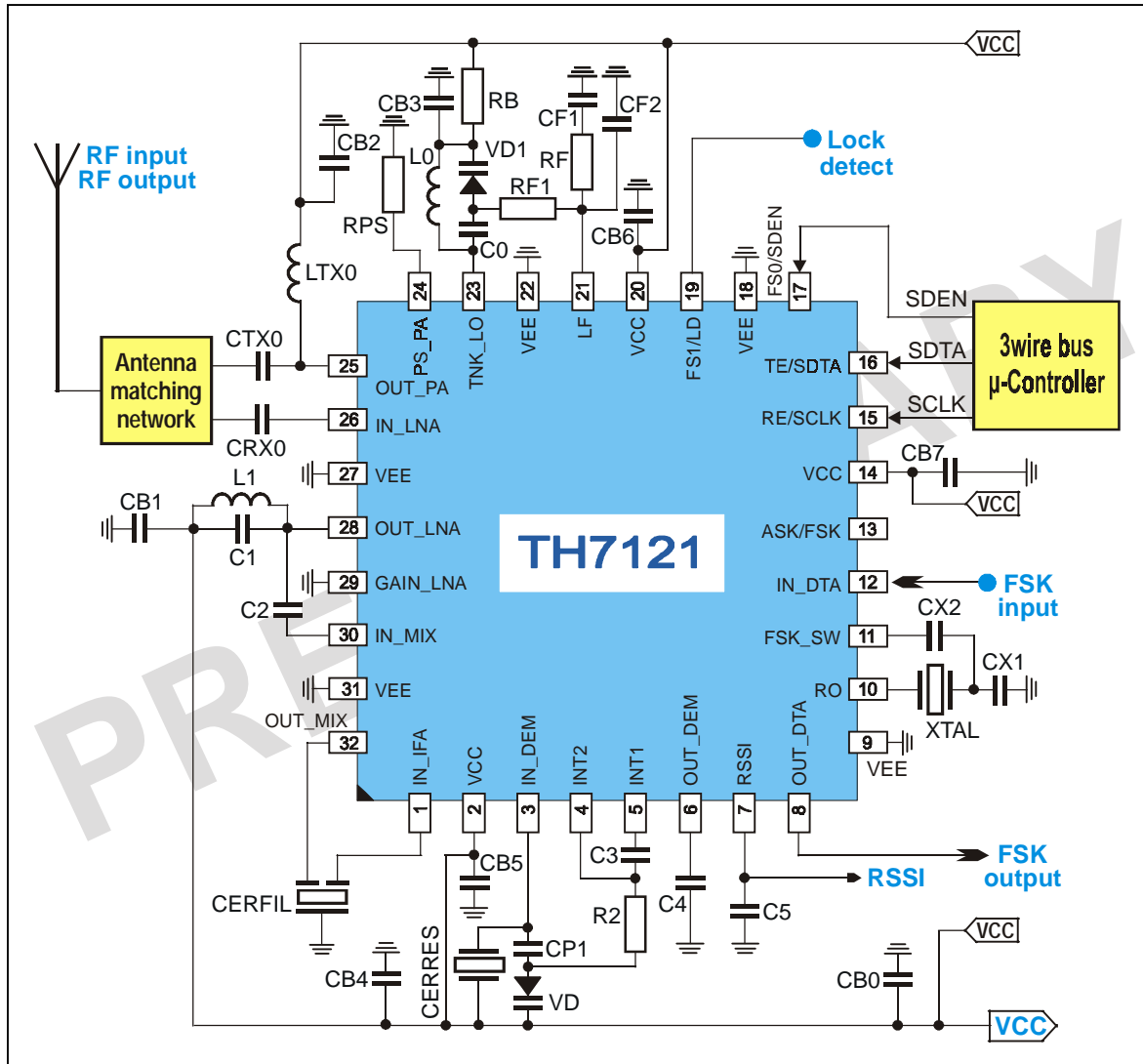


Figure 8: Test circuit for programmable channel FSK operation with AFC

Circuit Features

- Automatic Frequency Control (AFC)
- Increases input frequency acceptance range up to $RF_{nom} \pm 50$ kHz
- Compensation of calibration tolerances of ceramic resonator
- Compensation of temperature tolerances of ceramic resonator

Fixed-Frequency FSK Application Circuit with AFC

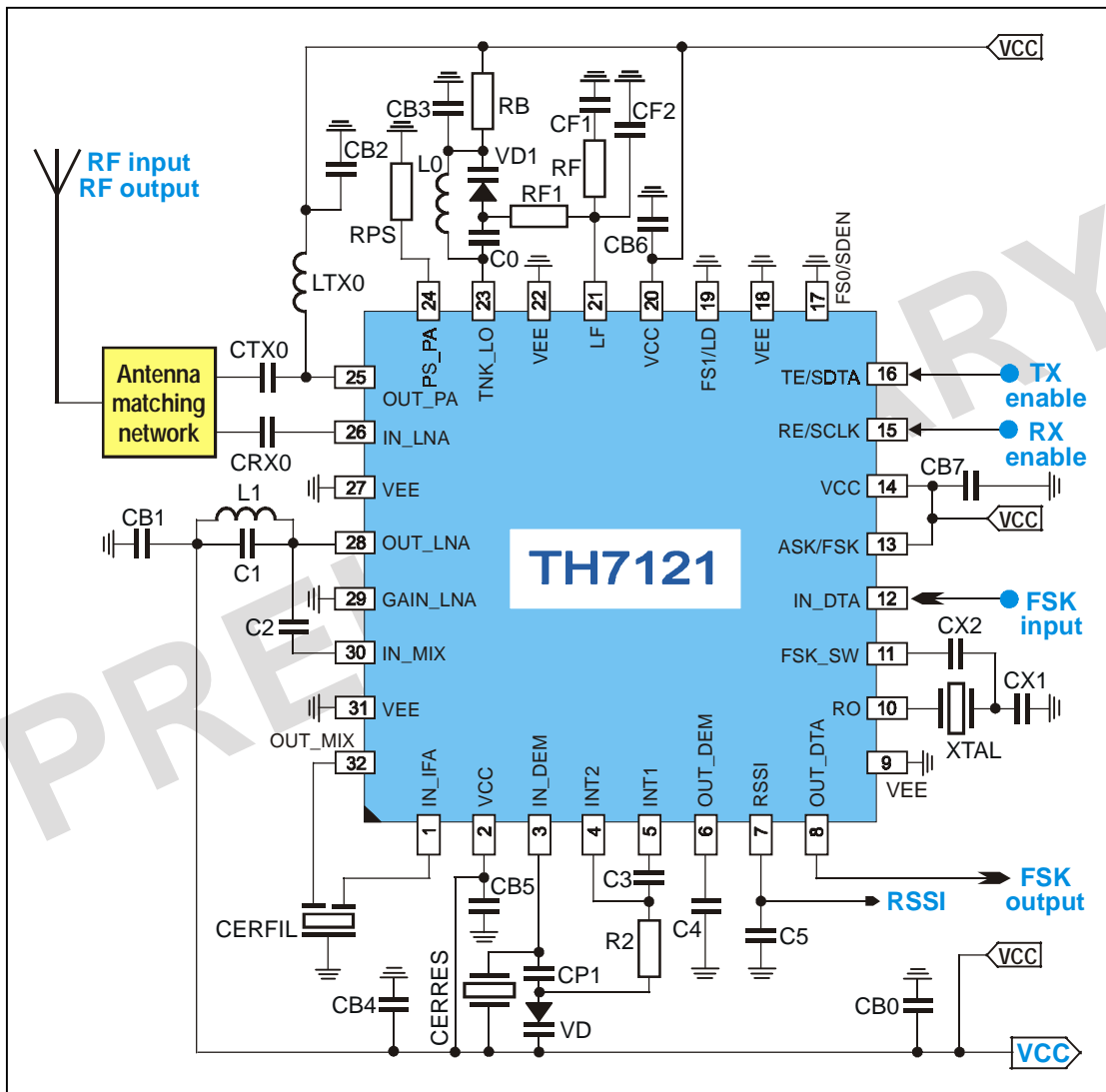


Figure 9: Test circuit for fixed-frequency FSK operation at 868 MHz with AFC

Circuit Features

- Automatic Frequency Control (AFC)
- Increases input frequency acceptance range up to $RF_{nom} \pm 50$ kHz
- Compensation of calibration tolerances of ceramic resonator
- Compensation of temperature tolerances of ceramic resonator

Package Dimensions

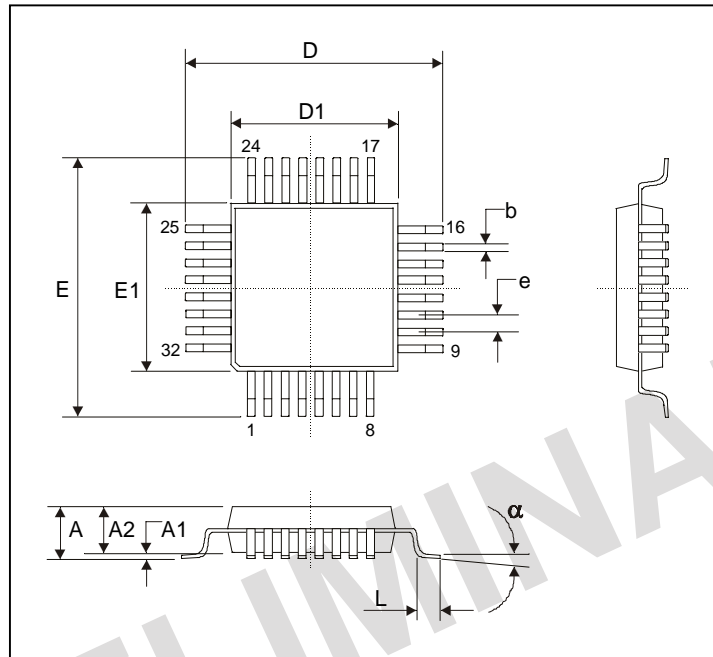


Fig. 7: LQFP32 (Low Quad Flat Package)

| All Dimension in mm, coplanarity < 0.1mm | | | | | | | | | |
|---|--------|-------|-------|-------|-------|-------|-------|-------|----------|
| | E1, D1 | A | A1 | A2 | e | b | L | E, D | α |
| min | 7.00 | 1.60 | 0.05 | 1.35 | 0.8 | 0.30 | 0.45 | 9.00 | 0° |
| max | | | 0.15 | 1.45 | | 0.45 | 0.75 | | 7° |
| All Dimension in inch, coplanarity < 0.004" | | | | | | | | | |
| | E1, D1 | A | A1 | A2 | e | b | L | E, D | α |
| min | 0.276 | 0.630 | 0.002 | 0.053 | 0.031 | 0.012 | 0.018 | 0.354 | 0° |
| max | | | 0.006 | 0.057 | | 0.018 | 0.030 | | 7° |

Your Notes

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