Electrically Erasable PROM

TYPICAL FEATURES

- **Internally Organized 256 x 8**
- **2 Wire Serial Interface**
- **Provides Bidirectional Data Transfer Protocol**
- **Eight Byte Page Write Mode**
  - **—Minimizes Total Write Time Per Byte**
- **Self Timed Write Cycle**
  - **—Typical Write Cycle Time of 5 ms**
- **High Reliability**
  - **—Endurance: 100,000 Writes Per Byte**
  - **—Data Retention: 100 Years**
- **8 Pin Mini-DIP and 14 Lead SOIC Packages**

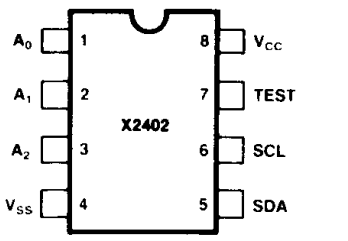
DESCRIPTION

The X2402 is a 2048 bit serial E²PROM, internally organized as one 256 x 8 page. The X2402 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories.

The X2402 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E²PROMs are designed and tested for applications requiring extended endurance and data retention. Endurance is specified as 100,000 cycles per byte minimum and data retention is specified as 100 years minimum. Refer to Xicor reliability reports RR-520 and RR-515 for details of endurance and data retention characteristics.

PIN CONFIGURATIONS



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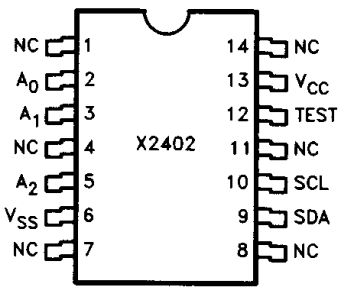

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PIN NAMES

A_0 to A_2	Address Inputs
V_{SS}	Ground
SDA	Serial Data
SCL	Serial Clock
Test	**Input to V_{SS}**
V_{CC}	Supply Voltage

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2402 ..... −10°C to +85°C
X2402I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2402 T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2402I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	X2402 Limits			X2402I Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Supply Current		20	30		20	35	mA	f_{SCL} = 100 KHz
I_{SB}	V_{CC} Standby Current		15	25		15	30	mA	
I_{LI}	Input Leakage Current		0.1	10		0.1	10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		0.1	10		0.1	10	µA	V_{OUT} = GND to V_{CC}
I_{TP}(2)	Test Pin Pull Down Current		16	30		16	30	µA	V_{IN} = V_{CC}
V_{IL}(4)	Input Low Voltage	−1.0		0.8	−1.0		0.8	V	
V_{IH}(4)	Input High Voltage	2.0		V_{CC} +0.5	2.0		V_{CC} +1.0	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL} = 3 mA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units	Conditions
Endurance	100,000		Cycles/Byte	Xicor Reliability Report RR-520
Data Retention	100		Years	Xicor Reliability Report RR-515

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) Test pin has on chip pull down device which sinks 16 µA (typical) to V_{SS}.
(3) This parameter is periodically sampled and not 100% tested.
(4) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

A.C. CHARACTERISTICS

X2402 T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2402I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read & Write Cycle Limits

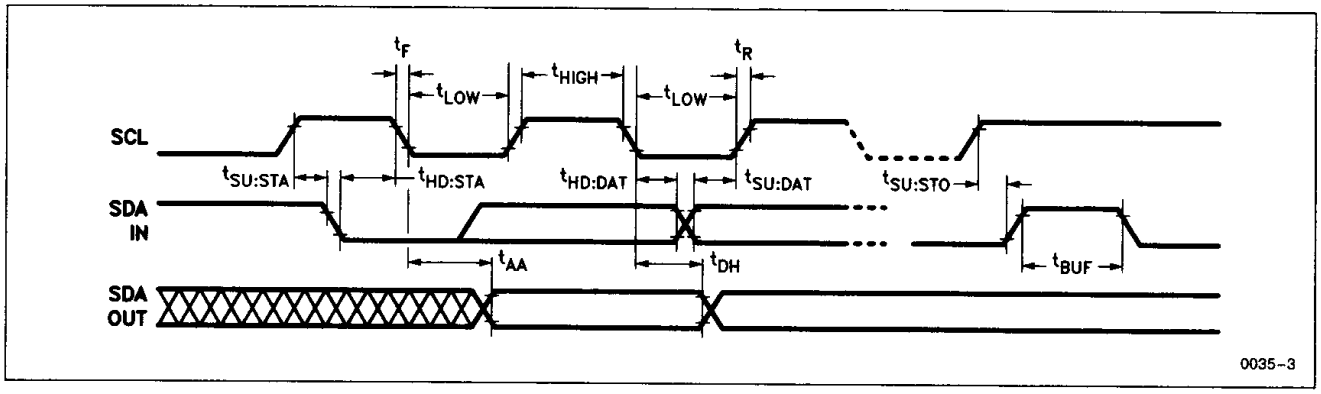
Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5	µs
t_{BUF}	Time the Bus Must be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t_{WR}	Write Cycle Time		5	10	ms

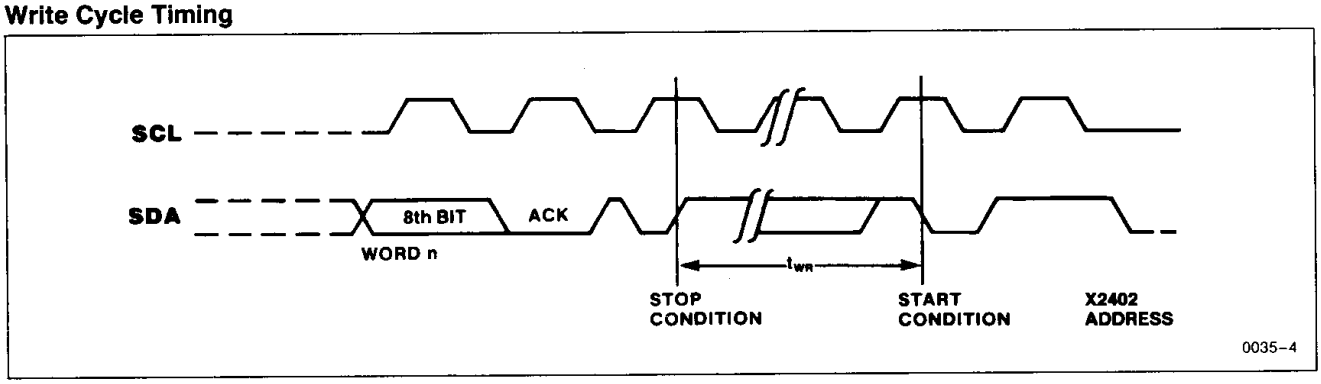
The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X2402 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Bus Timing



Note: (5) Typical values are for T_A = 25°C and nominal supply voltage.

Write Cycle Timing



PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

Address (A_0, A_1, A_2)

The Address inputs are used to set the least significant three bits of the seven bit slave address. The inputs are static, and should be tied HIGH or LOW, forming one unique address per device.

DEVICE OPERATION

The X2402 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X2402 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indication start and stop conditions. Refer to Figures 1 and 2.

Figure 1: Data Validity

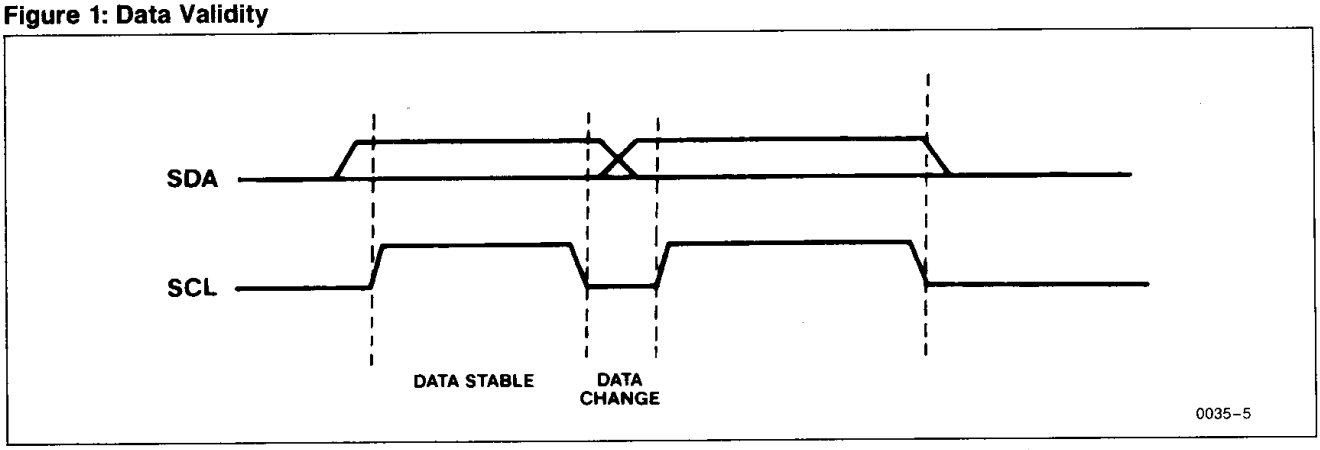
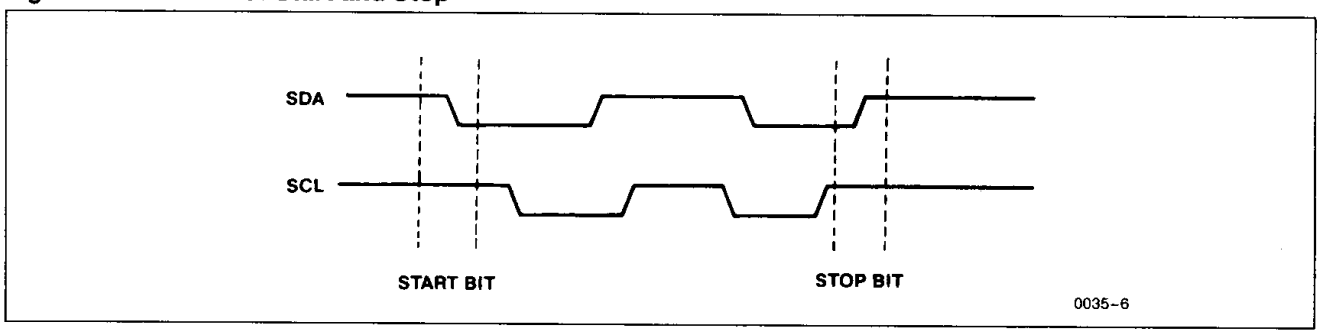


Figure 2: Definition of Start and Stop



Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X2402 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

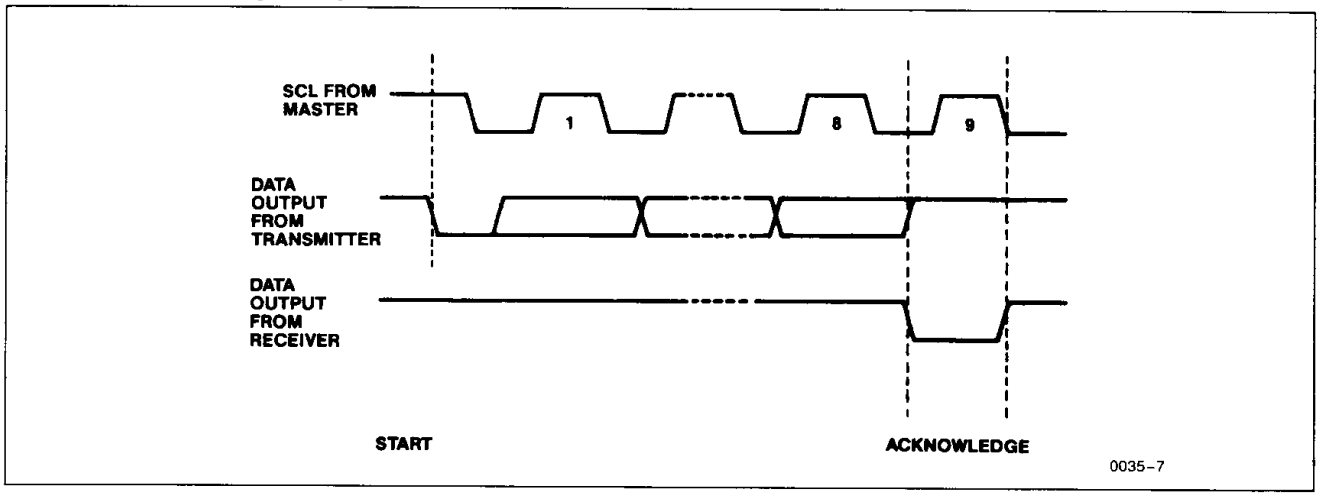
All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH.

Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X2402 will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X2402 will respond with an acknowledge after the receipt of each subsequent eight bit word.

Figure 3: Acknowledge Response from Receiver

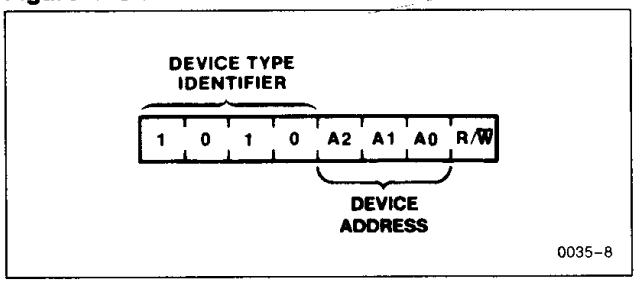


In the read mode the X2402 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X2402 will continue to transmit data. If an acknowledge is not detected, the X2402 will terminate further data transmissions and await the stop condition.

DEVICE ADDRESSING

Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Figure 4). For the X2402 this is fixed as 1010[B].

Figure 4: Slave Address



The next three significant bits address a particular device. A system could have up to eight X2402 devices on the bus (see Figure 10). The eight addresses are defined by the state of the A_0, A_1 and A_2 inputs.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected; when set to zero a write operation is selected.

Following the start condition, the X2402 monitors the SDA bus comparing the slave address being transmitted with its address (device type and state of A_0, A_1 and A_2 inputs). Upon a compare the X2402 outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the X2402 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X2402 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 256 words of memory. Upon receipt of the word address the X2402 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X2402 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X2402 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5: Byte Write

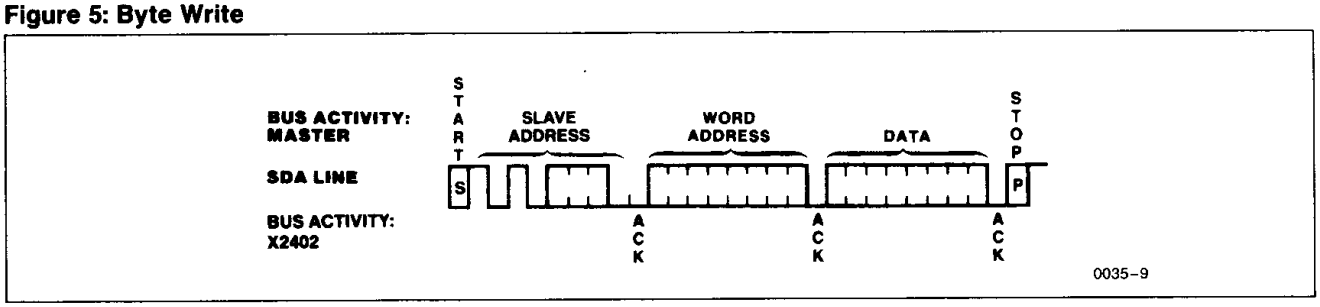
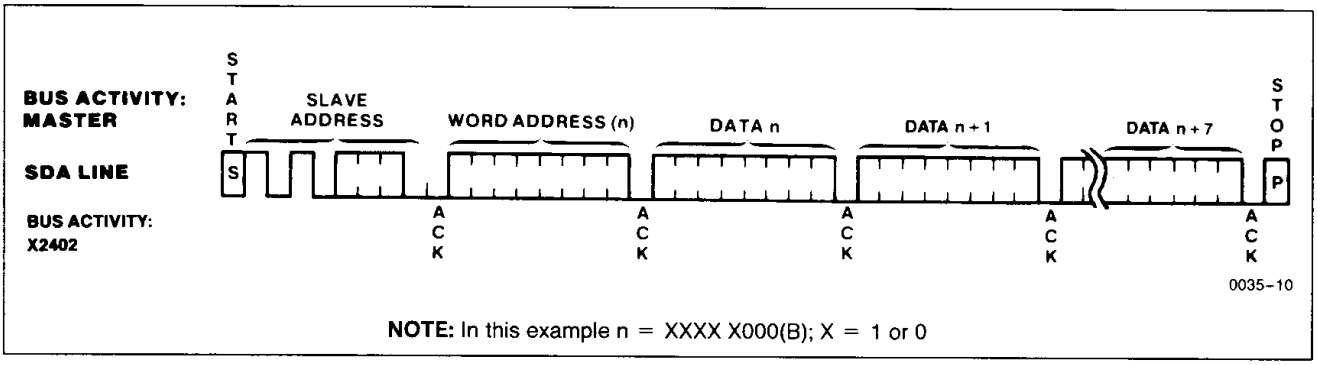


Figure 6: Page Write



NOTE: In this example n = XXXX X000(B); X = 1 or 0

Page Write

The X2402 is capable of an eight byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to seven more words. After the receipt of each word, the X2402 will respond with an acknowledge.

After the receipt of each word, the three low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X2402 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the X2402 is still busy with the write operation no ACK will be returned. If the X2402 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

Current Address Read

Internally the X2402 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n+1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the X2402 issues an acknowledge and transmits the eight bit word. The master does not acknowledge the transfer but does generate a stop condition and the X2402 discontinues transmission. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Figure 7: Current Address Read

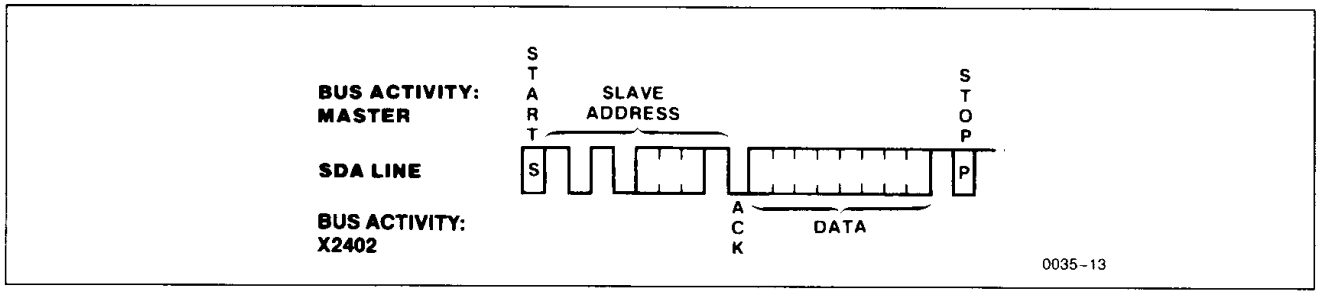
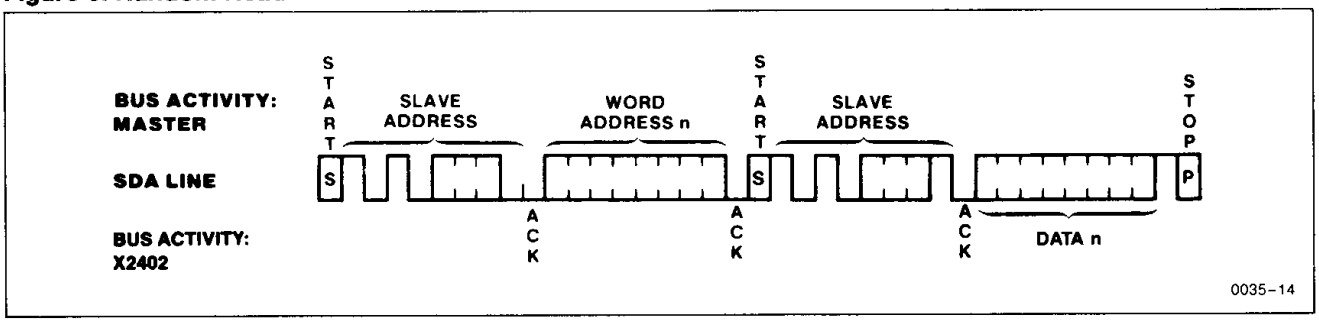


Figure 8: Random Read



Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the X2402 and then by the eight bit word. The master does not acknowledge the transfer but does generate a stop condition and the X2402 discontinues transmission. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as with the other read modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X2402 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge and generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all eight address bits, allowing the entire memory contents of the current 256 word page to be serially read during one operation. If more than 256 words are read, the counter "rolls over" and the X2402 continues to output data from the same 256 word page for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9: Sequential Read

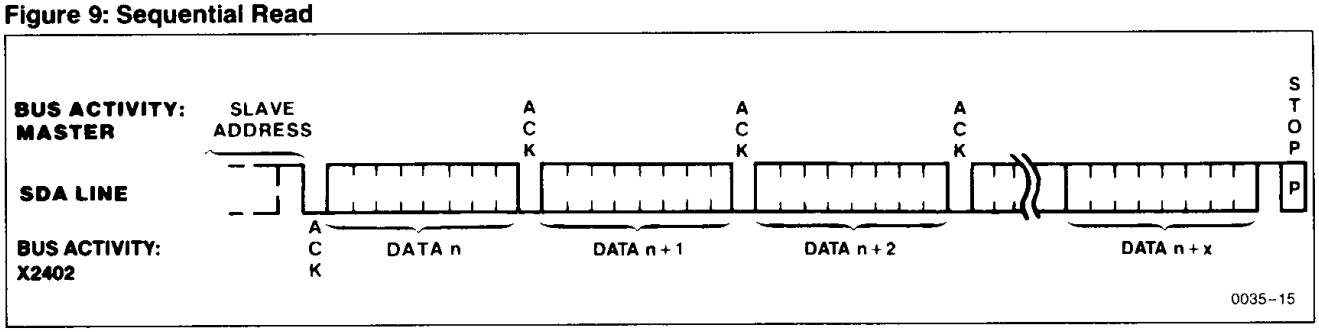
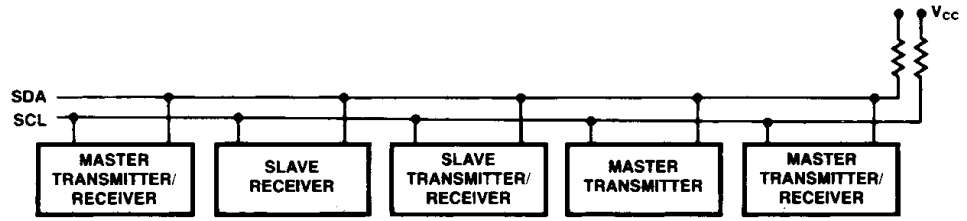


Figure 10: Typical System Configuration



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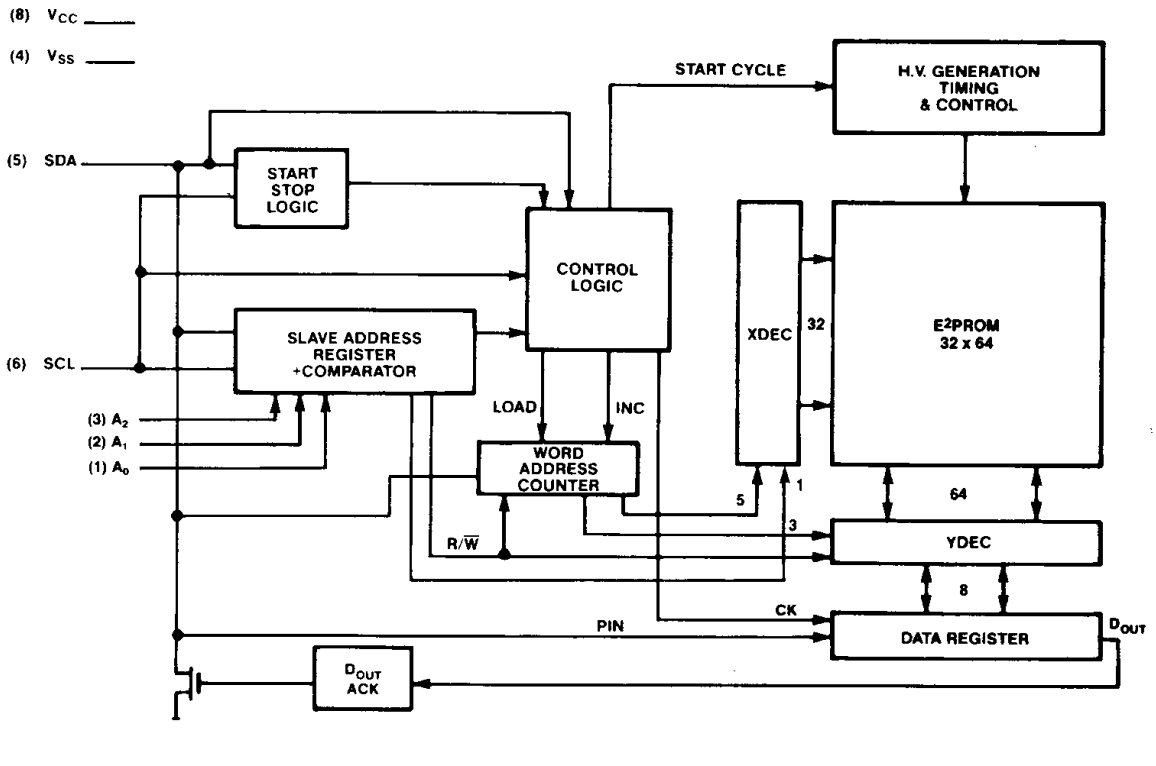
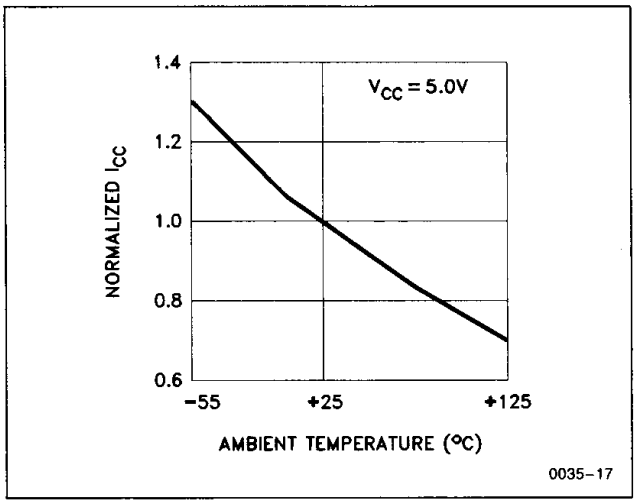
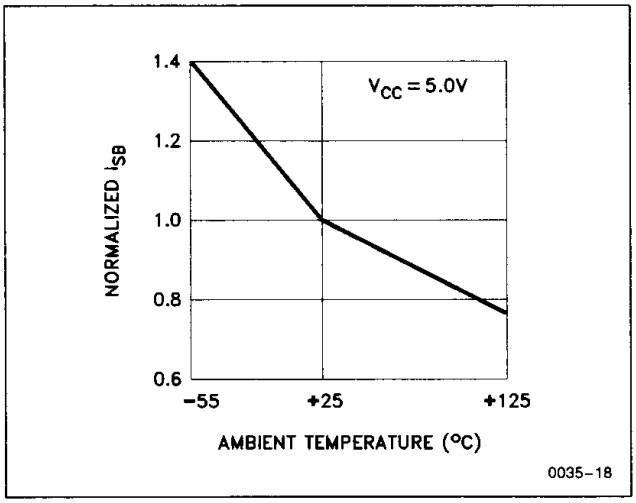
FUNCTIONAL DIAGRAM



Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance