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# 2SK2570

Silicon N-Channel MOS FET  
Low Frequency Power Switching

## HITACHI

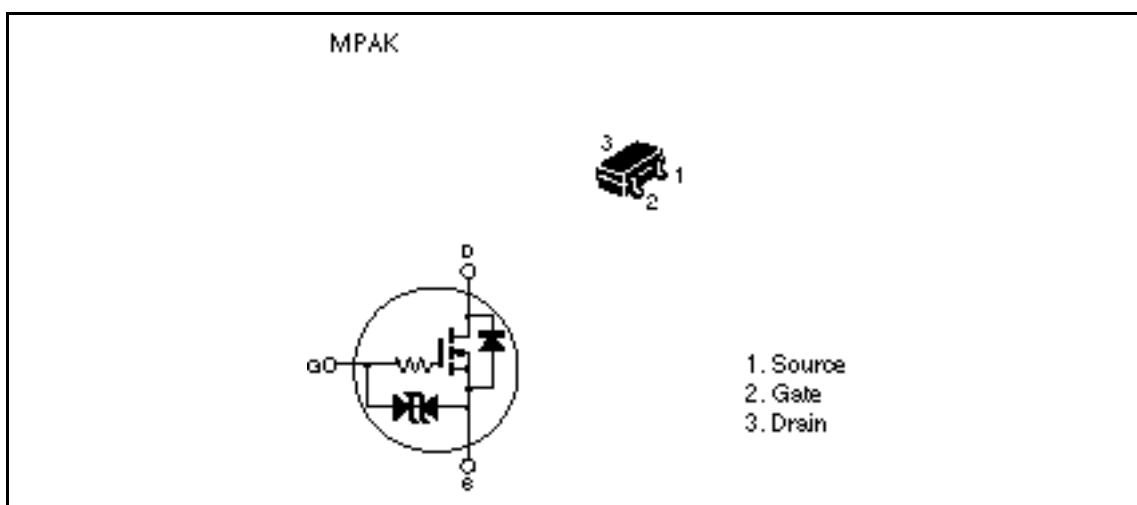
ADE-208-574  
1st. Edition

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### Features

- Low on-resistance  
 $R_{DS(on)} = 0.8 \text{ } \Omega$  typ. ( $V_{GS} = 4 \text{ V}$ ,  $I_D = 100 \text{ mA}$ )
- 2.5V gate drive devices.
- Small package (MPAK)

### Outline



## 2SK2570

### Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	20	V
Gate to source voltage	$V_{GSS}$	$\pm 10$	V
Drain current	$I_D$	0.2	A
Drain peak current	$I_{D(pulse)}^{*1}$	0.4	A
Channel dissipation	Pch	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

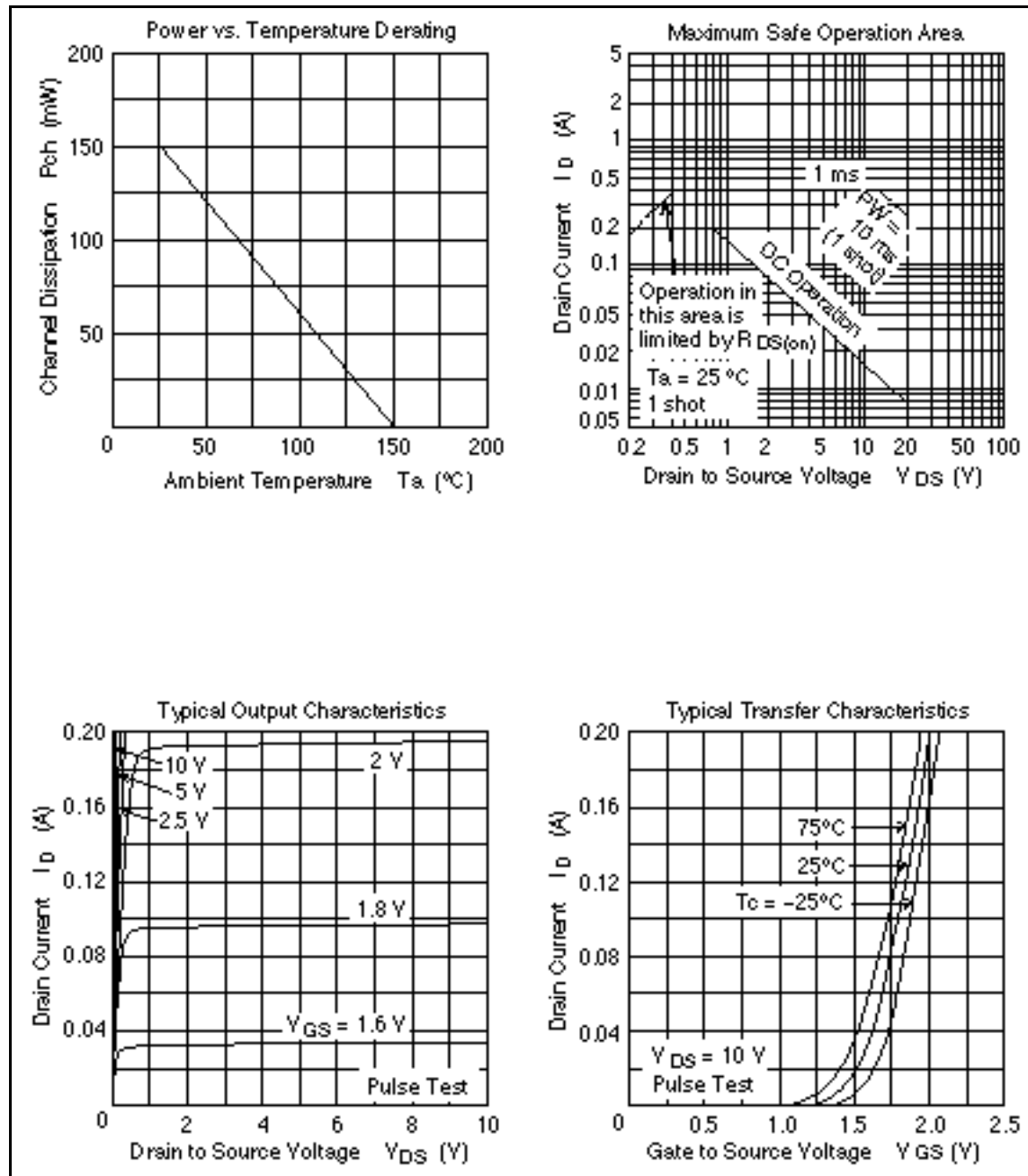
Note: 1. PW 10μs, duty cycle 1 %

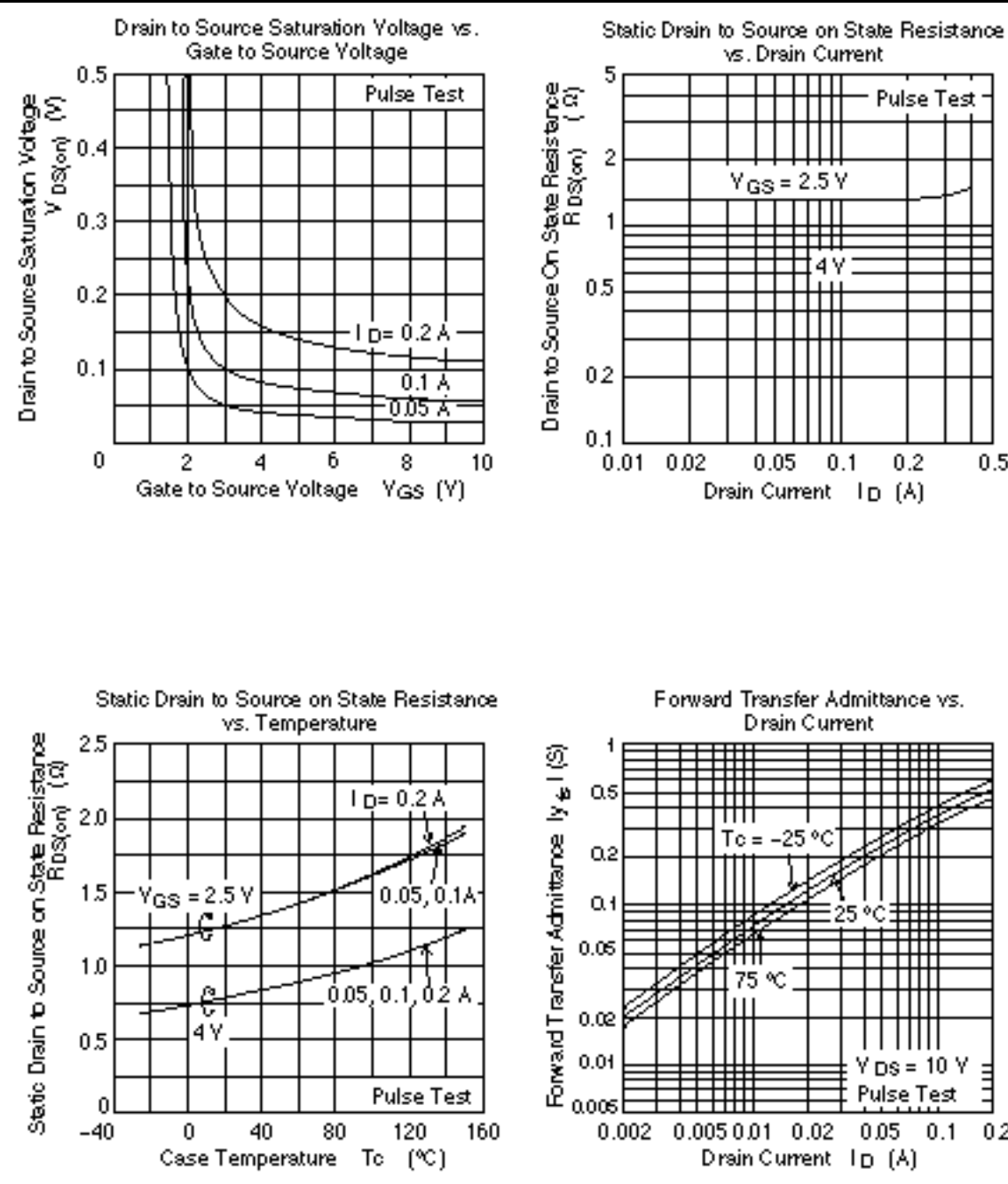
### Electrical Characteristics (Ta = 25°C)

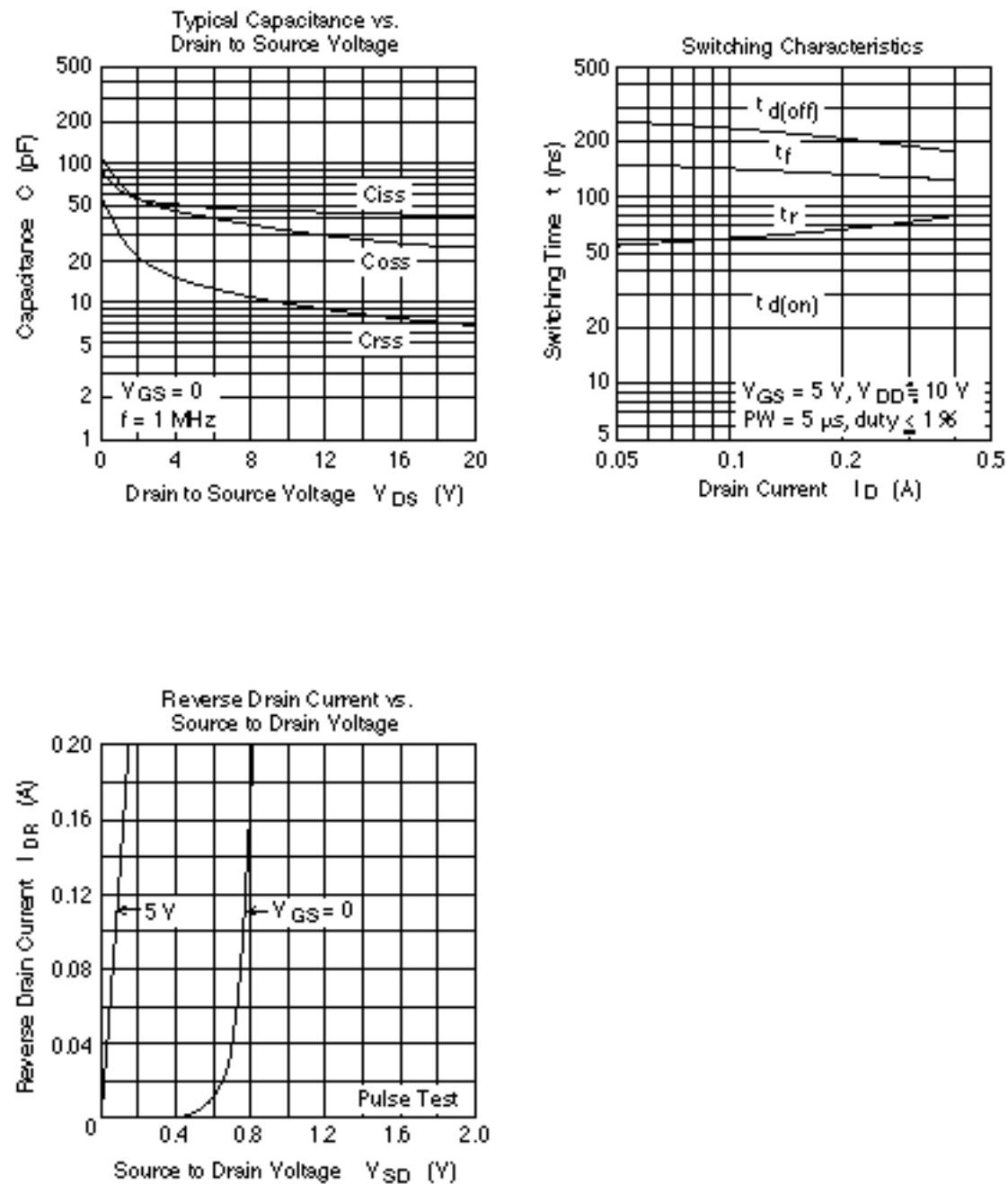
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	$I_D = 10\mu A, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 10$	—	—	V	$I_G = \pm 100\mu A, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1.0	μA	$V_{DS} = 20 V, V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 5.0$	μA	$V_{GS} = \pm 6.5 V, V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	$I_D = 10\mu A, V_{DS} = 5 V$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.8	1.1		$I_D = 100 mA$
						$V_{GS} = 4 V^{*1}$
			1.3	2.2		$I_D = 40 mA$ $V_{GS} = 2.5 V^{*1}$
Forward transfer admittance	$ y_{fs} $	0.22	0.35	—	S	$I_D = 100 mA$ $V_{DS} = 10 V^{*1}$
Input capacitance	Ciss	—	45	—	pF	$V_{DS} = 10 V$
Output capacitance	Coss	—	33	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	9.6	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$V_{GS} = 5 V, I_D = 100 mA$
Rise time	$t_r$	—	60	—	ns	$R_L = 100$
Turn-off delay time	$t_{d(off)}$	—	240	—	ns	
Fall time	$t_f$	—	140	—	ns	

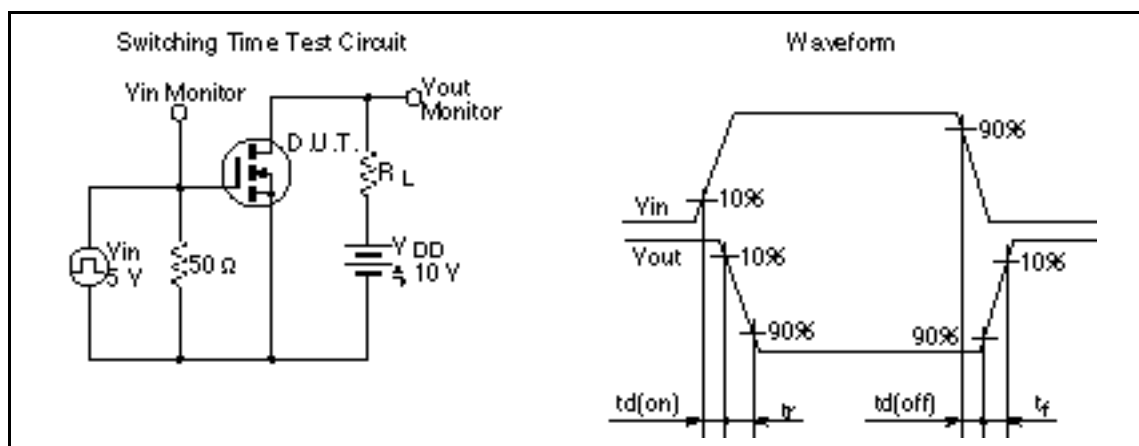
Notes: 1. Pulse test  
2. Marking is "ZL—"

## Main Characteristics



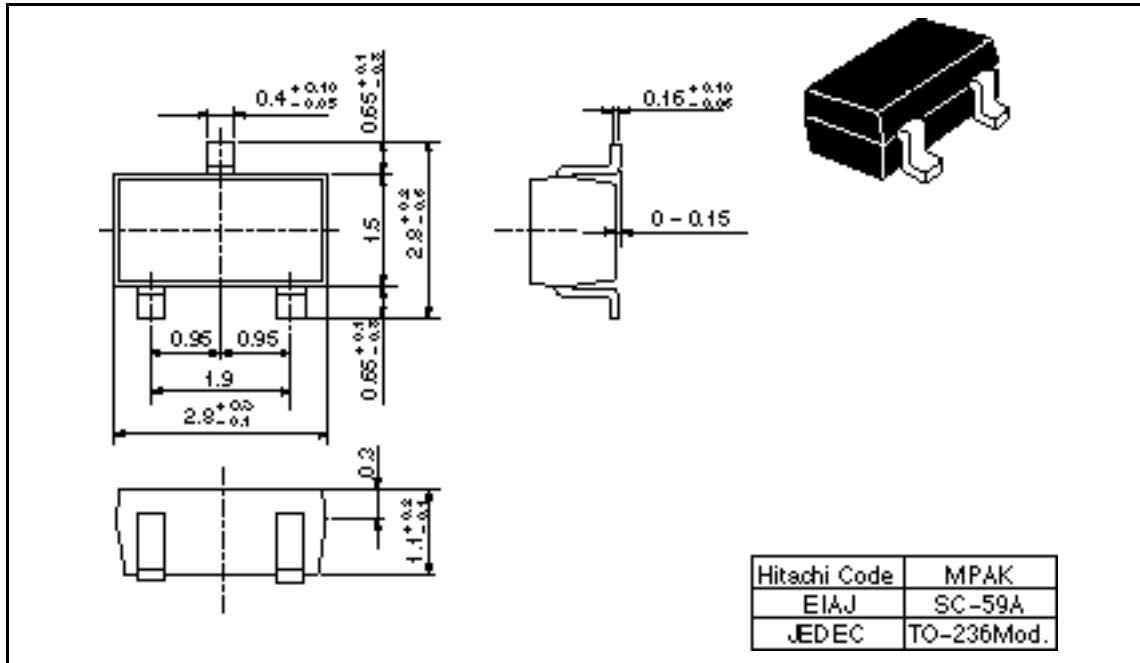






# Package Dimensions

Unit: mm



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# HITACHI

## **Hitachi, Ltd.**

Semiconductor & IC Div.

Nippon Bldg., 2-6-2, Ohite-machi, Chiyoda-ku, Tokyo 100, Japan

Tel Tokyo (03) 3270-2111

Fax (03) 3270-5109

For further information write to:

**Hitachi America, Ltd.**

Semiconductor & IC Div.

2000 Sierra Point Parkway

Brisbane, CA 94005-4835

U.S.A.

Tel 415-589-8300

Fax 415-589-4207

**Hitachi Europe GmbH**

Electronic Components Group

Continental Europe

Danewicher Straße 3

D-85522 Feldkirchen

München

Tel 089-9 94 80-0

Fax 089-9 29 30 00

**Hitachi Europe Ltd.**

Electronic Components Div.

Northern Europe Headquarters

Whitebrook Park

Lower Cookham Road

Marlow

Berkshire SL6 8YA

United Kingdom

Tel 0628-585000

Fax 0628-778322

**Hitachi Asia Pte. Ltd.**

45 Collyer Quay #20-00

Hitachi Tower

Singapore 04104

Tel 535-2400

Fax 535-1533

**Hitachi Asia (Hong Kong) Ltd.**

Unit 706, North Tower,

World Finance Centre

Harbour City, Canton Road

Tsim Sha Tsui, Kowloon

Hong Kong

Tel 27359218

Fax 27308074

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