24-26.5GHz Low Noise Amplifier

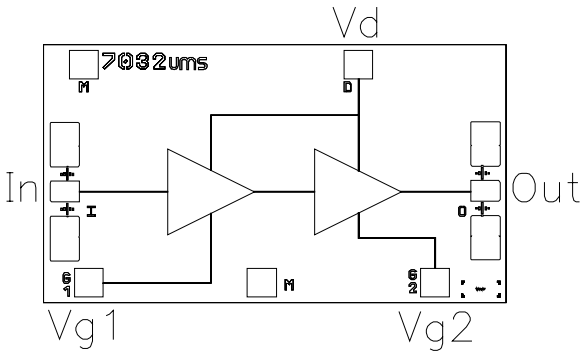
GaAs Monolithic Microwave IC

preliminary

Description

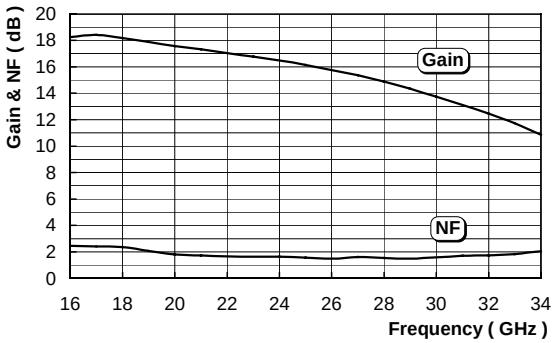
The CHA2192 is a two stages low noise amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

The circuit is manufactured with a HEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Main Features

- 1.8 dB noise figure
- 15 dB ± 1dB gain
- 10 dBm output power
- Very good broadband input matching
- DC power consumption, 40mA @ 3.5V
- Chip size : 1.67 x 0.97 x 0.10 mm



Typical on Wafer Measurements

Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	24		26.5	GHz
G	Small signal gain	14	15		dB
NF	Noise figure		1.8	2.0	dB
P1dB	Output power at 1dB gain compression	8	10		dBm

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

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Electrical Characteristics for Broadband Operation

Tamb = +25°C, Vd = 3.5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	24		26.5	GHz
G	Small signal gain (1)	14	15		dB
ΔG	Small signal gain flatness (1)		±1.0		dB
Is	Reverse isolation (1)		30		dB
NF	Noise figure		1.8	2.0	dB
P1dB	Pulsed output power at 1dB compression (1)	8	10		dBm
VSWRin	Input VSWR (1)			2.0:1	
VSWRout	Output VSWR (1)			2.0:1	
Id	Bias current		40	60	mA

(1) These values are representative for pulsed on-wafer measurements that are made without bonding wires at the RF ports.

Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.0	V
Id	Drain bias current	150	mA
Vg	Gate bias voltage	-2.0 to +0.4	V
Pin	Maximum peak input power overdrive (2)	+15	dBm
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +155	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

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Typical On Wafer Scattering Parameters and Noise Figure

Bias Conditions : Vd = +3.5V, Id = 40 mA

Freq. GHz	S11 dB	S11 /°	S12 dB	S12 /°	S21 dB	S21 /°	S22 dB	S22 /°	NF
1	-0,11	-15,4	-73,89	58,1	-30,22	153,9	-0,46	-24,8	
2	-0,14	-30,7	-74,53	35,2	-32,18	112,1	-1,19	-48,2	
3	-0,15	-45,8	-70,24	3,8	-36,24	88,2	-2,30	-68,3	
4	-0,18	-61,2	-81,19	41,8	-48,79	92,5	-3,30	-86,2	
5	-0,22	-76,4	-73,30	31,0	-36,60	-160,2	-4,78	-104,3	
6	-0,26	-92,1	-59,10	-38,8	-25,44	11,8	-5,35	-103,2	
7	-0,33	-107,7	-66,55	-77,6	-17,39	-49,1	-5,98	-124,0	
8	-0,42	-124,1	-62,12	-115,8	-7,82	-73,1	-7,15	-138,5	
9	-0,62	-140,9	-60,15	172,5	1,09	-105,1	-9,06	-150,3	
10	-0,86	-157,3	-54,22	112,5	7,90	-151,2	-11,46	-151,2	
11	-0,79	-175,1	-49,02	44,8	11,29	162,0	-11,65	-145,7	
12	-0,72	162,9	-45,15	10,1	13,12	126,0	-11,54	-150,2	
13	-0,92	136,4	-41,76	-22,0	14,80	96,0	-11,99	-154,2	
14	-1,52	104,7	-38,85	-49,6	16,38	67,0	-12,57	-155,9	
15	-2,68	67,2	-36,59	-75,1	17,54	37,5	-12,53	-156,1	
16	-4,24	24,8	-34,81	-99,7	18,09	8,7	-12,65	-158,0	2,45
17	-5,70	-19,6	-33,78	-121,4	18,21	-17,0	-11,76	-161,0	2,41
18	-6,70	-59,7	-33,16	-140,0	17,92	-40,7	-12,19	-167,8	2,36
19	-7,06	-92,2	-32,74	-154,3	17,56	-60,8	-12,76	-174,9	2,08
20	-7,30	-117,7	-32,23	-167,8	17,23	-78,9	-13,95	-174,2	1,79
21	-7,86	-138,8	-31,82	-179,5	16,98	-96,5	-15,34	-178,3	1,72
22	-8,82	-155,5	-31,31	172,5	16,66	-113,0	-16,56	-162,6	1,66
23	-10,02	-165,5	-30,23	161,5	16,42	-128,7	-16,82	-160,7	1,64
24	-11,19	-168,9	-29,72	150,2	16,20	-144,6	-16,08	-144,0	1,63
25	-11,90	-168,4	-29,12	139,6	15,88	-160,2	-16,06	-138,8	1,56
26	-11,60	-163,0	-28,62	128,6	15,51	-175,2	-14,23	-130,9	1,49
27	-10,37	-161,7	-28,30	117,8	15,14	170,0	-13,06	-130,4	1,60
28	-8,73	-165,0	-28,02	106,9	14,66	155,1	-11,23	-127,6	1,58
29	-7,20	-172,1	-27,90	96,6	14,11	140,7	-10,29	-131,8	1,65
30	-6,30	179,4	-27,92	87,0	13,48	127,2	-9,22	-134,4	1,44
31	-5,14	169,7	-27,87	78,6	12,82	113,8	-8,51	-140,7	1,80
32	-4,39	159,2	-27,95	67,9	12,10	100,8	-7,82	-140,5	1,56
33	-3,68	148,6	-28,04	59,8	11,34	88,0	-7,48	-148,2	1,67
34	-3,28	138,2	-28,28	51,7	10,44	76,1	-6,85	-148,1	1,73
35	-2,83	127,8	-28,28	42,5	9,56	64,1	-6,58	-156,0	1,92
36	-2,55	118,2	-28,51	34,7	8,63	53,4	-6,37	-155,3	2,17
37	-2,20	108,3	-29,15	26,3	7,70	43,1	-6,16	-161,7	
38	-1,94	98,5	-29,22	21,9	6,75	33,5	-6,17	-161,3	
39	-1,89	89,3	-29,80	13,5	5,76	24,0	-5,73	-167,2	
40	-1,54	80,2	-30,02	10,8	4,94	14,9	-6,01	-167,7	

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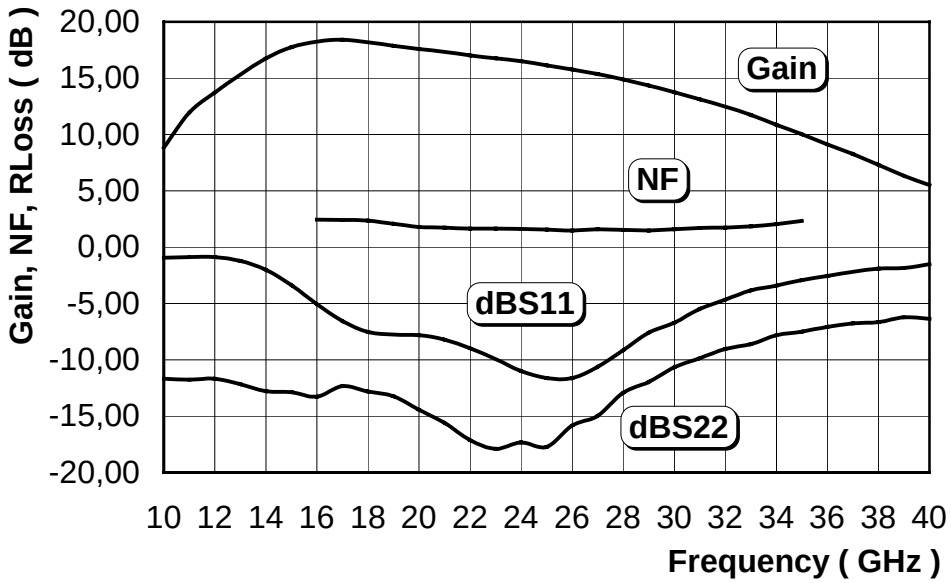
Typical on Wafer Measurements

Bias conditions: Vd=3.5V, Id= 40mA



Typical Bias Tuning for Low Noise Operation

For low noise operation, a separate access to the gate voltages of the input stage (Vgs1) and of the output stage (Vgs2) is provided.
Nominal bias for low noise operation is obtained for a typical current of 20 mA for the output stage and 10 mA for the input stage (30 mA for the amplifier).
The first step to bias the amplifier is to tune the Vgs1 = -1V, and Vgs2 to drive 20 mA for the full amplifier. Then Vgs1 is reduced to obtain 30 mA of current through the amplifier.
A fine tuning of the noise figure may be obtained by modifying the Vgs1 bias voltage, but keeping the previous value for Vgs2.

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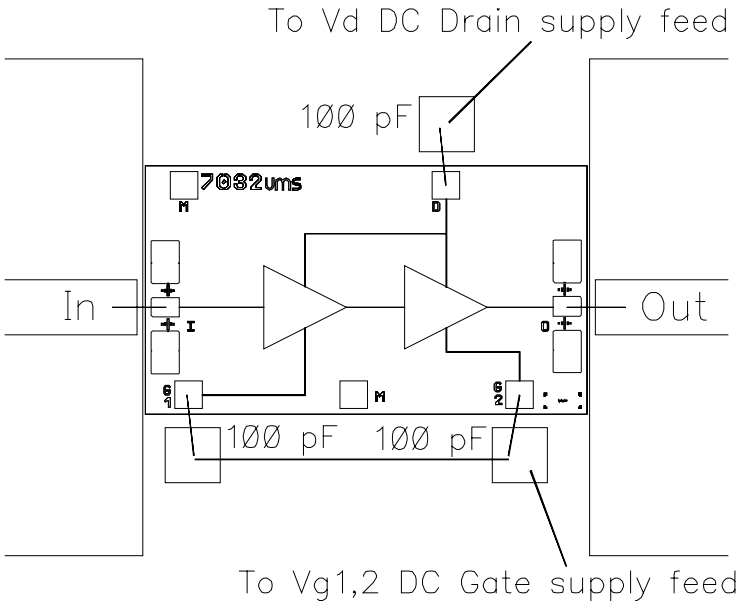
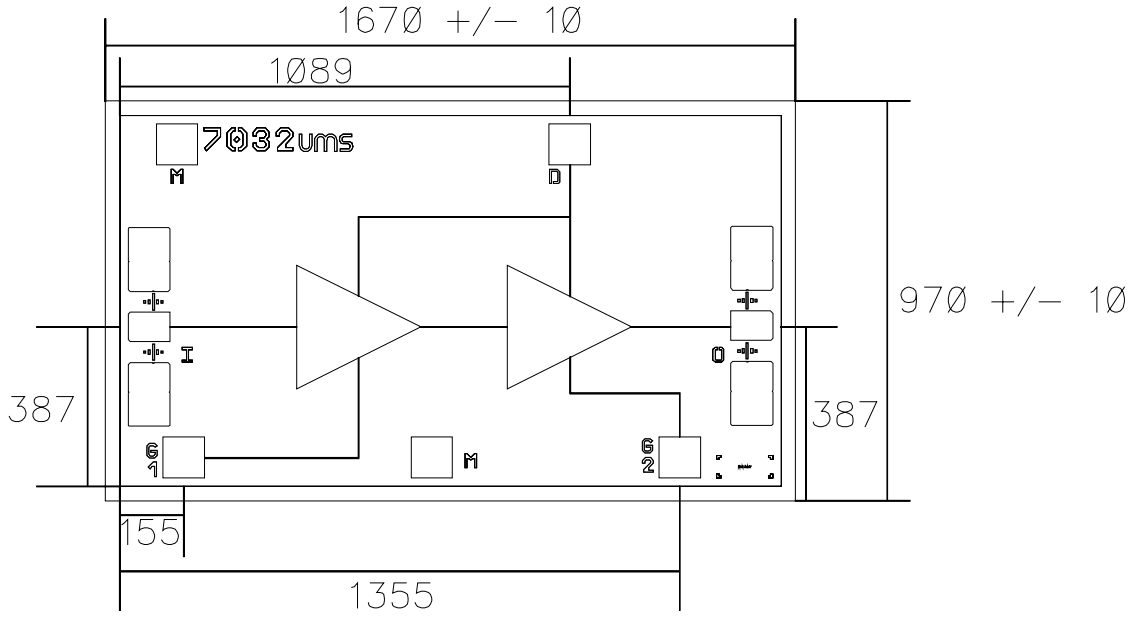
Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is to be prefered.



Bonding pad positions.

(Chip thickness : 100µm. All dimensions are in micrometers)

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Ordering Information

Chip form : CHA2192-99F/00

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