

CMOS 8-bit Single Chip Microcomputer

Piggyback/
evaluator type

Description

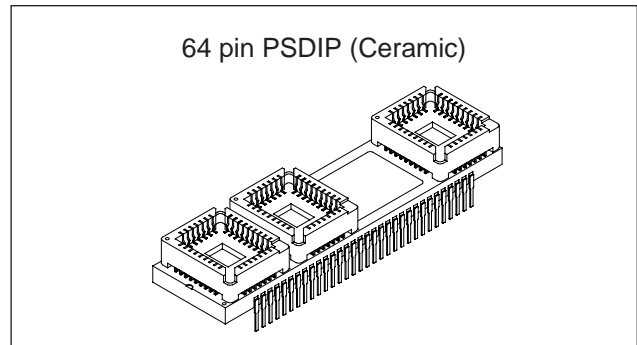
The CXP85890A is a CMOS 8-bit single chip micro-computer of biggyback/evaluator combined type, which is developed for evaluating the function of the CXP85840A/ 85848A/ 85856A.

For the CXP85890A, the custom font is supported.

Features

- A wide instruction set (213 instructions) which covers various types of data
 - 16-bit operation/multiplication and division/ Boolean bit operation instructions
- Minimum instruction cycle 333ns at 12MHz operation
- Applicable EPROM LCC type 27C512 (Maximum 56K bytes are available.)
- Incorporated RAM 2176 bytes (Excludes closed caption decoder and VRAM for on-screen display)
- EPROM for custom font LCC type 27C512 (Maximum 6K bytes are available.)
- Peripheral functions
 - A/D converter 8-bit 6-channel successive approximation method (Conversion time of 26.7 μ s at 12MHz)
 - Serial interface 8-bit clock sync type, 1 channel
 - Timer 8-bit timer
8-bit timer/counter
19-bit time-base timer
 - Closed caption decoder Data slicer
Corresponds to FCC (EDS supported), 8 \times 13 dots, 192 character types
15 character colors, 4 lines \times 34 characters
frame background 15 colors/ half blanking
italic, underline, vertical scrolling
 - On-screen display (OSD) function 12 \times 16 dots, 192 character types, 15 character colors
2 lines \times 24 characters
frame background 8 colors/ half blanking
background on full screen 15 colors/ half blanking
edging and vertical scrolling for every line
jitter elimination circuit
sprite OSD, 12 \times 16 dots, 1 screen, 8 colors for every dot
 - I²C bus interface
 - PWM output 8 bits, 8 channels
 - Remote control reception circuit 8-bit pulse measurement counter, 6-stage FIFO
 - HSYNC counter 2 channels
 - Watchdog timer
- Interruption 15 factors, 15 vectors, multi-interruption possible
- Standby mode Sleep
- Package 64-pin ceramic PSDIP (Supports custom font)

Note) Mask option is fixed by the CXP85890A. Refer to the Products List for details.



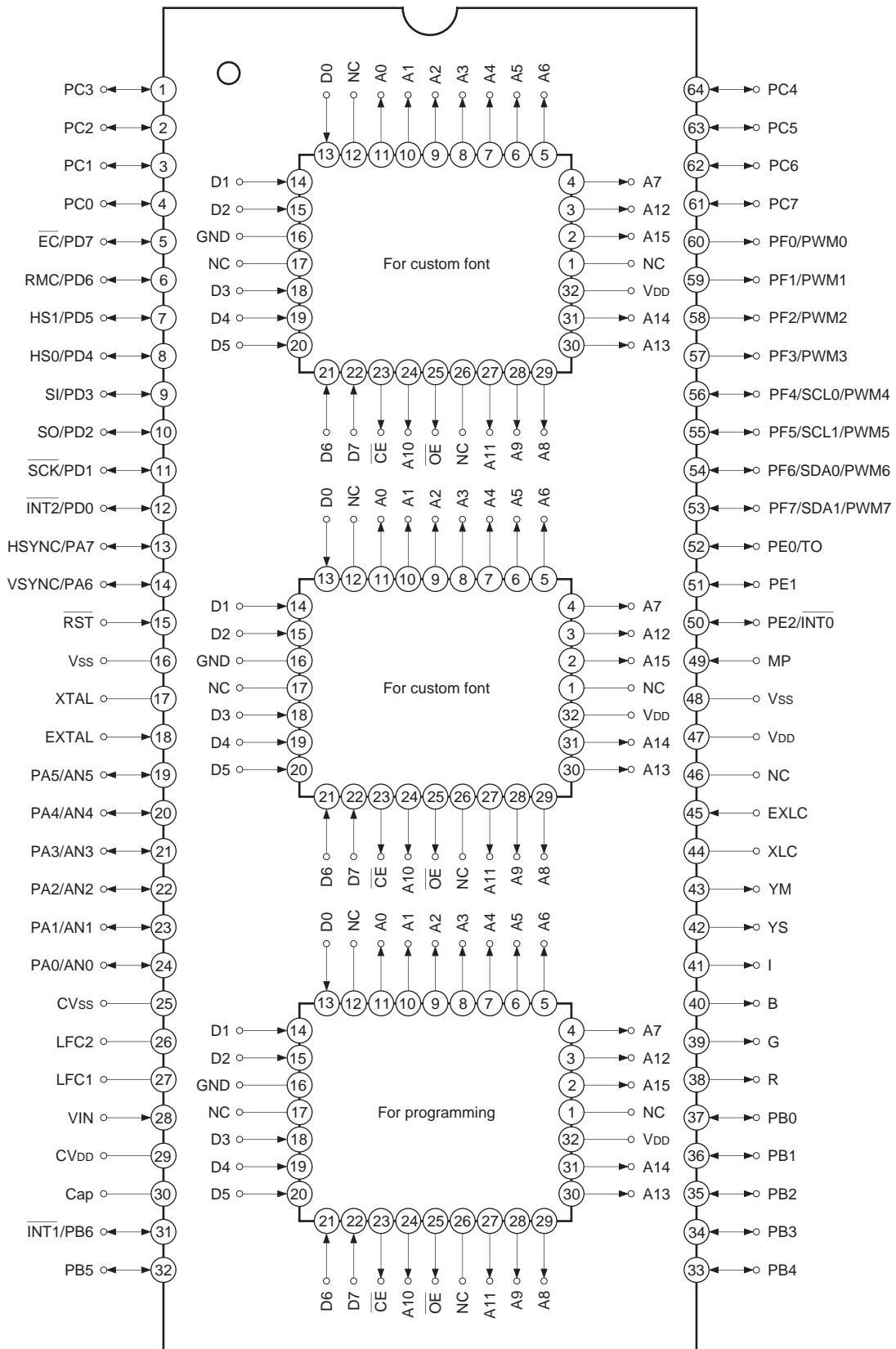
Structure

Silicon gate CMOS IC

Purchase of Sony's I²C components conveys a licence under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specifications as defined by Philips.

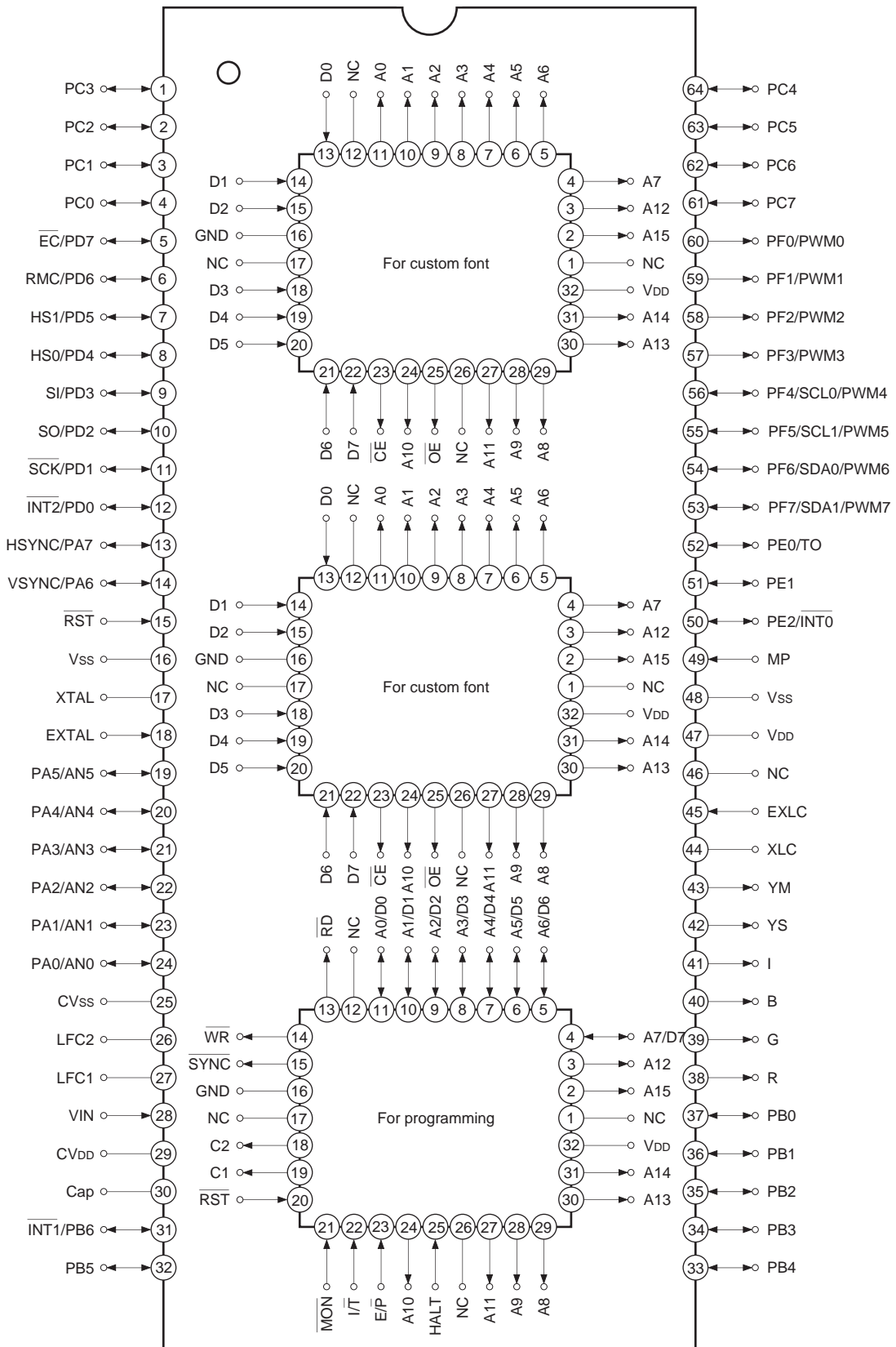
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Pin Assignment in Piggyback Mode (Top View)



- Note)**
1. NC (Pin 46) is always connected to V_{DD}.
 2. V_{SS} (Pins 16 and 48) are both connected to GND.
 3. MP (Pin 49) is always connected to GND.

Pin Assignment in Evaluator Mode (Top View)

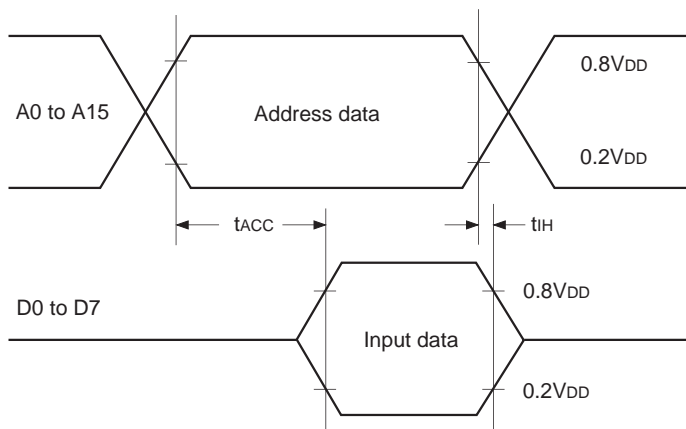


- Note)**
1. NC (Pin 46) is always connected to VDD.
 2. Vss (Pins 16 and 48) are both connected to GND.
 3. MP (Pin 49) is always connected to GND.

EPROM Read Timing

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

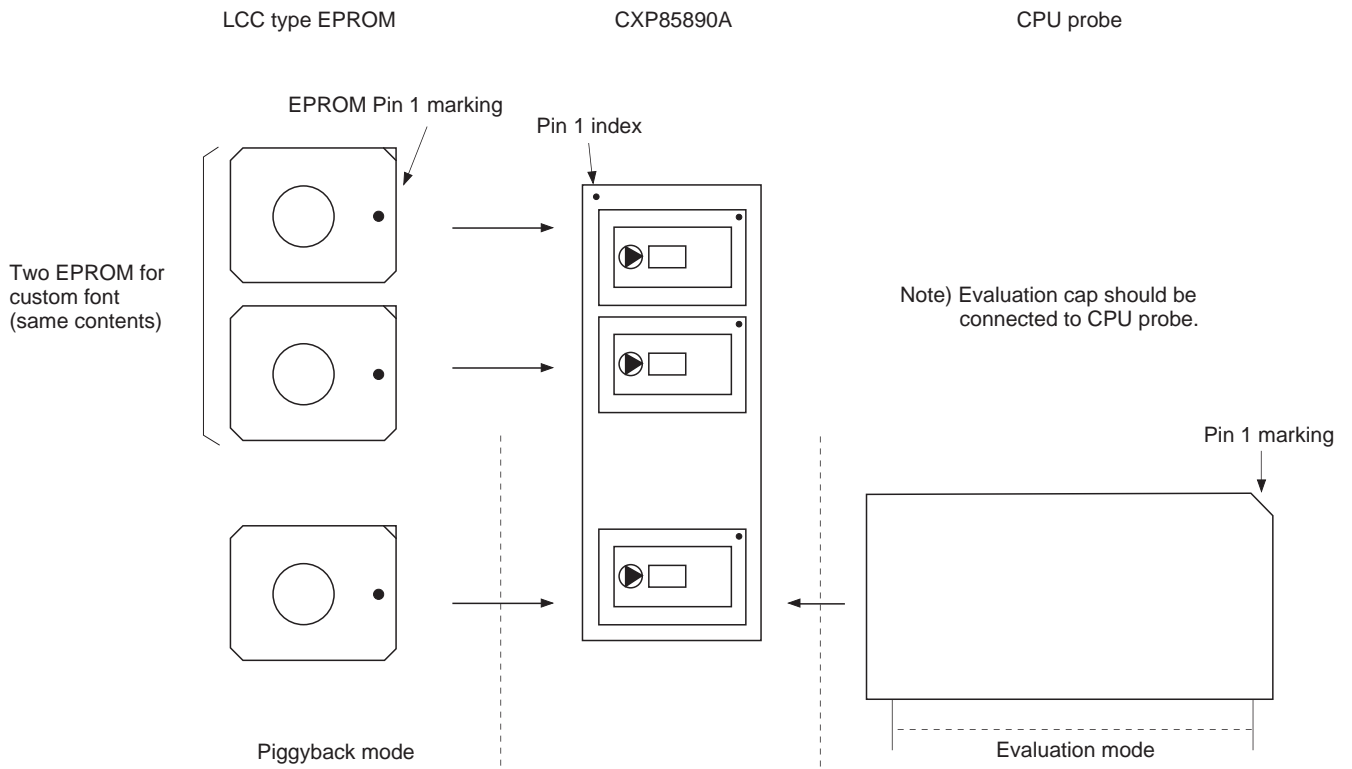
Item	Symbol	Pin	Min.	Max.	Unit
Address → Data input delay time	t_{ACC}	A0 to A15 D0 to D7		100	ns
Address → Data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns



Product List

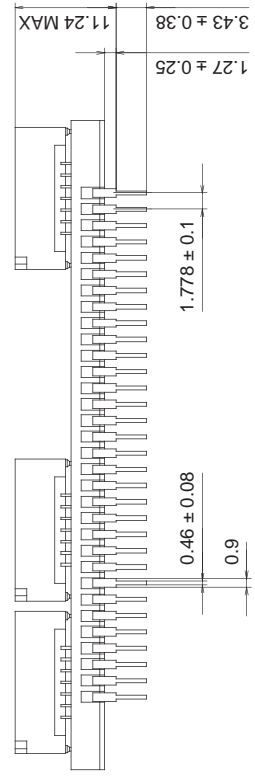
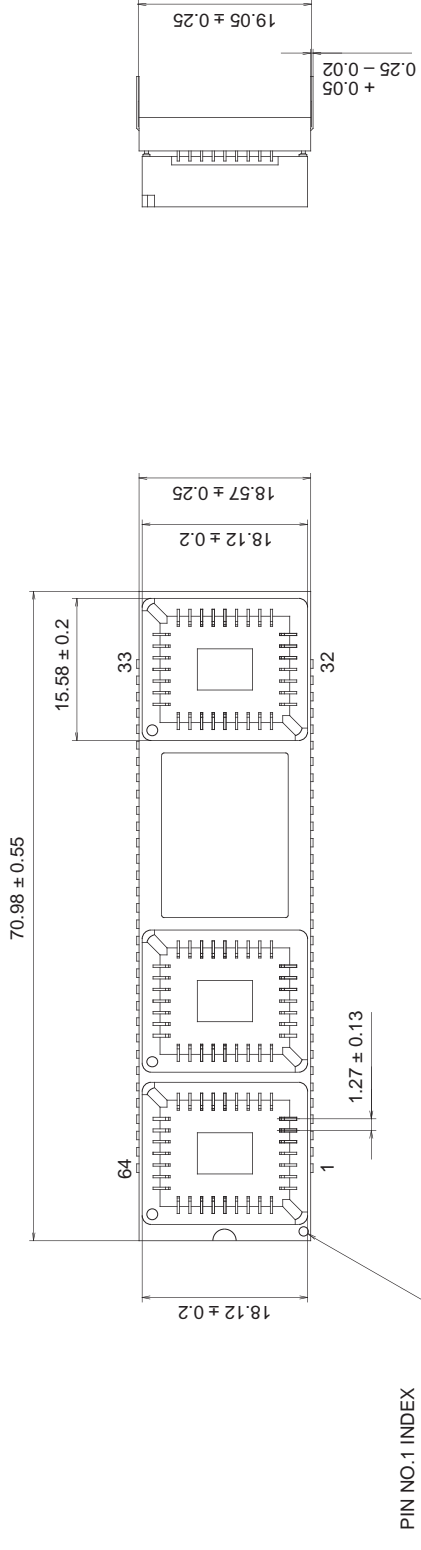
Option item	Products			
	Mask			Piggyback/evaluator
	CXP85840A	CXP85848A	CXP85856A	CXP85890A-U01S
Package	64-pin plastic SDIP			64-pin ceramic PSDIP
Oscillation clock	12MHz			
ROM capacity	40K bytes	48K bytes	56K bytes	EPROM 56K bytes
Reset pin pull-up resistor	Existent/Non-existent			Existent
Font data	User designation			EPROM 6K bytes

Piggyback mode/evaluator mode can be switched as shown below.



Package Outline Unit: mm

64PIN PSDIP (CERAMIC)



PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	22.8g

SONY CODE	PSDIP-64C-02
EIAJ CODE	ADIP064-C-0750-B
JEDEC CODE	