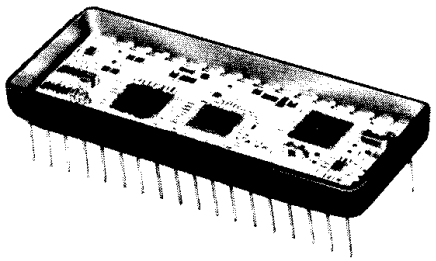
DDC
ILC DATA DEVICE CORPORATION

HSDC-8915 MONOBRID® SERIES*

14 BIT MONOLITHIC HYBRID S/D AND R/D TRACKING CONVERTERS



DESCRIPTION

The HSDC-8915 Monobrid® Series is the first complete 14-bit synchro-to-digital or resolver-to-digital converter contained in a single hybrid module. Most of its circuitry has been incorporated into a custom designed monolithic chip, thereby greatly reducing parts count inside the hybrid. The Monobrid combination of monolithic and hybrid technologies allows a more sophisticated design with better performance and additional features to fit inside a standard 36 pin DDIP hybrid package. Power consumption is reduced, reliability is increased, and costs are lower.

New features found in the HSDC-8915 Series are 3-state output in two bytes, and a transparent latch which allows the converter to keep tracking even while an Inhibit is being applied. Innovative features found in other recent DDC hybrid converters are also included, such as a ±2.6 minute high accuracy option, analog velocity signal, error voltage outputs, solid state signal and reference isolation, broadband input, and accommodation to non-standard line-to-line voltage levels.

The HSDC-8915 Series is available in two accuracy grades: ±4 minutes ±0,9 LSB and ±2,6 minutes. The accuracy is not affected by carrier amplitude variation because the conversion is ratiometric. Phase sensitive detection in the error loop rejects quadrature and noise. Adjustments and calibration are never required.

The HSDC-8915 Series accepts broadband inputs: 360 to 1000 Hz or 47 to 1000 Hz. Two kinds of input signal isolation are available: internal differential solid state input with high common mode rejection, and transformer isolation with external transformers. Output angle is natural binary code, parallel positive logic, and TTL/CMOS compatible. Synchronization to a computer is complete via a Converter Busy output and an Inhibit input.

Only one main power supply is required. Its +15V DC nominal level can range from +11 to +16.5 volts with no degradation in performance. The HSDC-8915 is also connected to the external logic power supply. Internal logic is CMOS, and all logic inputs and outputs are buffered to the external logic level. TTL or any external CMOS logic level between +4.5V and the +15V supply level can be accommodated.

APPLICATIONS

With three-state output and an Inhibit that does not stop the tracking process, HSDC-8915 Series converters are especially suited for bus multiplexing and interfacing with microprocessors. These converters are ideal for remotely located and hard to access equipment where low power requirements, small size, and high MTBF are critical. All units are processed to MIL-STD-883. They are well suited to the most stringent and severe industrial or military and avionics applications. In conjunction with other devices, they are easily adapted for closed loop control.

Designed for printed circuit board mounting by standard techniques, the HSDC-8915 Series can be readily incorporated into other equipment by the OEM user. Because of their low cost, they are competitive with discrete S/D converters in many applications.

FEATURES

- *10 RPS TRACKING*
- *LOW POWER:*
  150 mW, Typical
- *ACCURACY:*
  ±4 minutes ±0.9 LSB standard
  ±2.6 minutes high accuracy option
- *3-STATE LATCHED OUTPUTS FOR MICROPROCESSOR DATA BUS*
- *USABLE AS CONTROL TRANSFORMER (CT)*
- *INHIBIT DOES NOT INTERRUPT TRACKING*
- *LOGIC:*
  TTL and CMOS compatible 14 bit parallel binary angle
  Converter Busy and Inhibit
  Enable lines for 3-state output

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*Patented

Note: Monobrid® is a registered trademark of ILC Data Device Corporation.

HSDC 8915 MONOBRID SERIES SPECIFICATIONS

Over reference amplitude, temperature, and power supply ranges; 10% signal amplitude variation; and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE
RESOLUTION	14 bits
ACCURACY	
Normal Accuracy	±4.0 minutes ±0.9 LSB
High Accuracy Option "a"	±2.6 minutes max (total error)
REFERENCE INPUT	
Carrier Frequency Ranges	
Nominal 400 Hz Units	360 – 1000 Hz
Nominal 60 Hz Units	47 – 1000 Hz
Reference Input Characteristics	
Voltage Range	4 – 130V rms
Input Impedance	250 KΩ min, single ended 500 KΩ min, differential
Common Mode Range	DC common mode plus recurrent AC peak = 210V max
SYNCHRO/RESOLVER SIGNAL INPUTS	
SOLID STATE BUFFER INPUT MODULES	
Minimum Input Impedance (Balanced)	

Synchro	Z_{IN} Line to Line	Z_{IN} Each Line to GND
90V L-L (8918, 8919)	130 KΩ	85 KΩ
11.8V L-L (8917)	17.5 KΩ	11.5 KΩ

Resolver	Z_{IN} Single Ended	Z_{IN} Differential	Z_{IN} Each Line to GND
90V L-L (8922)	175 KΩ	350 KΩ	175 KΩ
26V L-L (8921)	50 KΩ	100 KΩ	50 KΩ
11.8V L-L (8920)	23 KΩ	46 KΩ	23 KΩ

Common Mode Ranges		
For 90V L-L Input	182V Max	DC common mode plus recurrent AC peak
For 26V L-L Input	60V Max	
For 11.8V L-L Input	60V Max	
VOLTAGE FOLLOWER BUFFER INPUT MODULES		
(For External Transformers)		
Input Signal Type	Sin and cos resolver signals referenced to converter internal reference V (not to external GND)	
Sin Cos Voltage Range	1V nominal, 1.15V max	
Max Voltage Without Damage	15V rms continuous, 100V peak transient	
Input Impedance	Z_{IN} > 10 MΩ (transient protected voltage follower)	
TRANSFORMER CHARACTERISTICS		
(See Ordering Information for List of Transformers. Reference Transformers are Optional for Both Solid State and Voltage Follower Input Options.)		
400 Hz TRANSFORMERS		
Reference Transformer		
Carrier Frequency Range	360 – 1000 Hz	
Voltage Range	18 – 130V	
Input Impedance	40 KΩ min	
Breakdown Voltage to GND	1200V peak	
Signal Transformer		
Carrier Frequency Range	360 – 1000 Hz	
Breakdown Voltage to GND	700V peak	
Minimum Input Impedances (Balanced)		

	Synchro Z_{IN} (Z_{SO})*	Resolver Z_{IN}
90V L-L (Option 4H)	180 KΩ	100 KΩ
26V L-L (Option 4M)	–	30 KΩ
11.8V L-L (Option 4L)	20 KΩ	30 KΩ

60 Hz TRANSFORMERS	
Reference Transformer	
Carrier Frequency Range	47 – 440 Hz
Input Voltage Range	80 – 138V rms, 115V rms nominal
Input Impedance	600 KΩ min, resistive
Input Common Mode Voltage	500V rms, transformer isolated
Output Description	+R (in phase with RH-RL) and -R (in phase with RL-RH) derived from op-amps. Short circuit proof.
Output Voltage	3.0V nominal riding on ground reference V. Output voltage level tracks input level.
Power Required	4 mA typ, 7 mA max from +15V supply.
Signal Transformer	
Carrier Frequency Range	47 – 440 Hz
Input Voltage Range	10 – 100V rms L-L; 90V rms L-L nominal
Input Impedance	148 KΩ min L-L balanced resistive
Input Common Mode Voltage	±500V rms, transformer isolated
Output Description	Resolver output, - sine (-S) and + cosine (+C) derived from op-amps. Short circuit proof.
Output Voltage	1.0V rms nominal riding on ground reference V. Output voltage level tracks input level.
Power Required	4 mA typ, 7 mA max from +15V supply.
DIGITAL INPUT/OUTPUT	
Logic Type	TTL/CMOS compatible, depending on logic supply voltage
Outputs	
14 Parallel Data Bits	Natural binary angle, positive logic
Converter Busy (CB)	0.5 – 2.0 µs positive pulse, leading edge initiates counter update
Drive Capability	1 Standard TTL load, 1.6 mA at 0.4 V_{max} (logic "0") 10 Standard TTL loads, 0.4 mA at 2.8 V (logic "1") 10 µA_{max} (high impedance).
Input	Z_{IN} ≥ 25 KΩ pull up resistor to V_L
Inhibit Input (INH)	INH – Logic 0 inhibits
Enable, Bits 1 to 6 (EN 1-6)	(EN 1-6) and (EN 7-14) – Logic 0 enables
Enable, Bits 7 to 14 (EN 7-14)	Logic 1 high impedance
S (Control Transformer) Logic Type	Logic 0 for use as CT
Loading	CMOS Compatible – Logic "0" ≤ 0.3 V_L "1" ≥ 0.7 V_L CMOS
ANALOG OUTPUTS	
Filtered DC Error Voltage (E) DC Velocity Voltage ($\dot{\theta}$)	–1 VDC per +LSB of error (±3 LSB range) +1 VDC per +2.1 rps at 400 Hz +1 VDC per +0.54 rps at 60 Hz
AC Error Voltage Near Null (e)	16 mV rms for +1 LSB of error (nominal input voltage)
Loading	1.0 mA)
DYNAMIC CHARACTERISTICS	
Input Rate	
At 400 Hz	0 to ±10 rps min
At 60 Hz	0 to ±2.5 rps min
Velocity Constant	K_V = ∞ (No limitation with Type II servo loop)
Acceleration Constant	
At 400 Hz	K_a = 65,000 sec^{-2} nominal
At 60 Hz	K_a = 1000 sec^{-2} nominal
Settling Time	
For 179° Step Change	
At 400 Hz	150 ms typ to 1 LSB 200 ms max to final value
At 60 Hz	350 ms typ to 1 LSB 400 ms max to final value
TEMPERATURE RANGES	
Operating	
–1 option	–55°C to +125°C
–3 option	0°C to +70°C
Storage	–55°C to +135°C

POWER SUPPLIES		
Nominal Voltage	+15 VDC	Logic Supply
Voltage Range	+11 to +16.5V	+4.5V to +15 supply
Absolute Max Voltage	+18V	+18V
Current or Impedance	15 mA max*	Z_{IN} = 5 KΩ min

*Does not include current required by 60 Hz active transformers

PHYSICAL CHARACTERISTICS	
Converter	
Type	36 pin double DIP
Size	0.78 x 1.9 x 0.21 inch (2.0 x 4.8 x 0.53 cm)
Weight	1 oz max (28 g)
400 Hz Transformer	
Type	Encapsulated module. Signal input uses 2 modules (T1A and T1B). Ref uses 1 module (T2)
Size	0.8 x 0.6 x 0.3 inch (2 x 1.5 x 0.8 cm)
Weight	0.4 oz max (11 g)
60 Hz Transformer	
Type	Encapsulated module. Signal transformer and reference transformer each consist of one such module
Size	1.125 x 1.125 x 0.42 inch (2.86 x 2.86 x 1.07 cm)
Weight	0.7 oz max (20 g)

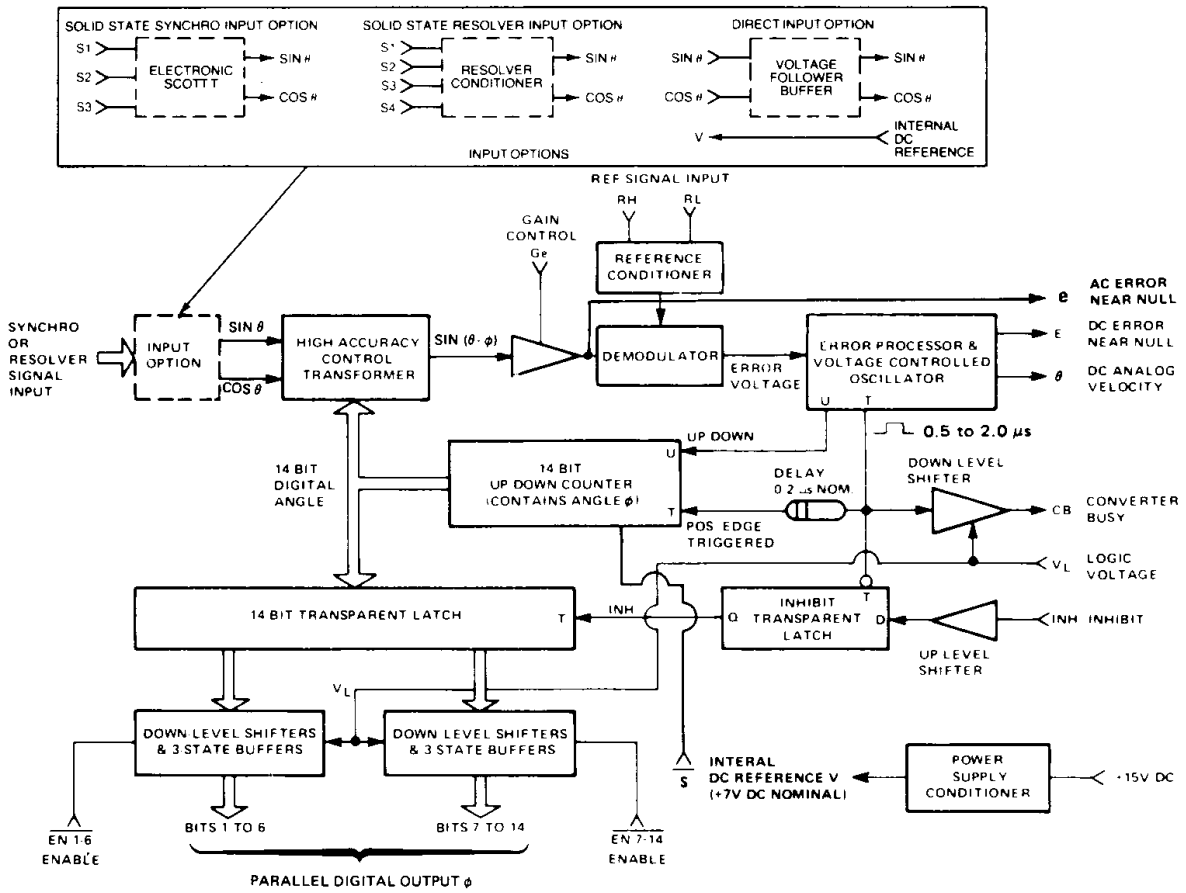


FIGURE 1. HSDC-8915 SERIES BLOCK DIAGRAM

TECHNICAL INFORMATION

INTRODUCTION

The circuit shown in the HSDC-8915 block diagram, Figure 1, consists of three main parts: the signal input option; a feedback loop whose elements are the control transformer, demodulator, error processor, and up-down counter; and digital interface circuitry including various latches and buffers.

The input options accept a synchro or resolver input and produce a resolver type output for the control transformer. The first two options, called solid state synchro and resolver input, accept synchro and resolver signal inputs directly, and provide signal isolation; it is a voltage follower buffer and requires an external signal conditioner such as a transformer. Both options, the solid state input and the external transformer isolated buffer, are available for the following standard inputs:

All input options are DC coupled with broadband characteristics up to 1000 Hz. HSDC-8915 Series converters are usable to 10 KHz with slight degradation in accuracy – consult factory for further information.

In a synchro or resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the terminals. The internal converter operates with signals in resolver format, $\sin\theta \cos\omega t$ and $\cos\theta \cos\omega t$. Synchro signals are of the form $\sin\theta \cos\omega t$, $\sin(\theta + 120^\circ)\cos\omega t$, and $\sin(\theta + 240^\circ)\cos\omega t$. Diagrams on the following page show synchro and resolver signals as a function of the angle θ.

The feedback loop produces a 14 bit digital angle Φ which tracks the analog input angle θ to within the specified accuracy of the converter. The control transformer performs the following trigonometric computation:

$$\sin(\theta - \Phi) = \sin\theta \cos\Phi - \cos\theta \sin\Phi$$

where θ is the angle representing the synchro or resolver shaft position, and Φ is the digital angle contained in the up-down counter in the converter. The tracking process consists of continually adjusting Φ to make $(\theta - \Phi) \rightarrow 0$, so that Φ will represent the shaft position θ.

The output of the demodulator is an analog DC level proportional to $\sin(\theta - \Phi)$. The error processor integrates this $\sin(\theta - \Phi)$ error signal, and the output of the integrator is used to control the frequency of a voltage controlled oscillator. This oscillator produces "clock" pulses which are accumulated by the up-down counter. The up-down counter is functionally an incremental integrator. Therefore there are two stages of integration, making the converter a Type II tracking servo. In a Type II servo, the voltage controlled oscillator always settles to a counting rate which makes $d\Phi/dt$ equal to $d\theta/dt$ without lag. The output data will always be fresh and available so long as the maximum tracking rate of the converter is not exceeded.

The digital interface circuitry has three main functions: to latch the output bits during an Inhibit command so that stable data can be read out, to furnish both 14 bit parallel and 3-state data formats, and to act as a buffer between the internal CMOS logic and the external logic level.

Applying an Inhibit command will lock the data in the transparent latch without interfereing with continuous tracking of the feedback loop. This is a new feature, since S/D and R/D converters usually lock the up-down counter while an Inhibit is applied. In the HSDC 8915 Series Monobrids, therefore, the digital angle Φ is always updated and the Inhibit can be applied for an arbitrary amount of time. The Inhibit transparent latch and the 0.2 μs delay are also parts of the Inhibit circuitry, whose detailed operation is described in the Logic Output/Input Section.

When testing or evaluating the converter, it is advisable to limit the power supply currents as follows:

+15V Supply Limit at 20 mA.
Logic Supply V_L at 2 mA + Digital Load at Logic 1.

Analog circuits inside the 8915 module are referenced to an internal DC reference level V which rides at +7V nominal with respect to the external ground (GND). V should not be connected to the external ground.

VOLTAGE FOLLOWER BUFFER INPUT

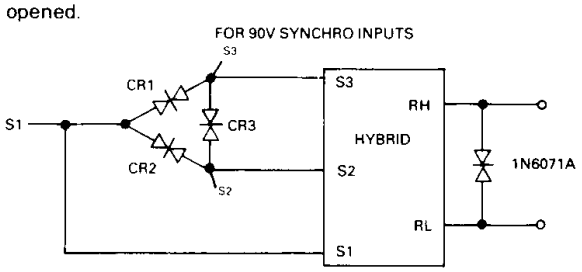
Voltage follower buffer units require a signal isolation transformer or a similar signal conditioner that provides a 1.0V rms nominal resolver type signal referenced to the internal DC level V. This input option may be preferred in applications where the signal conditioner can be integrated with other components, as in many multiplexed systems.

SOLID STATE BUFFER INPUTS

The solid state signal and reference inputs are true differential inputs with high AC and DC common mode rejection, so most applications will not require units with isolation transformers. Input impedance is maintained with power off. The recurrent AC peak + DC common mode voltage should not exceed the following values:

Input	Common Mode Maximum	Max Transient Peak Voltage
11.8V L-L	60V Peak	150V
26 V L-L	60V Peak	150V
90 V L-L	182V Peak	500V
Reference	210V Peak	1000V

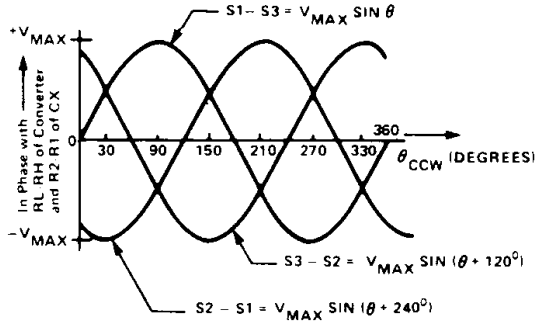
90 V line-to-line systems may have voltage transients which exceed the 500V specification listed above. These transients can destroy the thin film input resistor network in the hybrid. Therefore, 90V L-L solid state input modules may be protected by installing voltage suppressors as shown. Voltage transients are likely to occur whenever synchro or resolver voltages are switched on or off. For instance, a 1000V transient can be generated when the primary of a CX or TX driving a synchro or resolver input is opened.



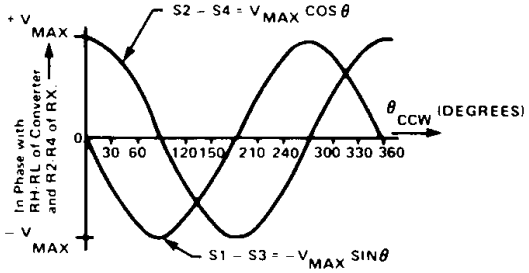
CR1, CR2 and CR3 are 1N6068A, 100V bipolar transient voltage suppressors or equivalent.

Non-standard synchro and resolver voltage levels can be accommodated with no degradation in the specifications. A unit should be selected whose voltage level 11.8V, 26V, or 90V is the next higher standard level above that of the non-standard signal. To correct the error gradient, a resistor R of the following value in ohms must be added between pins Ge and V:

$$R = \frac{1000}{A-1} \quad \text{where } A = \frac{\text{Standard Signal Voltage}}{\text{Non-Standard Signal Voltage}}$$



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

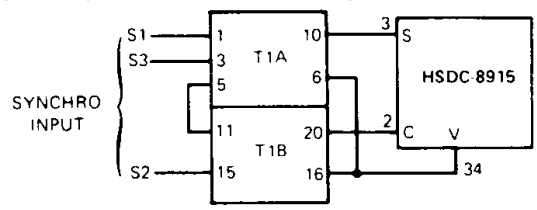
SYNCHRO AND RESOLVER SIGNALS

TRANSFORMERS

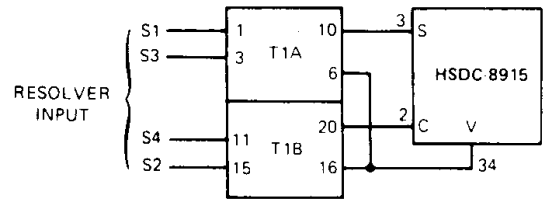
Transformer connection diagrams are shown in Figure 2. These transformers are designed for the voltage follower buffer input options HSDC 8915 and HSDC 8916. However, the reference transformers may also be used with the solid state buffer input options.

Note that the 60Hz transformers are active transformers. They have op-amp outputs and require connections to the +15V power supply as shown in Figure ?. Active devices are provided because passive transformers require considerably more volume at 60 Hz than at 400 Hz.

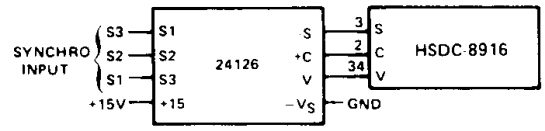
400 Hz SYNCHRO TRANSFORMER T1 21044 OR 21045



400Hz RESOLVER TRANSFORMER T1 21046 OR 21047 OR 21048



60 Hz SYNCHRO TRANSFORMER 24126



Note: Synchro inputs must be connected as shown for +sine and −cosine.

400 Hz REF TRANSFORMER 21049

60 Hz REF TRANSFORMER 24133

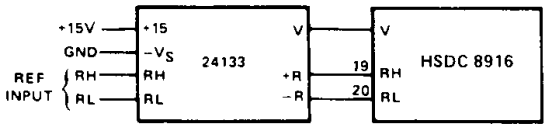
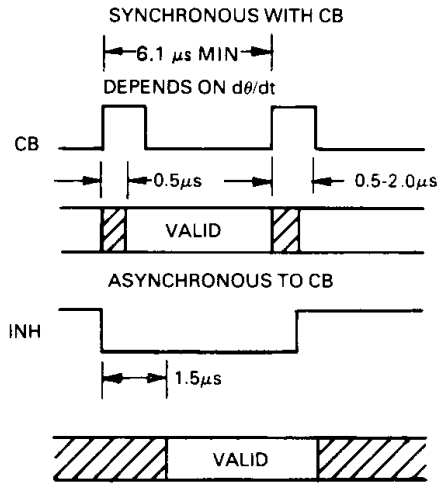


FIGURE 2 TRANSFORMER CONNECTION DIAGRAM

LOGIC OUTPUTS AND INPUTS

CAUTION: Appropriate handling procedures should be used to prevent damages to CMOS circuits.

Logic outputs consist of 14 parallel data bits and a Converter Busy (CB). All logic outputs are short-circuit proof to ground and to positive voltages as high as V_L. The CB output is a positive 0.5-2.0 μs pulse, and data changes about 0.2μs after the leading edge of the pulse because of an internal delay (see Figure 1). Data is valid 0.5μs after the leading edge of a CB. If the converter is operated with fewer than 14 bits, the unused LSB bits should be left unconnected.



TIMING DIAGRAM AT 10 RPS

The parallel digital outputs are gated to provide an 8 and a 6 line byte for microprocessor bus interfacing. When the Enables for the gates are at logic 0, the gate outputs are at normal logic 1 or 0, depending on the bit state. When the Enables are at logic 1, the gate outputs are high impedance and the microprocessor sees an essentially open line. Outputs are valid 0.5μs after an Enable is driven to logic 0. For 14 bit parallel output operation when the 3-state feature is not used, the Enable lines should be tied to logic 0.

The Inhibit (INH) logic input locks the 14 bit transparent latch so that the bits will remain stable while data is being transferred (see Figure 1). The output is stable 0.5μs after the Inhibit is driven to logic 0. A logic 0 at the T input locks the 14 bit latch, and a logic 1 allows the bits to change. The purpose of the INH transparent latch is to prevent the transmission of invalid data when there is an overlap between the CB and INH. While the counter is not being updated the CB is at logic 0 and the INH latch is transparent. When the CB goes to logic 1 the INH latch is locked. If a CB occurs after an INH has been applied, the 14 bit latch will remain locked and its data cannot change until the CB returns to logic 0. If an INH is applied during a CB pulse, the 14 bit latch will not lock until the CB pulse is over. The purpose of the 0.2μs delay is to prevent a race condition between the CB and the INH in which the up-down counter begins to change just as an INH is applied.

TIMING

Whenever an input angle change occurs, the converter changes the digital angle in 1 LSB steps and generates a converter busy pulse. The output data change is initiated by the leading edge of the CB pulse, delayed by the 0.2μs (nominal) delay. The output becomes stable in less than 0.5μs even though the CB pulse may last longer. Data transfer can be made synchronous with the leading edge of CB, delayed by 0.5μs. (See Timing Diagram.)

An Inhibit input, regardless of its duration, does not affect converter update. A simple method of interfacing to a computer, asynchronous to CB pulse, is to (a) apply the inhibit, (b) wait 1.5μs min.,(c) transfer the data and (d) release the inhibit.

ANALOG OUTPUTS

The analog outputs are V, e, and θ. V is an internal DC reference, +7 VDC nominal. The outputs e, E, and θ ride on the internal DC reference voltage V, and should be measured with respect to V. Outputs can swing ±5V when the voltage level of the +15V power supply is +15V. The output swing swing changes proportionally if the level is not at +15V.

Output e is the AC error voltage sin $(\theta - \Phi)$ near the null point. Its average amplitude at nominal input voltage for +1 LSB of error (equivalent to $(\theta - \Phi) = 0.022^\circ$) is 16 mV rms.

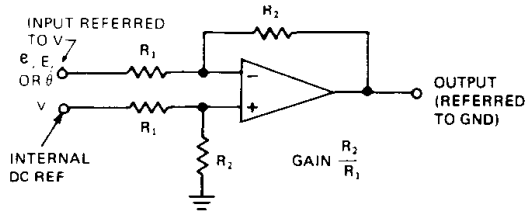
E is a DC voltage proportional to the error $(\theta - \Phi)$ near the null point, with −1 VDC output per +LSB of error.

θ is a DC voltage proportional to the angular velocity $d\theta/dt = d\Phi/dt$. A +1 VDC output corresponds to +2.1 rps for 400 Hz units, and +0.54 rps for 60 Hz units.

Maximum loading for each analog output is 1.0 mA. Outputs e, E, and θ are not required for normal operation of the converter; V is used as internal DC reference with the voltage follower buffer option.

The figure shows a difference circuit which may be used to reference the analog outputs with respect to normal ground instead of the internal DC reference ground V.

E



DIFFERENCE CIRCUIT FOR ANALOG OUTPUTS

The output e, E and θ are not closely controlled or characterized. Consult factory for further information.

USE AS A CT

The HSDC-8915 Series S/D can be used as a "Solid State CT". This is analogous to the function of a rotary control transformer except here the rotary shaft input is replaced by a digital angle. Referring to the equation below, the output is an AC voltage (e) which varies as the sine of the difference between the analog input angle and the digital angle.

$$e = \sin(\theta - \phi)\cos\omega t$$

where θ is the analog angle and ϕ is the digital angle.

Control transformers are frequently used as error signal generators in closed servo loops. They are useful when digital remote control of a position servo must be accomplished.

The procedure to enable this function is to disable the up-down counter by setting pin 30 ($\overline{S}$) to logic "0" and using the digital output lines (which are bidirectional) as digital inputs. Note that "e" rides on the internal DC reference voltage "V" (approximately 7.5V) and a differential amplifier should be used to reference this signal to real (circuit) ground as shown in diagram under analog outputs.

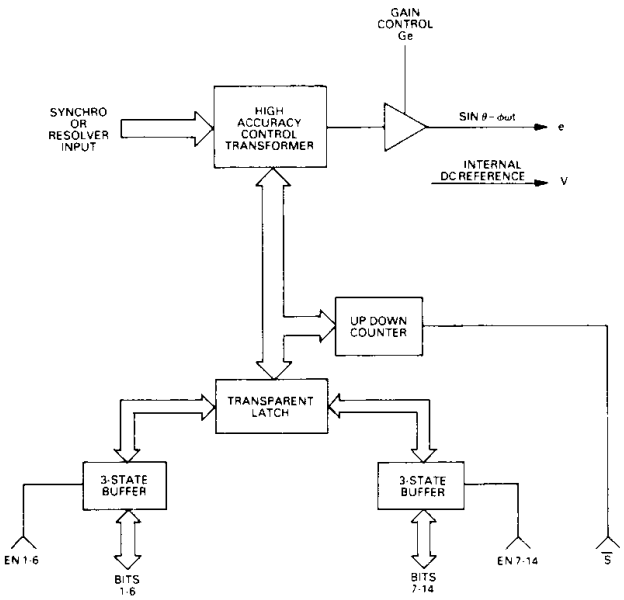


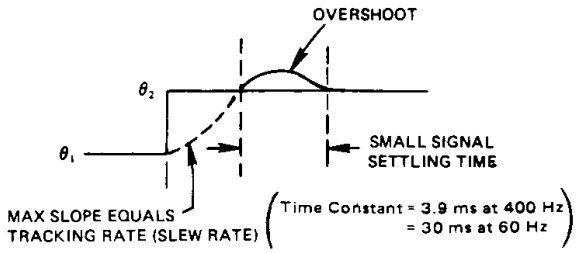
FIGURE 3. CT BLOCK DIAGRAM

The gain control function (Ge) is still operative in CT mode and the effect is the same as when used as an S/D. If you adjust the gain for a lower than nominal line-to-line signal, the error magnitude will remain the same, i.e., 16mV/LSB. If you adjust the gain for a lower signal level but come in with the "nominal" signal level, the error amplitude will be correspondingly gained-up (by the factor $V_{nominal}/V_{lower}$), however the usable error range (dynamic range) is correspondingly reduced.

DYNAMIC PERFORMANCE

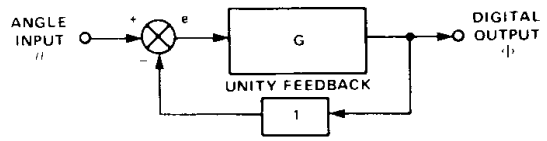
A Type II servo loop ($K_V = \infty$) and very high acceleration constants give the HSDC-8915 Series superior dynamic performance, as listed in the specifications.

If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. The response to a step input is shown below. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to final value is a function of the small signal settling time.



RESPONSE TO A STEP INPUT

The loop dynamics of the tracking converter is shown in the diagram. The closed loop transient response is nominally critically damped. All loop dynamics can be determined from the diagram and formulas listed.



For 60 Hz

$$G = \frac{33^2\left(\frac{S}{13}+1\right)}{S^2\left(\frac{S}{130}+1\right)\left(\frac{S}{550}+1\right)}$$

For 400 Hz

$$G = \frac{255^2\left(\frac{S}{100}+1\right)}{S^2\left(\frac{S}{1000}+1\right)\left(\frac{S}{2000}+1\right)}$$

CONVERTER LOOP DYNAMICS

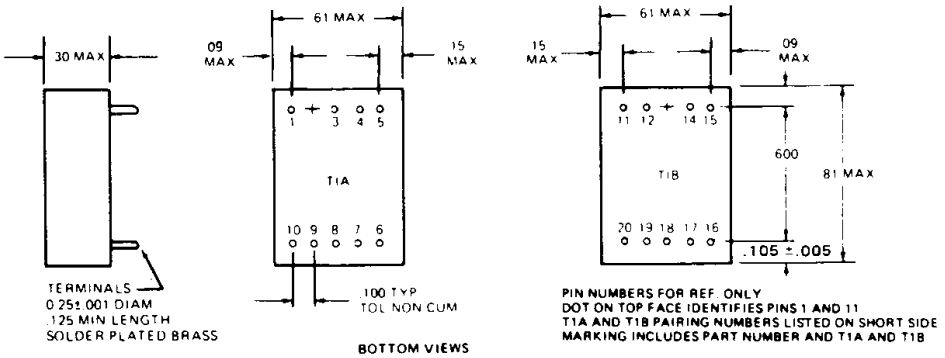
TRANSFORMER DIAGRAMS

These external transformers are for use with converter modules with voltage follower buffer inputs.

400 Hz SYNCHRO AND RESOLVER TRANSFORMER DIAGRAMS (T1A AND T1B)

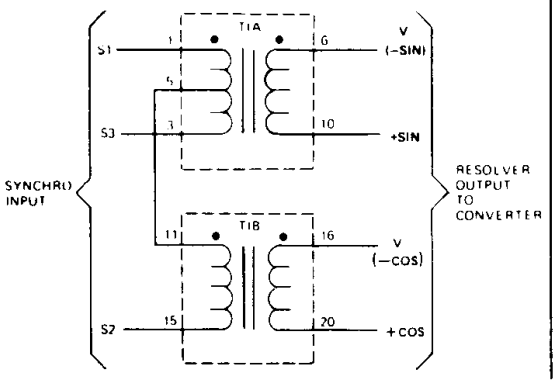
EACH TRANSFORMER CONSISTS OF TWO SECTIONS, T1A AND T1B

1. MECHANICAL OUTLINES

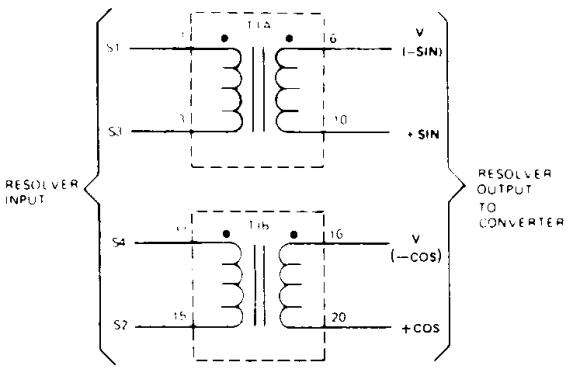


2. SCHEMATIC DIAGRAMS

A. SYNCHRO

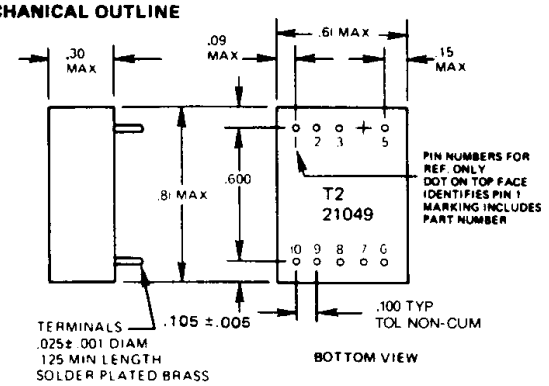


B. RESOLVER

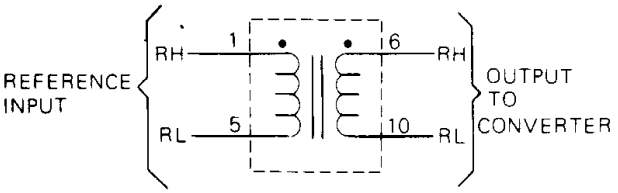


400 Hz REFERENCE TRANSFORMER DIAGRAMS (T2)

1. MECHANICAL OUTLINE

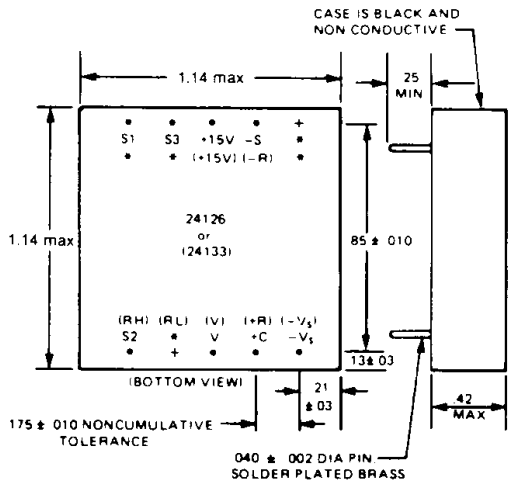


2. SCHEMATIC DIAGRAM



60 Hz SYNCHRO AND REFERENCE TRANSFORMER DIAGRAMS

The mechanical outline is the same for the synchro input transformer (24126) and the reference input transformer (24133), except for the pins. Pins for the reference transformer are shown in parenthesis ( ) below. An asterisk * indicates that the pin is omitted.



E

RELIABILITY

MTBF values are very high because the use of custom monolithics greatly decreases the number of active components, because thin film resistor networks are used, and because of careful thermal design. Summaries of MTBF calculations and susceptibility information are available on request.

ORDERING INFORMATION

1. Converters may be ordered as follows.

HSDC - 8915 –1 –a –883B

- Reliability Grade:
  - 883B = Fully compliant with MIL-STD-883
  - B = Screened to MIL-STD-883 but without QCI testing.
  - Blank = Standard DDC procedures.
- Accuracy:
  - Blank = ±4 minutes ±0.9 LSB (Standard)
  - a = ±2.6 minutes max. (High Accuracy)
- Operating Temperature Range:
  - 1 = –55°C to +125°C
  - 3 = 0°C to +70°C
- Input Type:
  - Voltage Follower Buffer (requires external signal conditioner such as an isolation transformer):
    - 8915 = 400 Hz
    - 8916 = 60 Hz
  - Solid State Synchro (direct input):
    - 8917 = 400 Hz, 11.8V L-L
    - 8918 = 400 Hz, 90V L-L
    - 8919 = 60 Hz, 90V L-L
  - Solid State Resolver (direct input):
    - 8920 = 400 Hz, 11.8V L-L
    - 8921 = 400 Hz, 26V L-L
    - 8922 = 400 Hz, 90V L-L

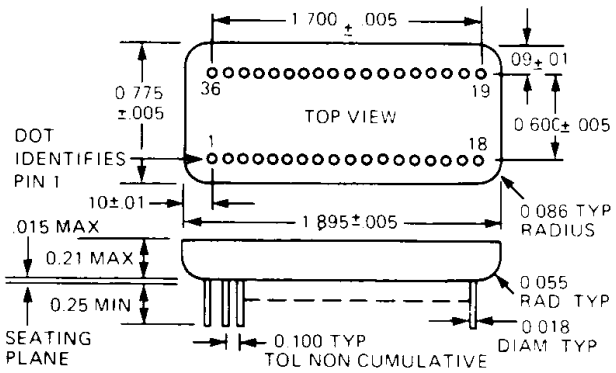
2. Reference and signal transformers for the voltage follower buffer input converters must be ordered separately as follows:

Type	Frequency	Ref. Voltage	L-L Voltage	Part Numbers	
				Ref. Xfmr.	Signal Xfmr.
Synchro	400 Hz	115V	90V	21049	21045*
Synchro	400 Hz	26V	11.8V	21049	21044*
Resolver	400 Hz	115V	90V	21049	21048*
Resolver	400 Hz	26V	26V	21049	21047*
Resolver	400 Hz	26V	11.8V	21049	21046*
Synchro†	60 Hz	115V	90V	24133-1	24126-1
				24133-3	24126-3

*The part number for each 400 Hz synchro or resolver isolation transformer includes two separate modules as shown in the outline drawings.

†60 Hz synchro transformers are available in two temperature ranges:
- 1 = –55°C to +105°C
- 3 = 0°C to +70°C

MECHANICAL OUTLINE
36 PIN DOUBLE DIP *



NOTES

1. Dimensions shown are in inches.
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
5. Package is Kovar with electroless nickel plating.
6. Case is electrically floating.

*Flatpack available, consult factory.

PIN CONNECTION TABLE

PIN	FUNCTION			PIN	FUNCTION
	Solid St. Resolver	Solid St. Synchro	Volt. Fol. Buffer		
1	S1	S1	N.C.	19	RH (Ref. High)
2	S2	S2	COS	20	RL (Ref. Low)
3	S3	S3	SIN	21	N.C.
4	S4	N.C.	N.C.	22	E (Filtered DC Error Out)
5	Bit 1 MSB			23	$\dot{\theta}$ (Analog Velocity Out)
6	Bit 2			24	CB (Converter Busy)
7	Bit 3			25	$\overline{EN\ 7\text{-}14}$ (Enable, Bits 7 to 14)
8	Bit 4			26	$\overline{EN\ 1\text{-}6}$ (Enable, Bits 1 to 6)
9	Bit 5			27	e (AC Error Out)
10	Bit 6			28	V_L (Logic Voltage Input)
11	Bit 7			29	GND
12	Bit 8			30	$\overline{S}$
13	Bit 9			31	Ge (Gain Control)
14	Bit 10			32	+15V (Power Supply In)
15	Bit 11			33	INH (Inhibit)
16	Bit 12			34	V (Internal DC Ref.)
17	Bit 13			35	BC (Buffered Cos)
18	Bit 14 LSB			36	BS (Buffered Sin)

NOTES

BS and BC pins are used in other applications.