SP5748

2.4GHz Very Low Phase Noise PLL

Datasheet

DS4875 ISSUE 2.3 November 2001

Features

- Complete 2.4 GHz Single Chip System (for faster device refer to SP5768)
- Optimised for Low Phase Noise, with Comparison Frequencies up to 4 MHz
- No RF Prescaler
- Selectable Reference Division Ratio
- Reference Frequency Output
- Selectable Charge Pump Current
- Integrated Loop Amplifier
- Two Switching Ports
- Low Power Replacement for SP5658 and SP5668
- Power Consumption 110mW with V_{CC} = 5·5V and all Ports off
- Downwards Software Compatible with SP5658
- ESD Protection 2kV min., MIL-STD-883B Method 3015 Cat.1 (Normal ESD handling procedures should be observed)

Applications

- TV, VCR and Cable Tuning Systems
- Communications Systems

Description

The SP5748 is a single chip frequency synthesiser designed for tuning systems up to 2.4 GHz and is optimized for low phase noise with comparison frequencies up to 4 MHz. It is designed to be downwards software compatible with the SP5658. The RF programmable divider contains a front end dual-modulus 416/17 functioning over the full operating range and allows for coarse tuning in the up-converter application and fine tuning in the down-converter.
Comparison frequencies are obtained either from a crystal controlled on-chip oscillator or from an external source. A buffered reference frequency output is also available to drive a second SP5748. The device also contains 2 switching ports.

Ordering Information

SP5748/KG/MP1S (Tubes)
SP5748/KG/MP1T (Tape and Reel)
(14 lead minature plastic package)
SP5748/KG/QP1S (Tubes)
SP5748/KG/QP1T (Tape and Reel)
(16 lead QSOP plastic Package)

Absolute Maximum Ratings

Supply voltage, V_{CC}	-0·3V to +7V
RF differential input voltage	2·5V
RF input DC offset	-0·3 to V_{CC} +0·3V
Port voltage	-0·3 to V_{CC} +0·3V
Charge pump DC offset	-0·3 to V_{CC} +0·3V
Varactor drive DC offset	-0·3 to V_{CC} +0·3V
Crystal DC offset	-0·3 to V_{CC} +0·3V
Buffered reference output	-0·3 to V_{CC} +0·3V
Data, clock and enable DC offset	-0·3 to V_{CC} +0·3V
Storage temperature	-55°C to +125°C
Junction temperature	+150°C
MP14 thermal resistance	
Chip to ambient, θ_{JA}	81°C/W
Chip to case, θ_{JC}	27°C/W

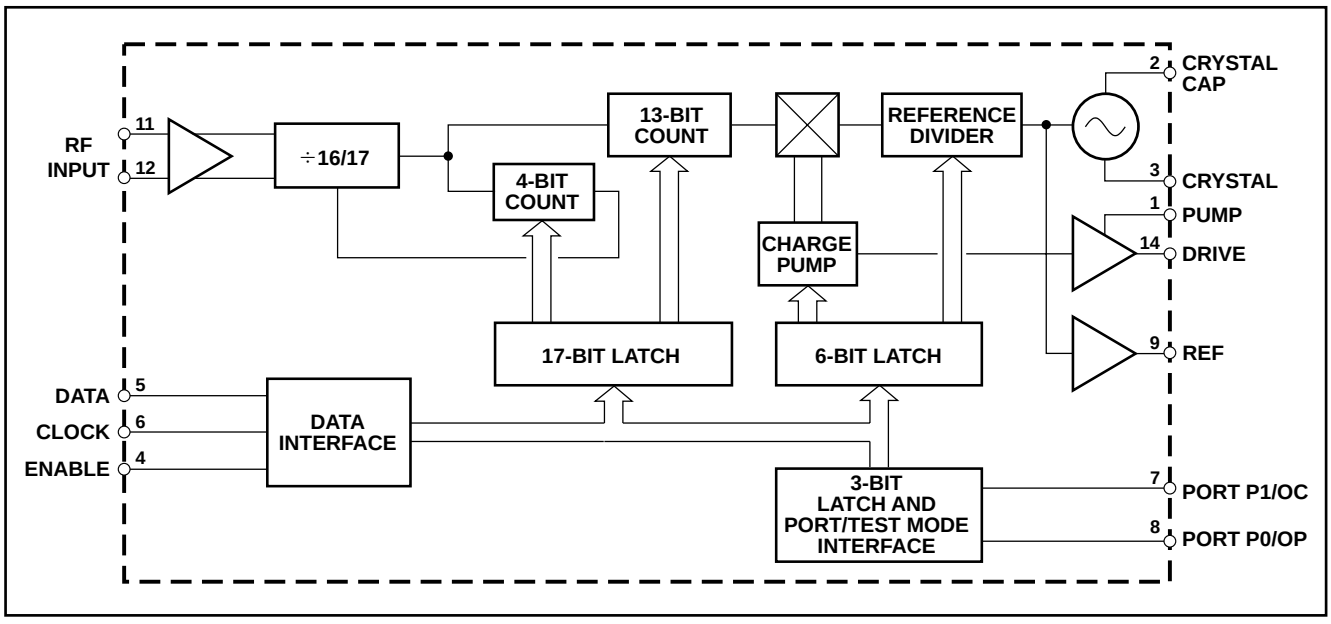


Figure 1 SP5748 Block Diagram (MP14 pinout)

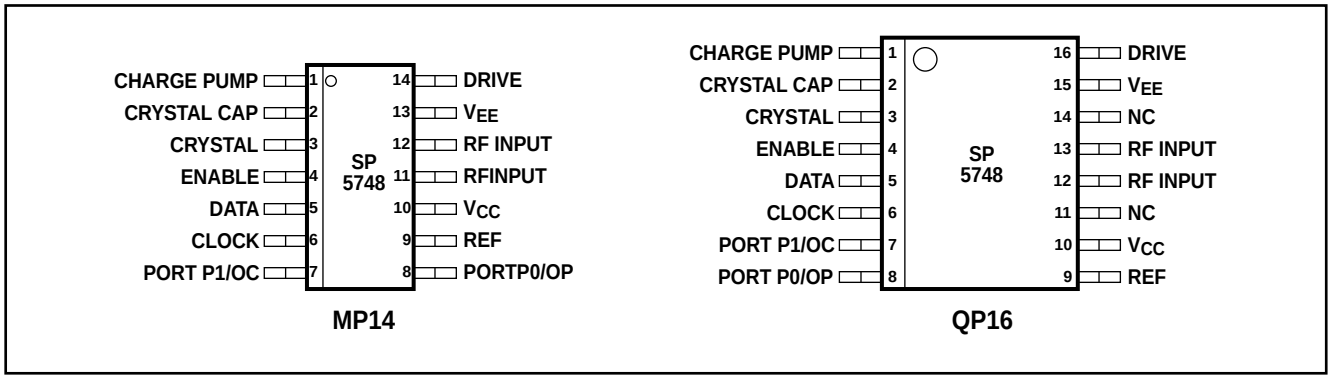


Figure 2 - Pin connections - top view

Electrical Characteristics

Test conditions (unless otherwise stated): Tamb = -40°C to +80°C, V_{CC} = 4·5V to 5·5V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Note:
Pin numbers refer to MP14 package.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	10		13	20	mA	
RF input	11,12					
Frequency range		80		-400	MHz	
Input voltage		30		300	mVrms	150MHz to 2400MHz, see Figure 6
		40		300	mVrms	80MHz to 150MHz, see Figure 6
Input impedance						See Figure 3
Data, clock and enable	5,6,4					
Input high voltage		3		V_{CC}	V	
Input low voltage		0		0·7	V	
Input current		-10		10	µA	All input conditions
Hysteresis			0·8		Vp-p	
Clock rate	6			500	kHz	
Bus timing	5,6,4					
Data set up		300			ns	
Data hold		600			ns	
Enable set up		300			ns	
Enable hold		600			ns	
Clock to enable		300			ns	
Charge pump						
Output current	1				µA	V_{PIN1} = 2V, See Table 1
Output leakage	1		±3	±10	nA	V_{PIN1} = 2V, V_{CC} = 15·0V, T_{AMB} = 25°C
Drive output current	14	0·5			mA	V_{PIN14} = 0·7V
Crystal frequency	2,3	2		20	MHz	See Figure 5 for application
External reference	2					
Input frequency		2		20	MHz	Sinewave coupled via 10nF blocking capacitor
Drive level		0·2		0·5	Vp-p	Sinewave coupled via 10nF blocking capacitor
Buffered reference output	9					AC coupled, see Note 1
Output amplitude			0·35		Vp-p	2-20MHz
Output impedance			250		Ω	

cont…

Electrical Characteristics (continued)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Comparison frequency				4	MHz	
Equivalent phase noise at phase detector		-148			dBc/Hz	At 10kHz SSB with 2MHz comparison from 4MHz crystal
RF division ratio		240		131071		
Reference division ratio		2		320		See Table 2
Output Ports P0 and P1	7,8					See Note 2
Sink current			2		mA	V_{PORT} = 0·7V
Leakage current				10	µA	$V_{PORT} = V_{CC}$

NOTES
1. Reference output disabled by connecting to V_{CC}.
2. Output ports high impedance on power-up, with data, clock and enable at logic '0'.

Functional description

The SP5748 contains all the elements necessary, with the exception of a frequency reference, loop filter and external high voltage transistor, to control a varicap tuned local oscillator, so forming a complete PLL frequency synthesised source. The device allows for operation with a high comparison frequency and is fabricated in high speed logic, which enables the generation of a loop with excellent phase noise performance, even with high comparison frequencies.

The block diagram is shown in Figure 1 and packages and pin allocations in Figure 2.

The SP5748 is controlled by a standard 3-wire bus comprising data, clock and enable inputs. The programming word contains 26 bits, two of which are used for port selection, 17 to set the programmable divider ratio, 4 bits to select the reference division ratio (bits RD and R0-R2, see Table 2), two bits to set charge pump current, bits C0 and C1 (see Table 1) and the remaining bit to access test modes (bit T0, see Table 3)). The programming data format is shown in Figure 4.

The clock input is disabled by an enable low signal, data is therefore only loaded into the internal shift registers during an enable high and is clocked into the controlling buffers by an enable high to low transition. This load is also synchronised with the programmable divider so giving smooth fine tuning.

The RF signal is fed to an internal preamplifier, which provides gain and reverse isolation from the divider signals. The output of the preamplifier is fed to the 17-bit fully programmable counter, which is of MN+A architecture. The M counter is 13 bits and the A counter 4 bits.

The output of the programmable divider is fed to the phase comparator where it is compared in both phase and frequency domain with the comparison frequency. This frequency is derived either from the on-chip crystal controlled oscillator or from an external reference source. In both cases the reference frequency is divided down to the comparison frequency by the reference divider which is programmable into1 of 16 ratios as described in Table 2.

The output of the phase detector feeds the charge pump and loop amplifier section, which when used with an external high voltage transistor and loop filter integrates the current pulses into the varactor line voltage. The charge pump current setting is described in Table 1.

A buffered crystal reference frequency suitable for driving further synthesisers is available from pin 9. If not required this output can be disabled by connecting to V_{CC}.

The programmable divider output divided by 2, $f_{PD}/2$ and comparison frequency, f_{COMP}, can be switched to ports P0 and P1 respectively by switching the device into test mode. The test modes are described in Table 3.

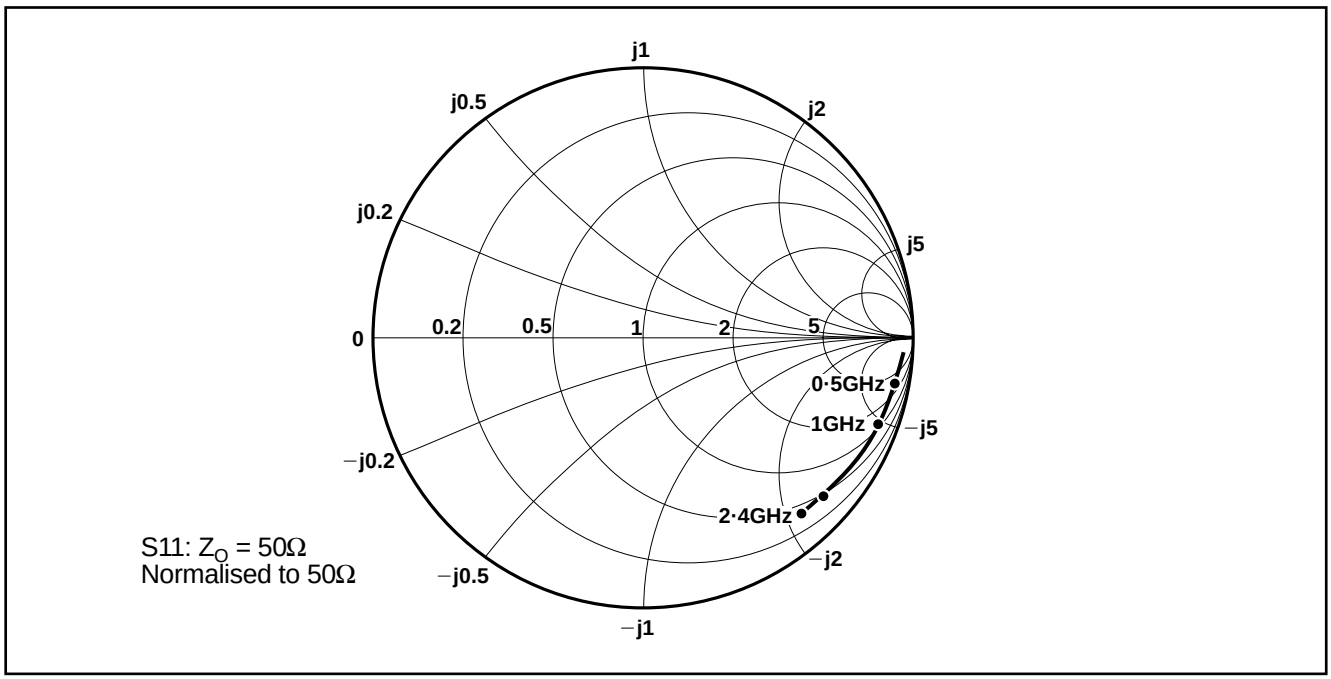
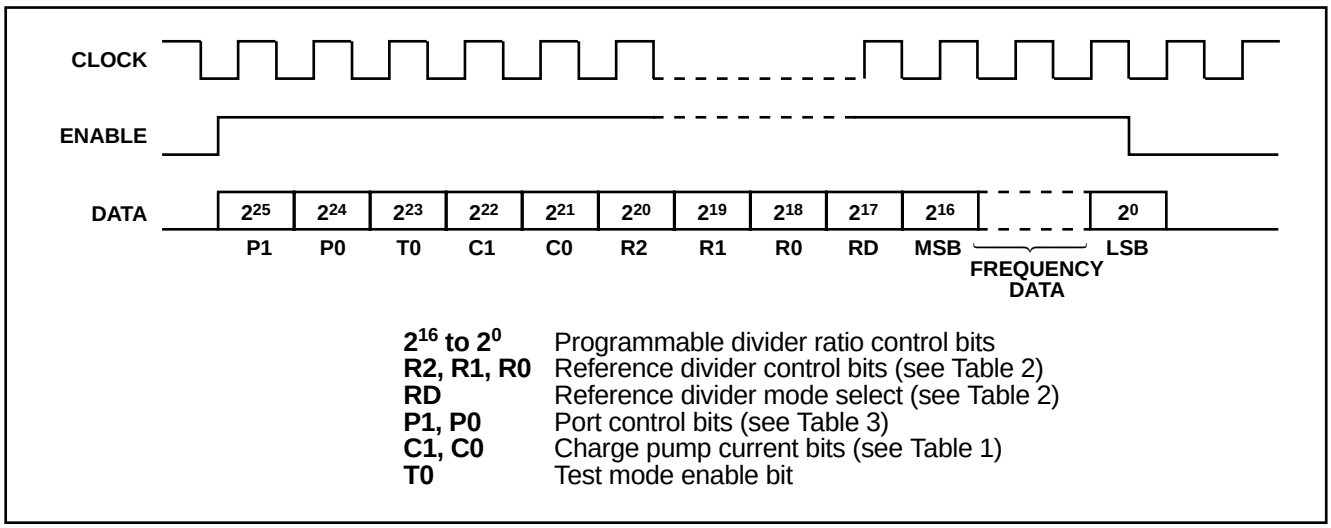


Figure 3 - RF input impedance



2^{16} to 2^{0}	Programmable divider ratio control bits
R2, R1, R0	Reference divider control bits (see Table 2)
RD	Reference divider mode select (see Table 2)
P1, P0	Port control bits (see Table 3)
C1, C0	Charge pump current bits (see Table 1)
T0	Test mode enable bit

Figure 4 - Data format

C1	C0	Charge pump current (μA)
0	0	±230
0	1	±1000
1	0	±115
1	1	±500

Table 1 - Charge pump current

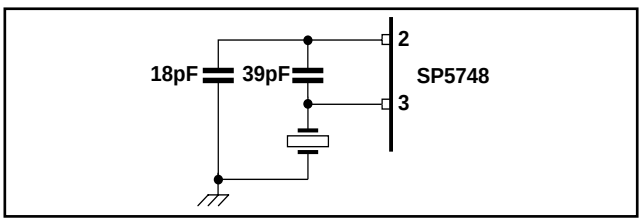


Figure 5 - Crystal oscillator application

RD	R2	R1	R0	Division ratio
0	0	0	0	2
0	0	0	1	4
0	0	1	0	8
0	0	1	1	16
0	1	0	0	32
0	1	0	1	64
0	1	1	0	128
0	1	1	1	256
1	0	0	0	3
1	0	0	1	5
1	0	1	0	10
1	0	1	1	20
1	1	0	0	40
1	1	0	1	80
1	1	1	0	160
1	1	1	1	320

Table 2 - Reference divider control

P1	P0	T0	Test mode description
X	X	0	Normal operation
0	0	1	Charge pump sink
0	1	1	Charge pump source
1	0	1	Charge pump disable
1	1	1	Port P1= f_{COMP}, P0 = $f_{PD}/2$

Table 3 - Test modes

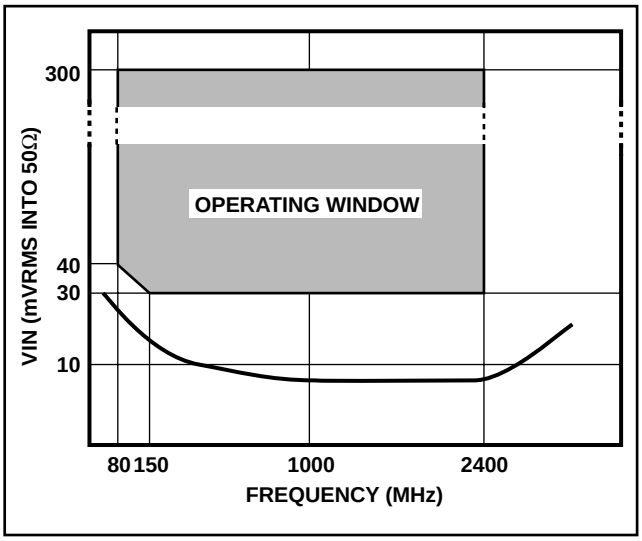


Figure 6 - Typical input sensitivity

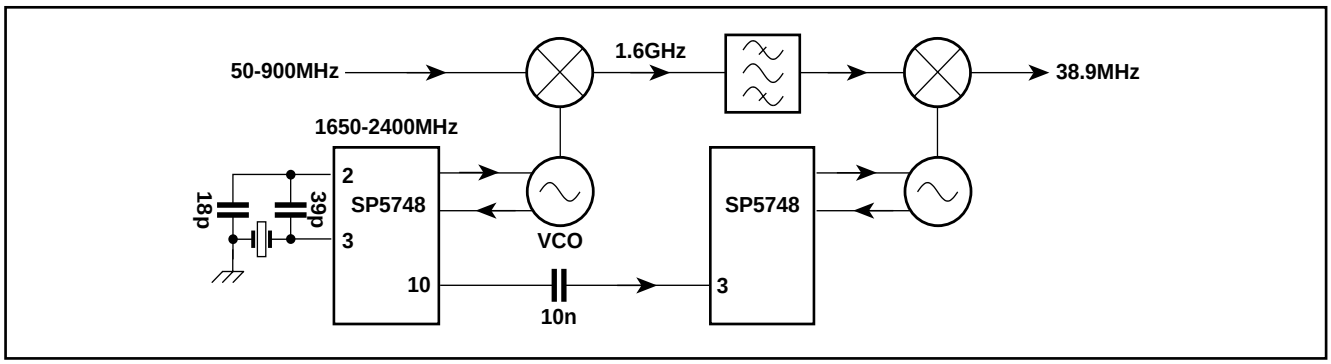


Figure 7 - Example of double conversion from VHF/UHF frequencies to TV IF

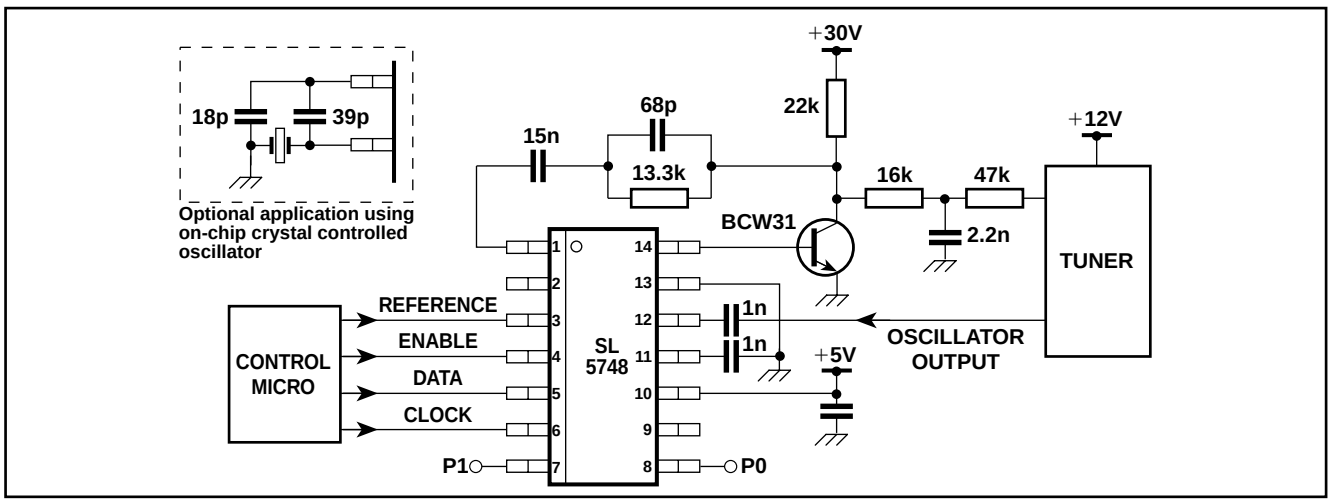


Figure 8 - Typical application of SP5748

Applications

A generic set of Application Notes AN168 for designing with synthesisers such as the SP5748 has been written, covering aspects such as loop filter design and decoupling. This application note is published on the Zarlink Semiconductor web site http:/www.zarlink.com. A generic test/demonstration board has been produced which can be used for the SP5748; the circuit diagram is shown in Figure 9, with component values in Table 4.

The board can be used for the following purposes:

- Measuring RF sensitivity performance.
- Indicating port function.
- Synthesising the voltage controlled oscillator.
- Testing of external reference.
- Measurement of phase noise performance.

Reference source
The SP5748 offers optimal LO phase noise performance when operated with a large step size. This is due to the fact that the LO phase comparator noise within the loop bandwidth is:

$$+20\log_{10}\left(\frac{\text{LO frequency}}{\text{Phase comparator frequency}}\right)$$

Assuming the phase comparator noise floor is flat irrespective of sampling frequency, this means that the best performance will be achieved when the overall LO

There are two ways of achieving a higher phase comparator sampling frequency:

(1) Reduce the division ratio between the reference source and the phase comparator
(2) use a higher reference source frequency.

Approach (2) may be preferred for best performance since it is possible that the noise floor of the reference osciliator may degrade the phase comparator performance if the reference division ratio is very small.

Loop bandwidth
The majority of applications for which the SP5748 is intended require a loop filter bandwidth of between 2kHz and10kHz.

Typically the VCO phase noise will be specified at both 1kHz and10kHz offset. It is common practice to arrange the loop filter bandwidth such that the 1kHz figure lies within the loop bandwidth. Thus the phase noise depends on the synthesiser comparator noise floor, rather than the VCO.

The 10kHz offset figure should depend on the VCO providing the loop is designed correctly, and is not underdamped.

Component	Value/type	Component	Value/type
C1	18pF	C20	1nF
C2	2·2nF	C21	1nF
C3	68pF	LED 1	HLMPK-150
C4	1nF	LED 2	HLMPK-150
C5	1nF	R1	4·7kΩ
C6	10nF	R4	4·7kΩ
C7	100nF	R6	
C8	4·7µF	R7	13·3kΩ
C9	100nF	R8	22kΩ
C10	10pF	R9	1kΩ
C11	1nF	R10	0Ω
C12	100pF	R11	16Ω
C13	100pF	R12	16Ω
C14	4·7nF	R13	16Ω
C15	100pF	R14	68Ω
C16	4·7µF	S1	SW DIP-2
C17	10nF	T1	BCW31
C18	39pF	VCO	POS_2000
C19	100pF	X1	4MHz

Table 4 - Component values for Figure 9

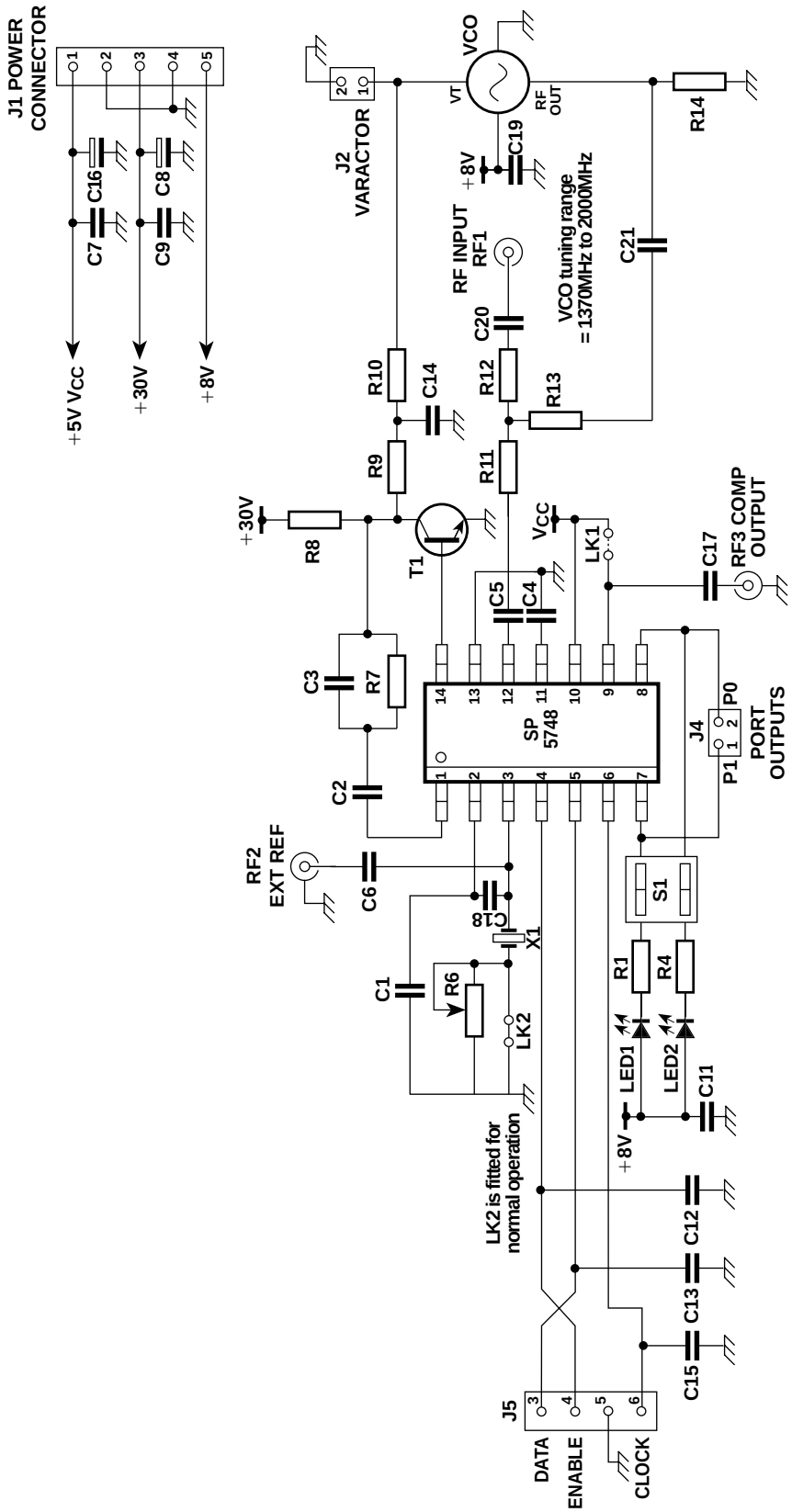
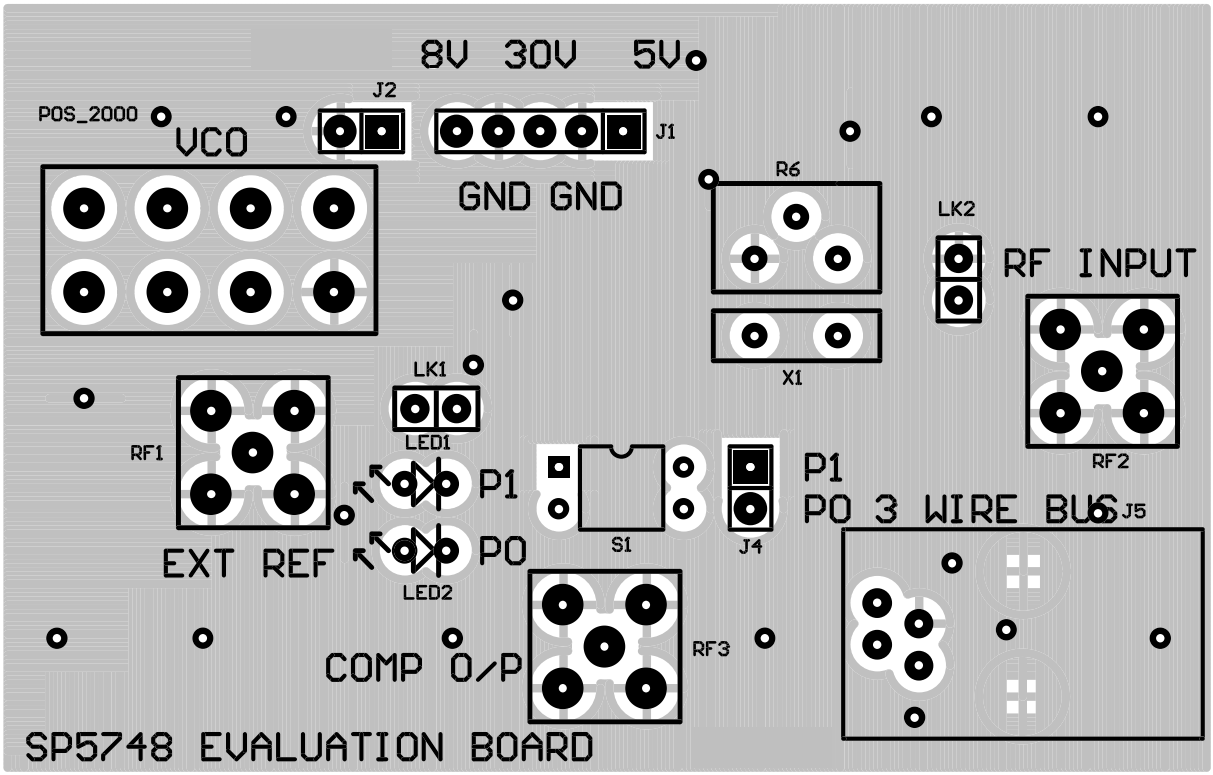
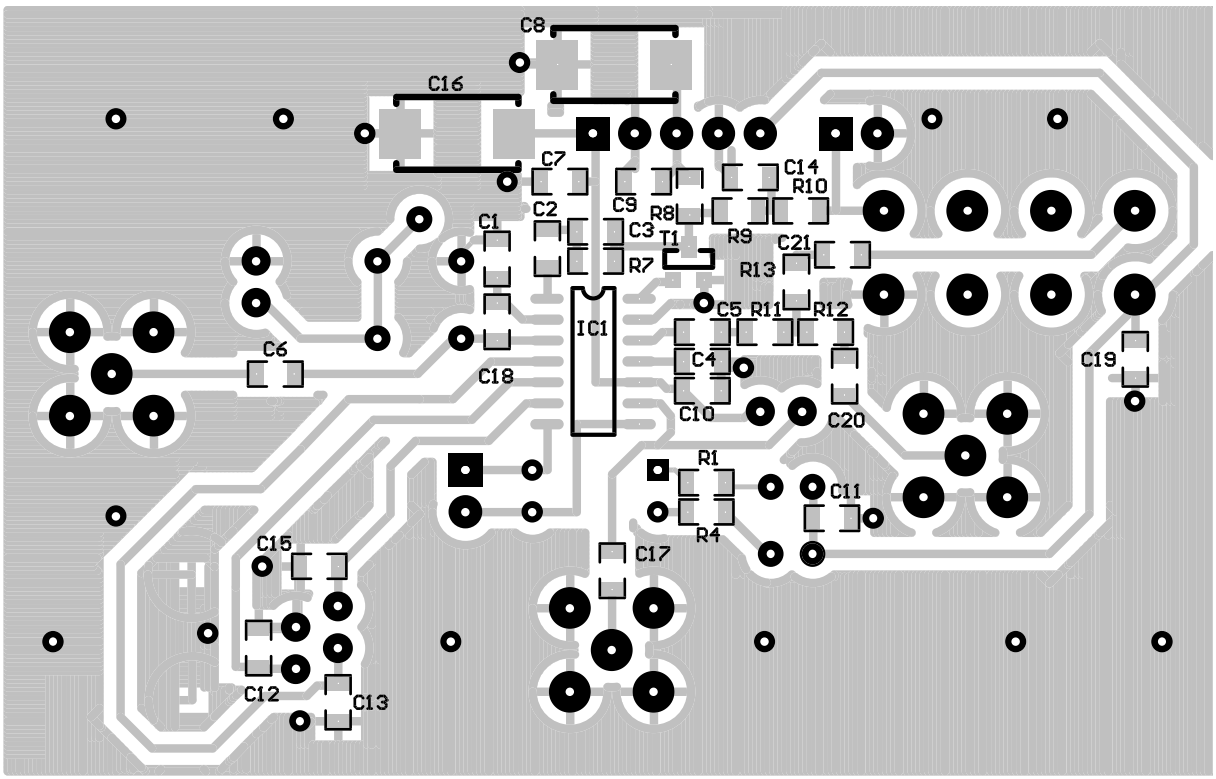


Figure 9 - SP5748 evaluation board



Top view



Bottom view

Figure 10 - SP5748 evaluation board layout

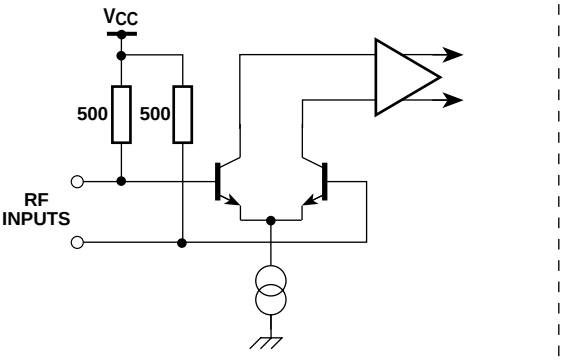


Figure 11a RF inputs

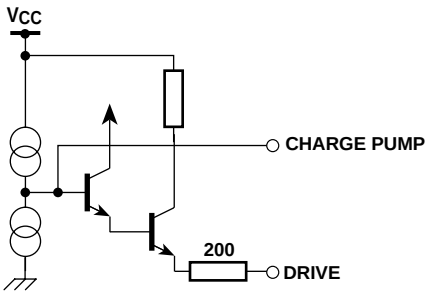


Figure 11b Loop amplifier

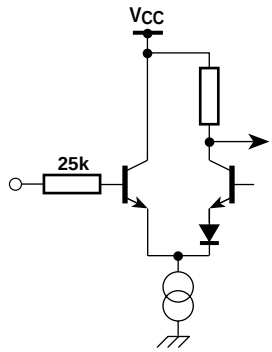


Figure 11c Enable, Data and Clock inputs

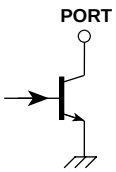


Figure 11d Output ports

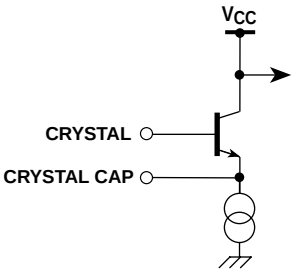


Figure 11e Reference oscillator

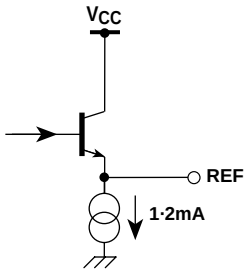
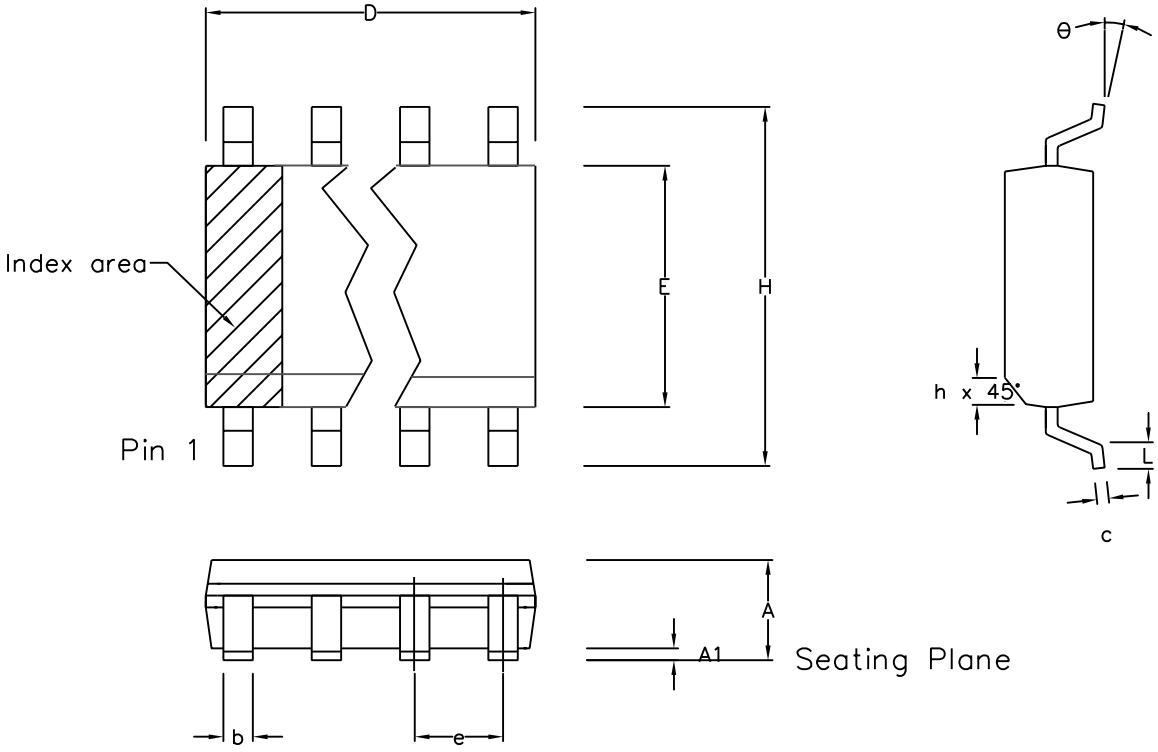


Figure 11f Reference output

Figure 11 - Input/output interface circuits



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	8.55	8.75	0.337	0.344
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	14		14	
Conforms to JEDEC MS-012AB Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	4	5
ACN	6745	201937	202596	203707	212430
DATE	7Apr95	27Feb97	12Jun97	9Dec97	25Mar02
APPRD.					

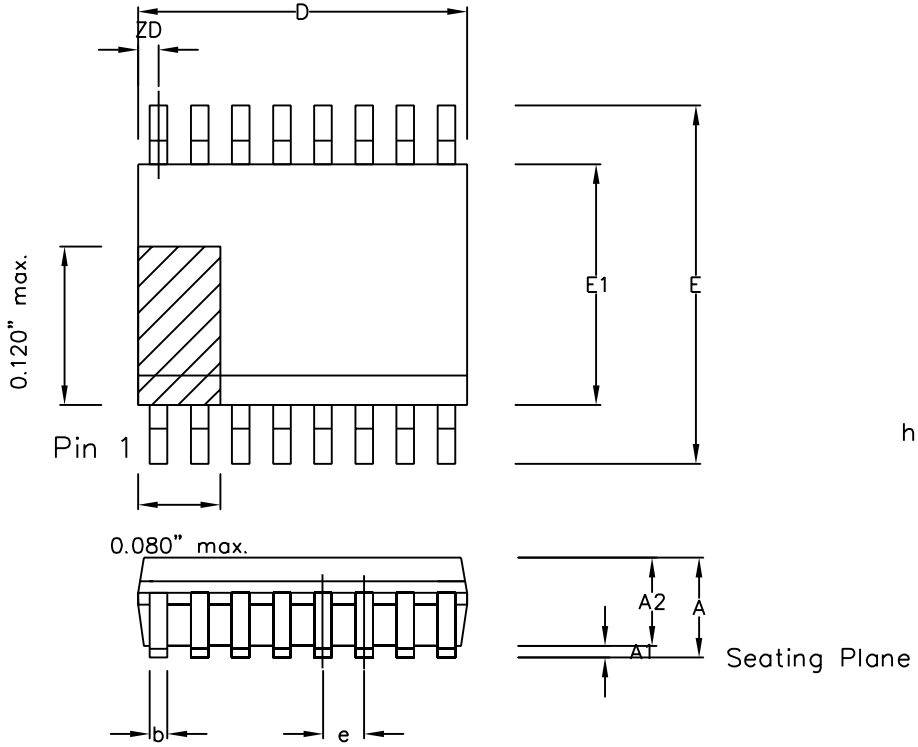
ZARLINK SEMICONDUCTOR

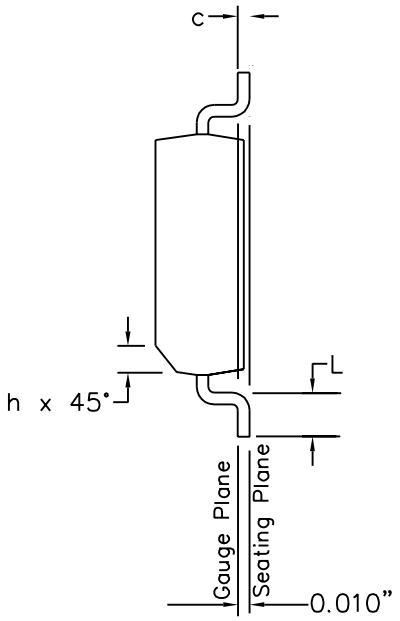
Previous package codes
MP / S

Package Code DC

Package Outline for
14 lead SOIC
(0.150" Body Width)

GPD00011





Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	—	0.059	—	1.50
D	0.189	0.197	4.80	5.00
ZD	0.009 REF.		0.23 REF.	
E	0.228	0.244	5.79	6.20
E1	0.150	0.157	3.81	3.99
L	0.016	0.050	0.41	1.27
e	0.025 BSC.		0.64 BSC.	
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.18	0.25
θ	0°	8°	0°	8°
h	0.010	0.020	0.25	0.50
	Pin features			
N	16			
Conforms to JEDEC MO-137AB Iss. A				

This drawing supersedes
418/ED/51617/001 (Swindon/Plymouth)

Notes:

1. The chamfer on the body is optional. If it is not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

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ACN	201928	207313	212474	
DATE	27Feb97	24Aug99	3Apr02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
QP / Q

Package Code DG

Package Outline for 16 lead QSOP (0.150" Body Width)

GPD00290

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www.zarlink.com