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# HN29W12814A Series

128M AND type Flash Memory  
More than 16,057-sector (67,824,768-bit) × 2

## HITACHI

ADE-203-944B (Z)

Rev. 2.0

Feb. 20, 1999

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### Description

The Hitachi HN29W12814A Series is stacked 2 chips Hitachi 64-Mbit Flash memory (HN29W6411A) that are CMOS Flash Memory with AND type memory cells. It has fully automatic programming and erase capabilities with a single 3.3 V and 5 V power supply. The functions are compatible with HN29W6411A Series and controlled by simple external commands. To fit the I/O card applications, the unit of programming and erase is as small as (512 + 16) bytes. Initial available sectors of HN29W12814A are more than 32,114 (98% of all sector address).

### Features

- On-board single power supply ( $V_{CC}$ ):
  - $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
  - $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$
- Organization
  - AND Flash Memory: (512 + 16) bytes × (More than 16,057 sectors) × 2
  - Data register: (512 + 16) bytes
- Automatic programming
  - Sector program time: 0.3 ms (typ)
  - Address, data latch function
  - Internal automatic program verify function
  - Status data polling function
- Automatic erase
  - Single sector erase time: 0.8 ms (typ)
  - Block erase time: 0.8 ms (typ)
  - System bus free
  - Internal automatic erase verify function
  - Status data polling function
- Erase mode
  - Single sector erase ((512 + 16) byte unit)
  - Block erase ((4096 + 128) byte unit)
- Fast serial read access time:
  - First access time: 5  $\mu\text{s}$  (max)

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## HN29W12814A Series

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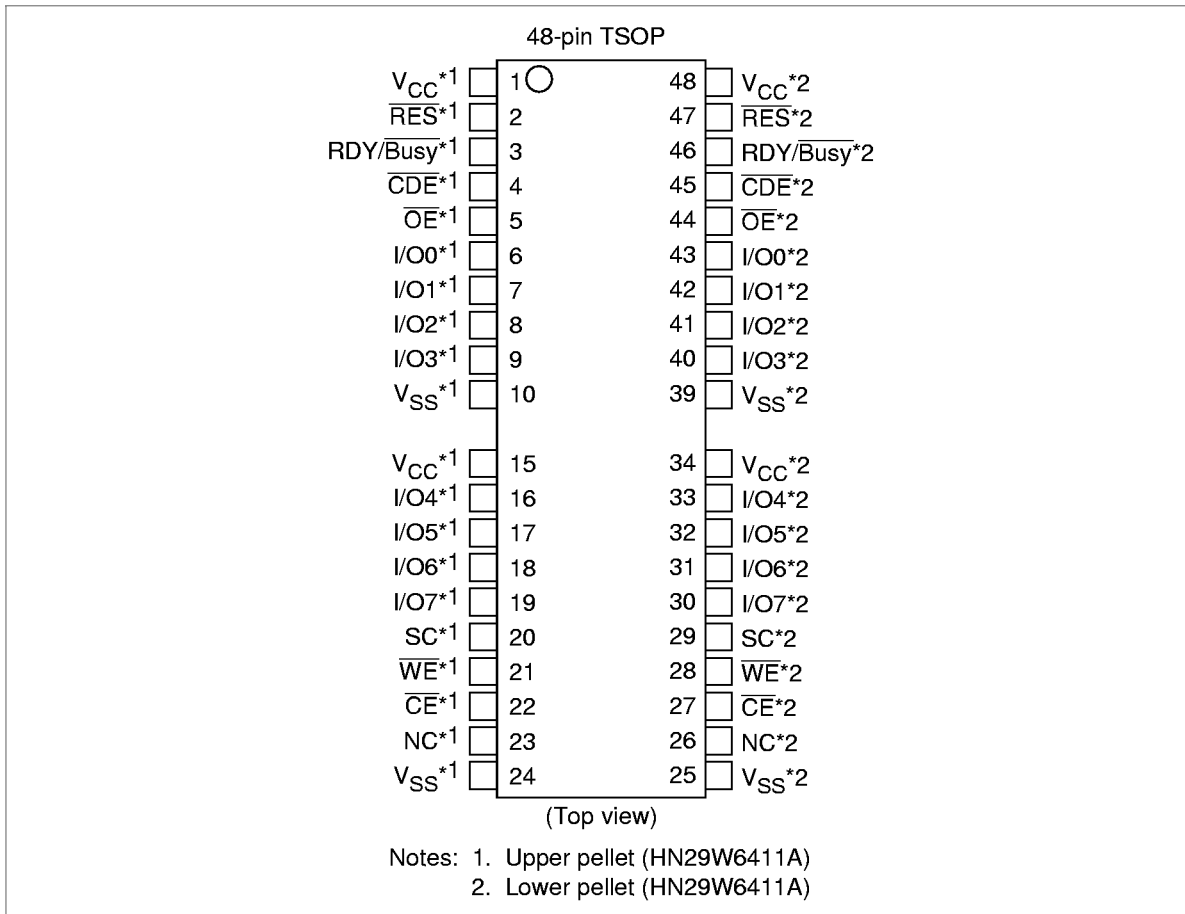
- Serial access time: 50 ns (max)
- Low power dissipation:
  - $I_{CC} = 100 \text{ mA (max)}$  (Read) ( $V_{CC} = 3.3 \text{ V}$ )
  - $I_{CC} = 140 \text{ mA (max)}$  (Read) ( $V_{CC} = 5 \text{ V}$ )
  - $I_{CC} = 100 \mu\text{A (max)}$  (Standby) ( $V_{CC} = 3.3 \text{ V}$ )
  - $I_{CC} = 200 \mu\text{A (max)}$  (Standby) ( $V_{CC} = 5 \text{ V}$ )
  - $I_{CC} = 80 \text{ mA (max)}$  (Erase/Program) ( $V_{CC} = 3.3 \text{ V}$ )
  - $I_{CC} = 120 \text{ mA (max)}$  (Erase/Program) ( $V_{CC} = 5 \text{ V}$ )
  - $I_{CC} = 10 \mu\text{A (max)}$  (Deep standby) ( $V_{CC} = 3.3 \text{ V}$ )
  - $I_{CC} = 20 \mu\text{A (max)}$  (Deep standby) ( $V_{CC} = 5 \text{ V}$ )
- Error correction (more than 1 bit error correction per each sector read) is required for data reliability.

### Ordering Information

Type No.	Available sector	Package
HN29W12814ATT-50	More than 32,114 sectors	12.7 × 19.68 mm <sup>2</sup> 0.8 mm pitch 48-pin plastic TSOP II (TTP-48/40DA)

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Pin Arrangement



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## HN29W12814A Series

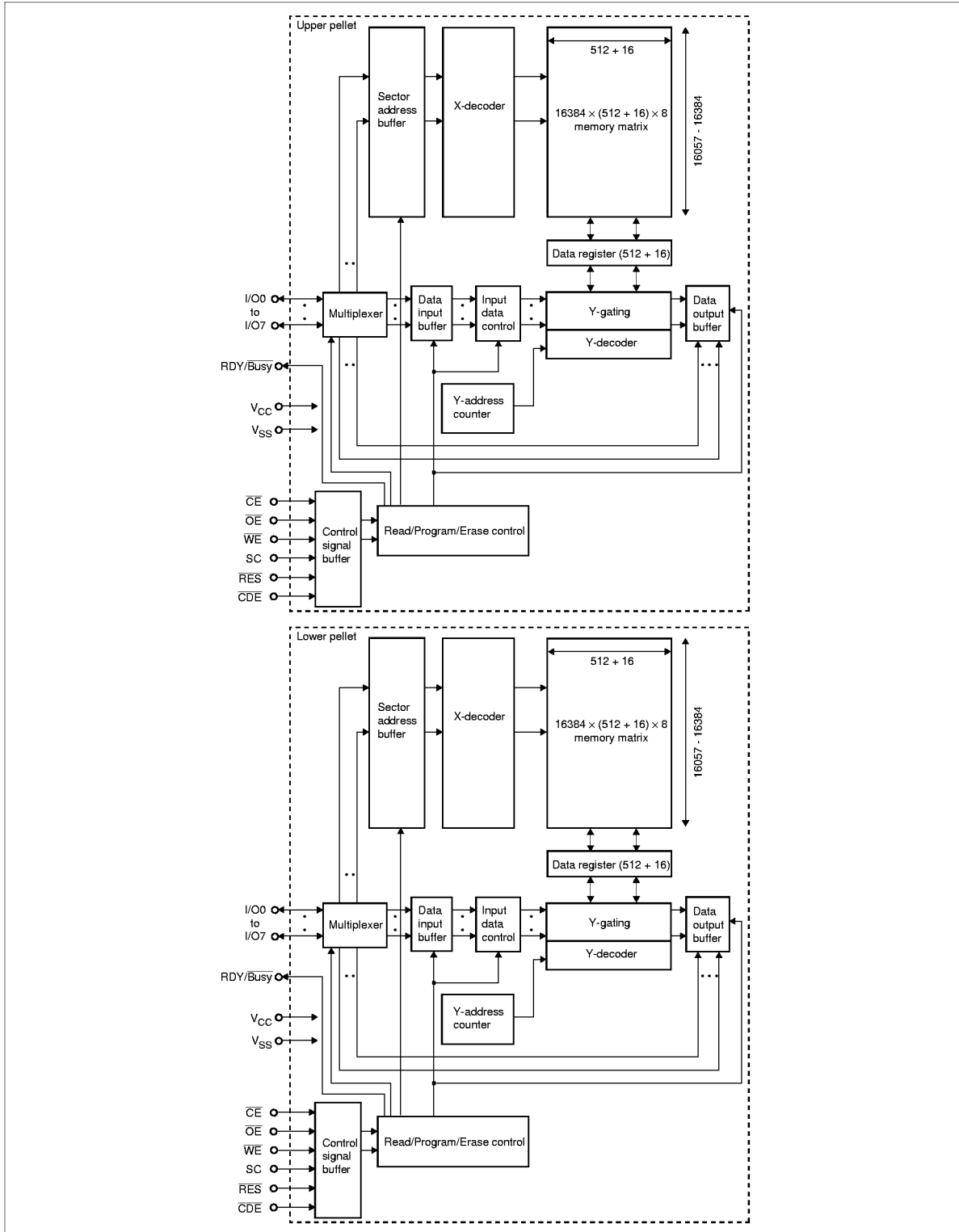
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### Pin Description

Pin name	Function
I/O0 to I/O7	Input/output
$\overline{\text{CE}}$	Chip enable
$\overline{\text{OE}}$	Output enable
$\overline{\text{WE}}$	Write enable
$\overline{\text{CDE}}$	Command data enable
$V_{\text{CC}}^{*1}$	Power supply
$V_{\text{SS}}^{*1}$	Ground
$\overline{\text{RDY/Busy}}$	Ready/Busy
$\overline{\text{RES}}$	Reset
SC	Serial clock
NC	No connection

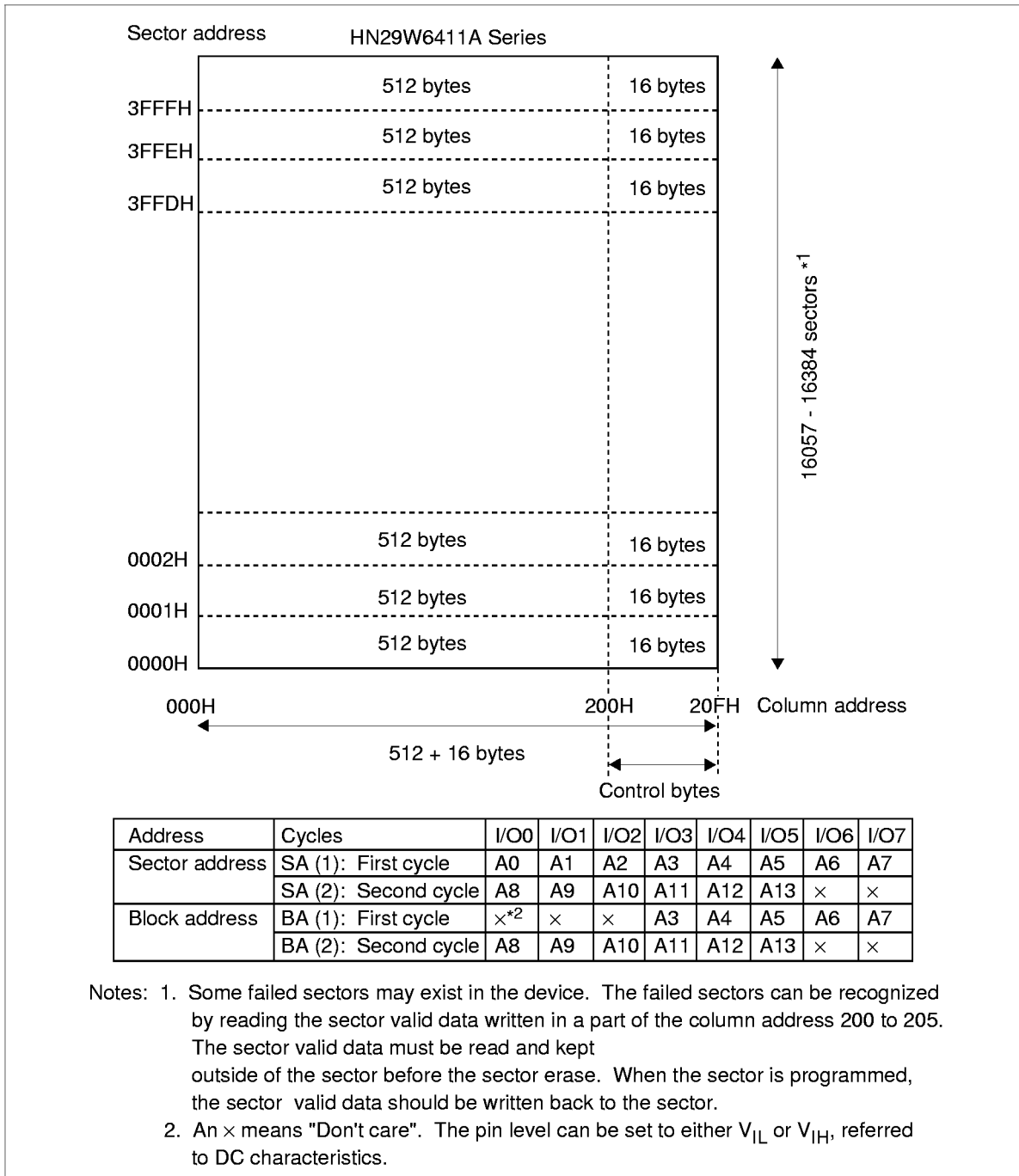
Note: 1. All  $V_{\text{CC}}$  and  $V_{\text{SS}}$  pins should be connected to a common power supply and a ground, respectively.

Block Diagram



# HN29W12814A Series

## Memory Map and Address



**Mode Selection**

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	SC	$\overline{RES}$	$\overline{CDE}$	R/ $\overline{B}$ *3	I/O0 to I/O7
Deep standby	$\times^{*4}$	$\times$	$\times$	$\times$	$V_{ILR}$	$\times$	$V_{OH}$	High-Z
Standby	$V_{IH}$	$\times$	$\times$	$\times$	$V_{IHR}$	$\times$	$V_{OH}$	High-Z
Output disable	$V_{IL}$	$V_{IH}$	$V_{IH}$	$\times$	$V_{IHR}$	$\times$	$V_{OH}$	High-Z
Status register read*1	$V_{IL}$	$V_{IL}$	$V_{IH}$	$\times$	$V_{IHR}$	$\times$	$V_{OH}$	Status register outputs
Command write*2	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IL}$	$V_{IHR}$	$V_{IL}$	$V_{OH}$	Din

- Notes: 1. Default mode after the power on is the status register read mode (refer to status transition). From I/O0 to I/O7 pins output the status, when  $\overline{CE} = V_{IL}$  and  $\overline{OE} = V_{IL}$  (conventional read operation condition).
2. Refer to the command definition. Data can be read, programmed and erased after commands are written in this mode.
3. The RDY/ $\overline{Busy}$  bus should be pulled up to  $V_{CC}$  to maintain the  $V_{OH}$  level while the RDY/ $\overline{Busy}$  pin outputs a high impedance.
4. An  $\times$  means "Don't care". The pin level can be set to either  $V_{IL}$  or  $V_{IH}$  referred to DC characteristics.

## HN29W12814A Series

### Command Definition\*1, 2

Command		Bus cycles	First bus cycle		Second bus cycle		Third bus cycle		Fourth bus cycle	
			Operation mode*3	Data in	Operation mode	Data in	Data out	Operation mode*3	Data in	Operation mode
Serial read (1)		3	Write	00H	Write	SA (1)*4	Write	SA (2)*4		
Serial read (2)		3	Write	F0H	Write	SA (1)*4	Write	SA (2)*4		
Read identifier codes		1	Write	90H	Read	ID*7, 8				
Auto erase	Single sector	4	Write	20H	Write	SA (1)*4	Write	SA (2)*4	Write	B0H*10
	Block	4	Write	7FH	Write	BA (1)*5	Write	BA (2)*5	Write	B0H*10
Auto program	Program (1)*6	4	Write	10H	Write	SA (1)*4	Write	SA (2)*4	Write	40H†10,11
	Program (2)*9	4	Write	1FH	Write	SA (1)*4	Write	SA (2)*4	Write	40H†10,11
	Program (3) (Control bytes)*6	4	Write	0FH	Write	SA (1)*4	Write	SA (2)*4	Write	40H†10,11
Erase verify		4	Write	A0H	Write	SA (1)*4	Write	SA (2)*4	Write	A0H
Reset		1	Write	FFH						
Read status register		1	Write	70H	Read	SRD*7				
Clear status register		1	Write	50H						

- Notes: 1. Commands and sector address are latched at rising edge of  $\overline{WE}$  pulses. Program data is latched at rising edge of SC pulses.
2. The chip is in the read status register mode when  $\overline{RES}$  is set to  $V_{IHR}$  first time after the power up.
3. Refer to the command read and write mode in mode selection.
4. SA (1) = Sector address (A0 to A7), SA (2) = Sector address (A8 to A13).
5. BA (1) = Block address (A3 to A7), BA (2) = Block address (A8 to A13). Address inputs of A0 to A2 are not necessary.
6. By using program (1) and (3), data can additionally be programmed maximum 15 times for each sector before erase.
7. ID = Identifier code; Manufacturer code (07H), Device code (92H). SRD = Status register data.
8. The manufacturer identifier code is output when  $\overline{CDE}$  is low and the device identifier code is output when  $\overline{CDE}$  is high.
9. Before program (2) operations, data in the programmed sector must be erased.
10. No commands can be written during auto program and erase (when the RDY/ $\overline{Busy}$  pin outputs a  $V_{OL}$ ).
11. The fourth cycle of the auto program comes after the program data input is complete.



## Mode Description

### Read

**Serial Read (1):** Memory data D0 to D527 in the sector of address SA is sequentially read. The mode turns back to the status register read mode at any time when  $\overline{CE}$  is reset. Output data is not valid after the number of the SC pulse exceeds 528.

**Serial Read (2):** Memory data D512 to D527 in the sector of address SA is sequentially read. The mode turns back to the status register read mode at any time when  $\overline{CE}$  is reset. Output data is not valid after the number of the SC pulse exceeds 16.

### Automatic Erase

**Single Sector Erase:** Memory data D0 to D527 in the sector of address SA is erased automatically by internal control circuits. After the sector erase starts, the erasure completion can be checked through the  $\overline{RDY/Busy}$  signal and status data polling. All the bits in the sector are "1" after the erase. The sector valid data stored in a part of memory data D512 to D527 must be read and kept outside of the sector before the sector erase.

**Block Erase:** Memory data D0 to D527 in the 8 sectors of block address BA is erased automatically by internal control circuits. After the block erase starts, the erasure completion can be checked through the  $\overline{RDY/Busy}$  signal and status data polling. All the bits in the sectors are "1" after the erase. The sector valid data stored in a part of memory data D512 to D527 must be read and kept outside of the sectors before the sector erase.

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## HN29W12814A Series

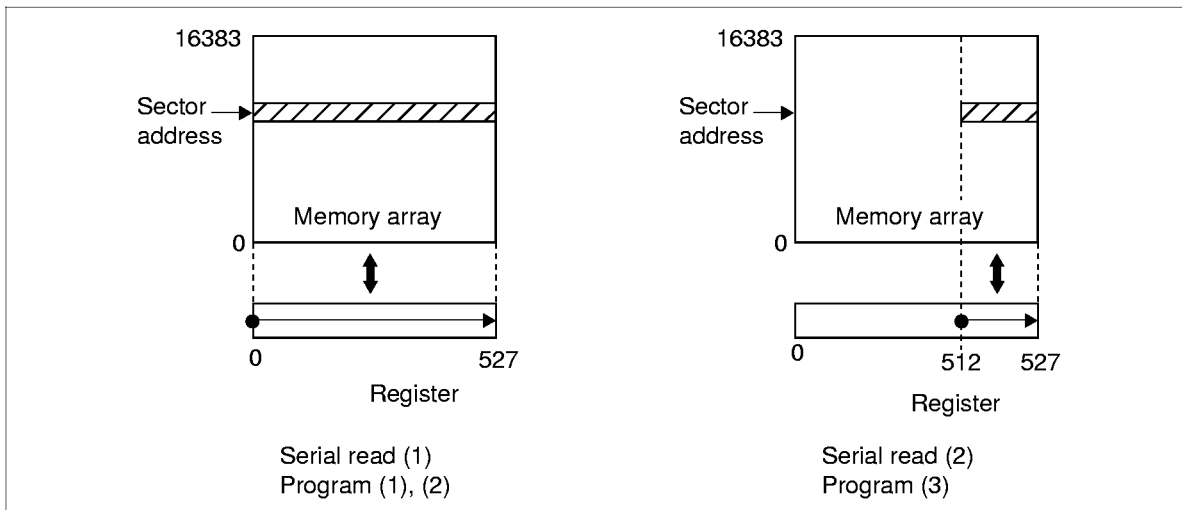
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### Automatic Program

**Program (1):** Program data PD0 to PD527 is programmed into the sector of address SA automatically by internal control circuits. By using program (1), data can additionally be programmed 15 times for each sector before the following erase. After the programming starts, the program completion can be checked through the RDY/ $\overline{\text{Busy}}$  signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed. The sector valid data should be included in the program data PD512 to PD527.

**Program (2):** Program data PD0 to PD527 is programmed into the sector of address SA automatically by internal control circuits. After the programming starts, the program completion can be checked through the RDY/ $\overline{\text{Busy}}$  signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed. The sector must be erased before programming. The sector valid data should be included in the program data PD512 to PD527.

**Program (3):** Program data PD512 to PD527 is programmed into the sector of address SA automatically by internal control circuits. By using program (3), data can additionally be programmed 15 times for each sector before the following erase. After the programming starts, the program completion can be checked through the RDY/ $\overline{\text{Busy}}$  signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed.



### Erase Verify

In the erase verify mode, I/O3 pin outputs a  $V_{OL}$  level if data in the selected sector are all "1". Otherwise, the I/O3 pin outputs a  $V_{OH}$  level.

### Status Register Read

In the status register read mode, I/O pins output the same operation status as in the status data polling defined in the function description.

**Identifier Read**

The manufacturer and device identifier code can be read in the identifier read mode. The manufacturer and device identifier code is selected with  $\overline{\text{CDE}}$  low and high, respectively.

**Function Description**

**Status Register:** The HN29W12814A outputs the operation status data as follows: I/O7 pin outputs a  $V_{OL}$  to indicate that the memory is in either erase or program operation. The level of I/O7 pin turns to a  $V_{OH}$  when the operation finishes. I/O5 and I/O4 pins output  $V_{OL}$ s to indicate that the erase and program operations complete in a finite time, respectively. If these pins output  $V_{OH}$ s, it indicates that these operations have timed out. To execute other erase and program operation, the status data must be cleared after a time out occurs. I/O3 pin outputs a  $V_{OL}$  to indicate that the result of the erase verify is a "pass". If the erase verify fails, I/O3 pin outputs a  $V_{OH}$ . From I/O0 to I/O2 and I/O6 pins are reserved for future use. The pins output  $V_{OL}$ s and should be masked out during the status data read mode. The function of the status register is summarized in the following table.

I/O	Flag definition	Definition
I/O7	Ready/ $\overline{\text{Busy}}$	$V_{OH}$ = Ready, $V_{OL}$ = Busy
I/O6	Reserved	Outputs a $V_{OL}$ and should be masked out during the status data polling mode.
I/O5	Erase check	$V_{OH}$ = Fail, $V_{OL}$ = Pass
I/O4	Program check	$V_{OH}$ = Fail, $V_{OL}$ = Pass
I/O3	Erase verify	$V_{OH}$ = Fail (not erased), $V_{OL}$ = Pass (erased)
I/O2	Reserved	Outputs a $V_{OL}$ and should be masked out during the status data polling mode.
I/O1	Reserved	
I/O0	Reserved	

**$\overline{\text{RDY/Busy}}$ :** The  $\overline{\text{RDY/Busy}}$  signal also indicates the program/erase status of the flash memory. The  $\overline{\text{RDY/Busy}}$  signal is initially at a high impedance state. It turns to a  $V_{OL}$  level after the fourth command for either an erase or programming operation is input. After the erase or programming operation finishes, the  $\overline{\text{RDY/Busy}}$  signal turns back to the high impedance state.

**$\overline{\text{WE}}$ :** Commands and address are latched at the rising edge of  $\overline{\text{WE}}$ .

**SC:** Programming data is latched at the rising edge of SC.

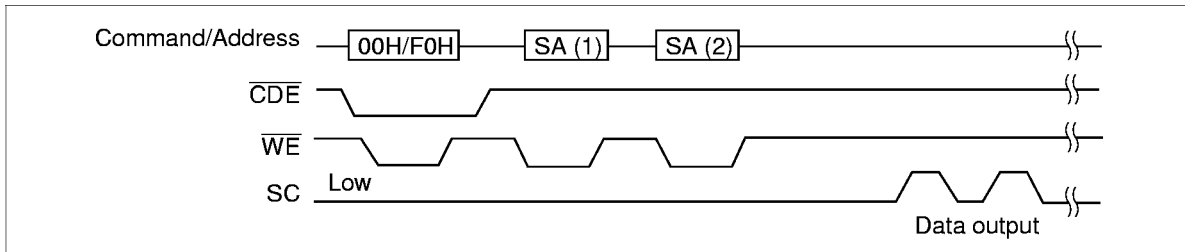
**$\overline{\text{CDE}}$ :** Commands and data are latched when  $\overline{\text{CDE}}$  is  $V_{IL}$  and Address is latched when  $\overline{\text{CDE}}$  is  $V_{IH}$ .

**$\overline{\text{RES}}$ :**  $\overline{\text{RES}}$  pin must be kept at the  $V_{ILR}$  ( $V_{SS} \pm 0.2 \text{ V}$ ) level when  $V_{CC}$  is turned on and off. In this way, data in the memory is protected against unintentional erase and programming.  $\overline{\text{RES}}$  must be kept at the  $V_{IHR}$  ( $V_{CC} \pm 0.2 \text{ V}$ ) level during any operations such as programming, erase and read.

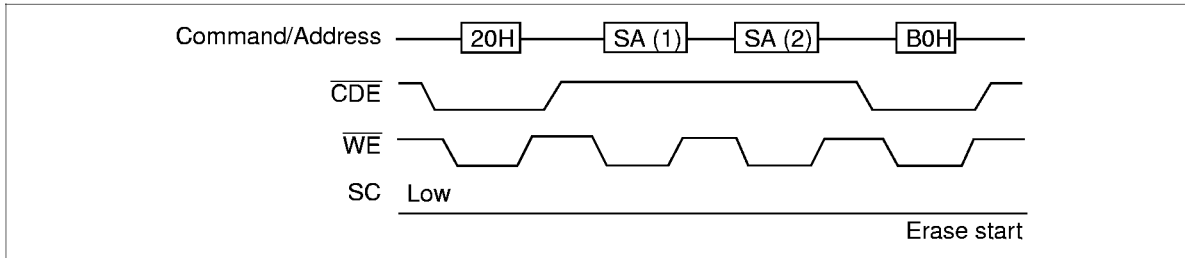
## HN29W12814A Series

### Command/Address/Data Input Sequence

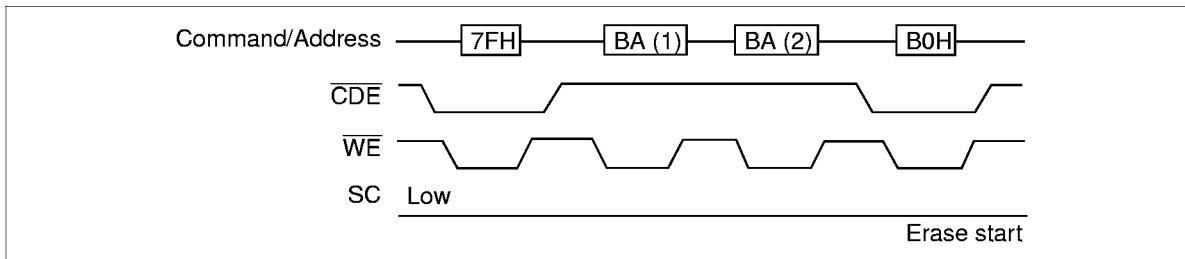
#### Serial Read (1) (2)



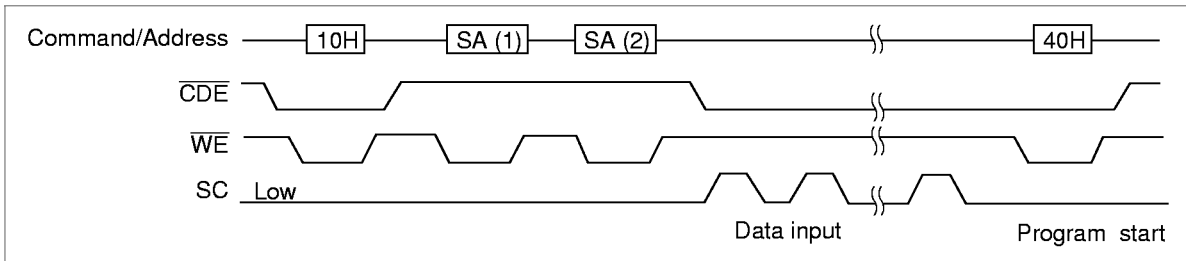
#### Single Sector Erase



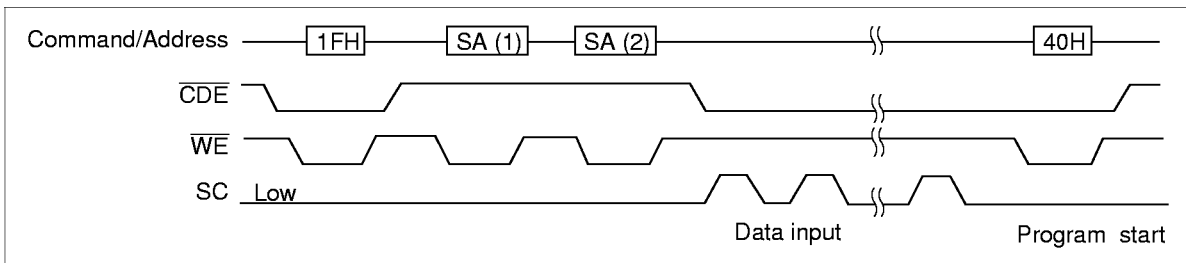
#### Block Erase



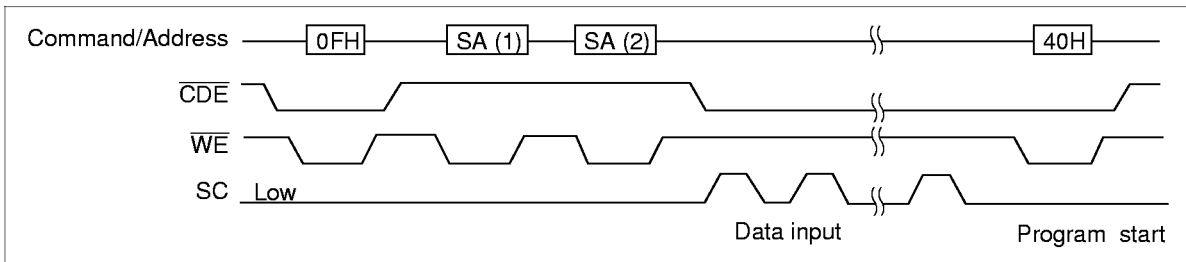
**Program (1)**



**Program (2)**



**Program (3)**

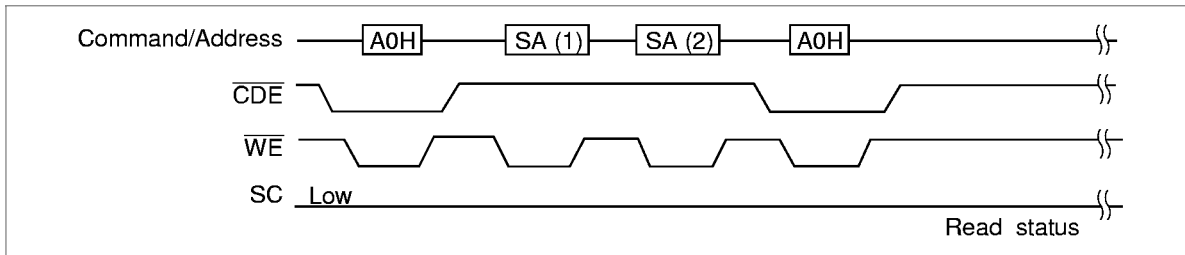


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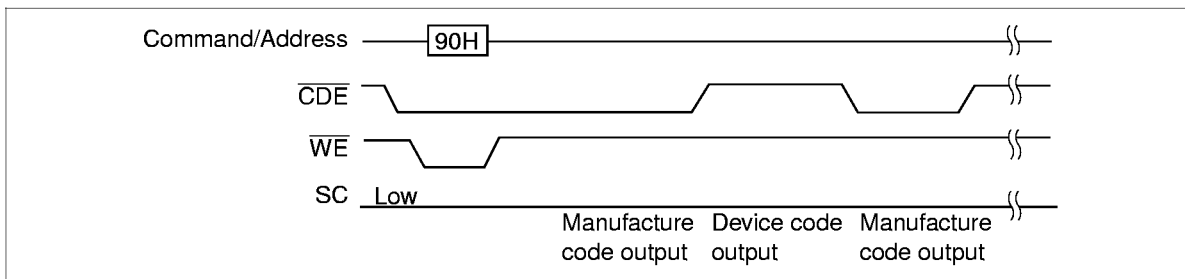
## HN29W12814A Series

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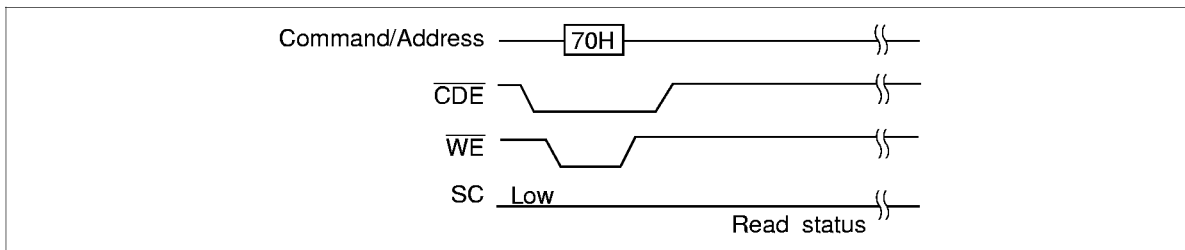
### Erase Verify Mode



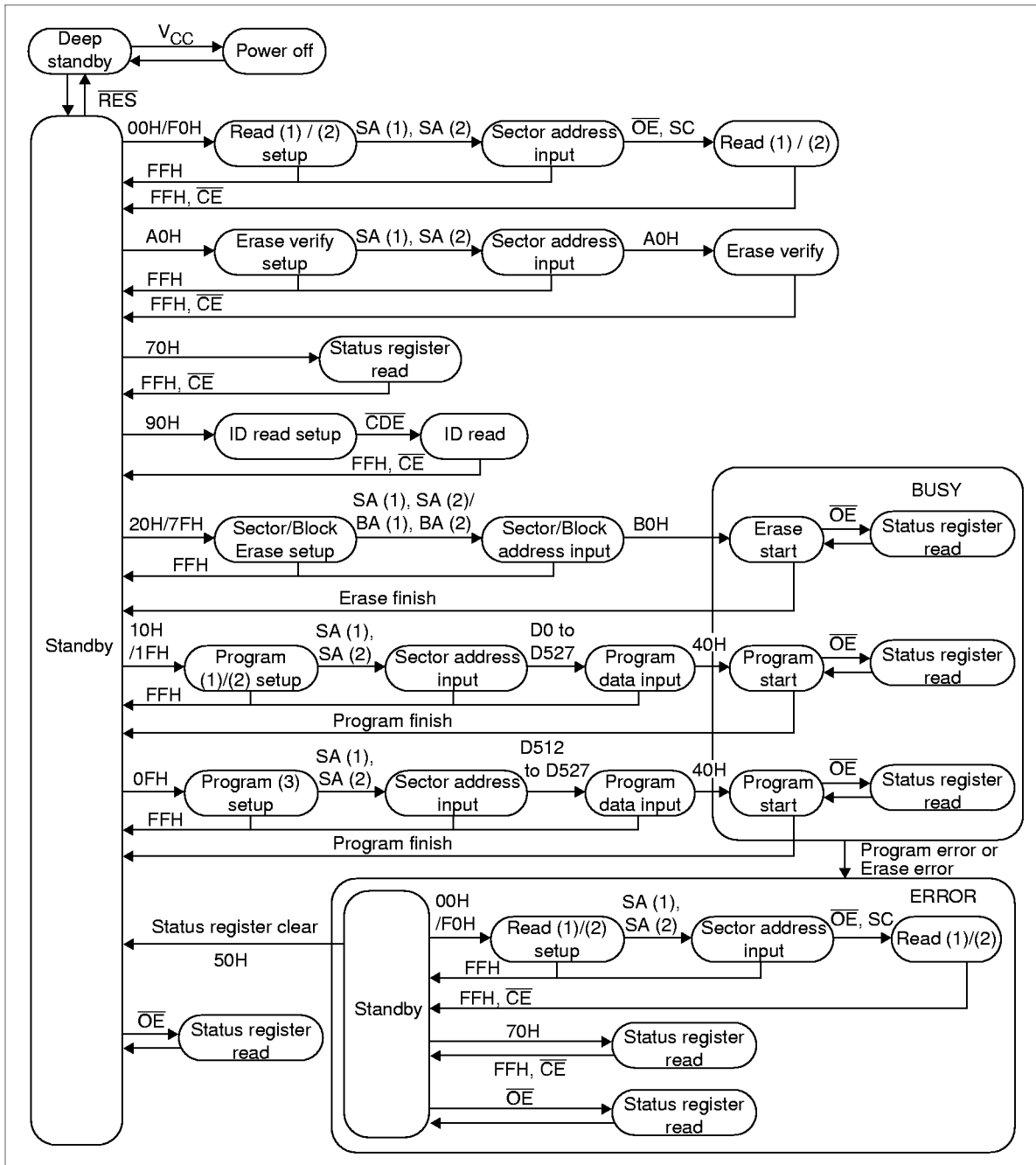
### ID Read Mode



### Status Register Read Mode



Status Transition



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## HN29W12814A Series

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### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
V <sub>CC</sub> voltage	V <sub>CC</sub>	-0.6 to +7	V	1
All input and output voltages	V <sub>in</sub> , V <sub>out</sub>	-0.6 to +7	V	1, 2
Operating temperature range	T <sub>opr</sub>	0 to +70	°C	
Storage temperature range	T <sub>stg</sub>	-65 to +125	°C	3
Storage temperature under bias	T <sub>bias</sub>	-10 to +80	°C	

Notes: 1. Relative to V<sub>SS</sub>.  
2. V<sub>in</sub>, V<sub>out</sub> = -2.0 V for pulse width ≤ 20 ns.  
3. Device storage temperature range before programming.

### Capacitance (T<sub>a</sub> = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	C <sub>in</sub>	—	—	6	pF	V <sub>in</sub> = 0 V
Output capacitance	C <sub>out</sub>	—	—	12	pF	V <sub>out</sub> = 0 V



## HN29W12814A Series

### DC Characteristics-1 ( $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ , $T_a = 0 \text{ to } +70^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	$I_{LI}$	—	—	2	$\mu\text{A}$	$V_{in} = V_{SS} \text{ to } V_{CC}$
Output leakage current	$I_{LO}$	—	—	2	$\mu\text{A}$	$V_{out} = V_{SS} \text{ to } V_{CC}$
Standby $V_{CC}$ current	$I_{SB1}$	—	0.6	2	mA	$\overline{CE} = V_{IH}$
	$I_{SB2}$	—	60	100	$\mu\text{A}$	$\overline{CE} = V_{CC} \pm 0.2 \text{ V}$ , $\overline{RES} = V_{CC} \pm 0.2 \text{ V}$
Deep standby $V_{CC}$ current	$I_{SB3}$	—	2	10	$\mu\text{A}$	$\overline{RES} = V_{SS} \pm 0.2 \text{ V}$
Operating $V_{CC}$ current	$I_{CC1}$	—	—	50	mA	$I_{out} = 0 \text{ mA}$ , $f = 0.2 \text{ MHz}$
	$I_{CC2}$	—	60	100	mA	$I_{out} = 0 \text{ mA}$ , $f = 20 \text{ MHz}$
Operating $V_{CC}$ current (Program)	$I_{CC3}$	—	—	80	mA	In programming
Operating $V_{CC}$ current (Erase)	$I_{CC4}$	—	—	80	mA	In erase
Input voltage	$V_{IL}$	$-0.3^{*1,2}$	—	0.8	V	
	$V_{IH}$	2.0	—	$V_{CC} + 0.3^{*3}$	V	
Input voltage ( $\overline{RES}$ pin)	$V_{ILR}$	-0.2	—	0.2	V	
	$V_{IHR}$	$V_{CC} - 0.2$	—	$V_{CC} + 0.2$	V	
Output voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2 \text{ mA}$
	$V_{OH}$	2.4	—	—	V	$I_{OH} = -2 \text{ mA}$

- Notes: 1.  $V_{IL}$  min = -1.0 V for pulse width  $\leq 50$  ns in the read operation.  $V_{IL}$  min = -2.0 V for pulse width  $\leq 20$  ns in the read operation.
2.  $V_{IL}$  min = -0.6 V for pulse width  $\leq 20$  ns in the erase/data programming operation.
3.  $V_{IH}$  max =  $V_{CC} + 1.5 \text{ V}$  for pulse width  $\leq 20$  ns. If  $V_{IH}$  is over the specified maximum value, the operations are not guaranteed.

## HN29W12814A Series

### DC Characteristics-2 ( $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ , $T_a = 0\text{ to }+70^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	$I_{LI}$	—	—	2	$\mu\text{A}$	$V_{in} = V_{SS}\text{ to }V_{CC}$
Output leakage current	$I_{LO}$	—	—	2	$\mu\text{A}$	$V_{out} = V_{SS}\text{ to }V_{CC}$
Standby $V_{CC}$ current	$I_{SB2}$	—	—	200	$\mu\text{A}$	$\overline{CE} = V_{CC} \pm 0.2\text{ V}$ , $\overline{RES} = V_{CC} \pm 0.2\text{ V}$
Deep standby $V_{CC}$ current	$I_{SB3}$	—	—	20	$\mu\text{A}$	$\overline{RES} = V_{SS} \pm 0.2\text{ V}$
Operating $V_{CC}$ current	$I_{CC1}$	—	—	100	$\text{mA}$	$I_{out} = 0\text{ mA}$ , $f = 0.2\text{ MHz}$
	$I_{CC2}$	—	—	140	$\text{mA}$	$I_{out} = 0\text{ mA}$ , $f = 20\text{ MHz}$
Operating $V_{CC}$ current (Program)	$I_{CC3}$	—	—	120	$\text{mA}$	In programming
Operating $V_{CC}$ current (Erase)	$I_{CC4}$	—	—	120	$\text{mA}$	In erase
Input voltage	$V_{IL}$	$-0.3^{*1,2}$	—	0.2	V	
	$V_{IH}$	$V_{CC} - 0.2$	—	$V_{CC} + 0.3^{*3}$	V	
Input voltage ( $\overline{RES}$ pin)	$V_{ILR}$	-0.2	—	0.2	V	
	$V_{IHR}$	$V_{CC} - 0.2$	—	$V_{CC} + 0.2$	V	
Output voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2\text{ mA}$
	$V_{OH}$	2.4	—	—	V	$I_{OH} = -2\text{ mA}$

- Notes: 1.  $V_{IL}$  min =  $-1.0\text{ V}$  for pulse width  $\leq 50\text{ ns}$  in the read operation.  $V_{IL}$  min =  $-2.0\text{ V}$  for pulse width  $\leq 20\text{ ns}$  in the read operation.
2.  $V_{IL}$  min =  $-0.6\text{ V}$  for pulse width  $\leq 20\text{ ns}$  in the erase/data programming operation.
3.  $V_{IH}$  max =  $V_{CC} + 1.5\text{ V}$  for pulse width  $\leq 20\text{ ns}$ . If  $V_{IH}$  is over the specified maximum value, the operations are not guaranteed.

**AC Characteristics** ( $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V} / V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ ,  $T_a = 0$  to  $+70^\circ\text{C}$ )**Test Conditions-1** ( $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ )

- Input pulse levels: 0.4 V/2.4 V
- Input rise and fall time:  $\leq 10 \text{ ns}$
- Output load: 1 TTL gate +50 pF (Including scope and jig.)
- Reference levels for measuring timing: 0.8 V, 1.8 V

**Test Conditions-2** ( $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ )

- Input pulse levels: 0.2 V/ $V_{CC} - 0.2 \text{ V}$
- Input rise and fall time:  $\leq 10 \text{ ns}$
- Output load: 1 TTL gate +50 pF (Including scope and jig.)
- Reference levels for measuring timing: 0.8 V, 1.8 V

## HN29W12814A Series

### Power on and off, Serial Read Mode (1) and (2)

Parameter	Symbol	Min	Max	Unit	Test conditions	Note
Write cycle time	$t_{CWC}$	120	—	ns		
Serial clock cycle time	$t_{SCC}$	50	—	ns		
$\overline{CE}$ setup time	$t_{CES}$	0	—	ns		
$\overline{CE}$ hold time	$t_{CEH}$	0	—	ns		
Write pulse time	$t_{WP}$	60	—	ns	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$	
Write pulse high time	$t_{WPH}$	40	—	ns		
Address setup time	$t_{AS}$	50	—	ns		
Address hold time	$t_{AH}$	10	—	ns		
Data setup time	$t_{DS}$	50	—	ns		
Data hold time	$t_{DH}$	10	—	ns		
SC to output delay	$t_{SAC}$	—	50	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$	
$\overline{OE}$ setup time for SC	$t_{OES}$	0	—	ns		
$\overline{OE}$ low to output low-Z	$t_{OEL}$	0	—	ns		
$\overline{OE}$ setup time before read	$t_{OEPS}$	40	—	ns		
$\overline{OE}$ setup time before command write	$t_{OEPS}$	0	—	ns		
SC to output hold	$t_{SH}$	15	—	ns	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$	
$\overline{OE}$ high to output float	$t_{DF}$	—	40	ns	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$	1
$\overline{WE}$ to SC delay time	$t_{WSD}$	5	—	$\mu s$		
$\overline{RES}$ to $\overline{CE}$ setup time	$t_{RP}$	1	—	ms		
SC to $\overline{CE}$ , $\overline{OE}$ hold time	$t_{SCH}$	50	—	ns		
SC pulse width	$t_{SP}$	20	—	ns		
SC pulse low time	$t_{SPL}$	20	—	ns		
SC setup time for $\overline{CE}$	$t_{SCS}$	0	—	ns		
$\overline{CDE}$ setup time for $\overline{WE}$	$t_{CDS}$	0	—	ns		
$\overline{CDE}$ hold time for $\overline{WE}$	$t_{CDH}$	20	—	ns		
$V_{CC}$ to $\overline{RES}$ setup time	$t_{RES}$	1	—	$\mu s$	$\overline{CE} = V_{IH}$	
$\overline{CE}$ setup time for $\overline{RES}$	$t_{CESR}$	1	—	$\mu s$		
RDY/ $\overline{Busy}$ undefined for $V_{CC}$ off	$t_{DFP}$	0	—	ns		
$\overline{RES}$ high to device ready	$t_{BSY}$	—	1	ms		
$\overline{CE}$ pulse high time	$t_{CPH}$	200	—	ns		
$\overline{CE}$ , $\overline{WE}$ setup time for $\overline{RES}$	$t_{CWRS}$	0	—	ns		
$\overline{RES}$ to $\overline{CE}$ , $\overline{WE}$ hold time	$t_{CWRH}$	0	—	ns		

Note: 1.  $t_{DF}$  is a time after which the I/O pins become open.

## HN29W12814A Series

### Program, Erase and Erase Verify

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Write cycle time	$t_{CWC}$	120	—	—	ns		
Serial clock cycle time	$t_{SCC}$	50	—	—	ns		
$\overline{CE}$ setup time	$t_{CES}$	0	—	—	ns		
$\overline{CE}$ hold time	$t_{CEH}$	0	—	—	ns		
Write pulse time	$t_{WP}$	60	—	—	ns	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$	
Write pulse high time	$t_{WPH}$	40	—	—	ns		
Address setup time	$t_{AS}$	50	—	—	ns		
Address hold time	$t_{AH}$	10	—	—	ns		
Data setup time	$t_{DS}$	50	—	—	ns		
Data hold time	$t_{DH}$	10	—	—	ns		
$\overline{OE}$ setup time before command write	$t_{OEWS}$	0	—	—	ns		
$\overline{OE}$ setup time before read	$t_{OEPS}$	40	—	—	ns		
Time to device busy	$t_{DB}$	—	—	150	ns		
Auto erase time (Sector)	$t_{ASE}$	—	0.8	20	ms		
Auto erase time (Block)	$t_{ABE}$	—	0.8	20	ms		
Auto program time	$t_{ASP}$	—	0.3	20	ms		
$\overline{CE}$ pulse high time	$t_{CPH}$	200	—	—	ns		
Write cycle time for control byte program	$t_{CWCC}$	2.5	—	—	$\mu$ s		
SC pulse width	$t_{SP}$	20	—	—	ns		
SC pulse low time	$t_{SPL}$	20	—	—	ns		
Data setup time for SC	$t_{SDS}$	0	—	—	ns		
Data hold time for SC	$t_{SDH}$	30	—	—	ns	$\overline{CDE} = V_{IL}$	
SC setup for $\overline{WE}$	$t_{SW}$	20	—	—	ns	$\overline{CDE} = V_{IL}$	
SC setup for $\overline{CE}$	$t_{SCS}$	0	—	—	ns		
SC hold time for $\overline{WE}$	$t_{SCHW}$	20	—	—	ns		
$\overline{CE}$ to output delay	$t_{CE}$	—	—	120	ns		
$\overline{OE}$ to output delay	$t_{OE}$	—	—	60	ns		
$\overline{OE}$ high to output float	$t_{DF}$	—	—	40	ns	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$	1
$\overline{RES}$ to write setup time	$t_{RP}$	1	—	—	ms		

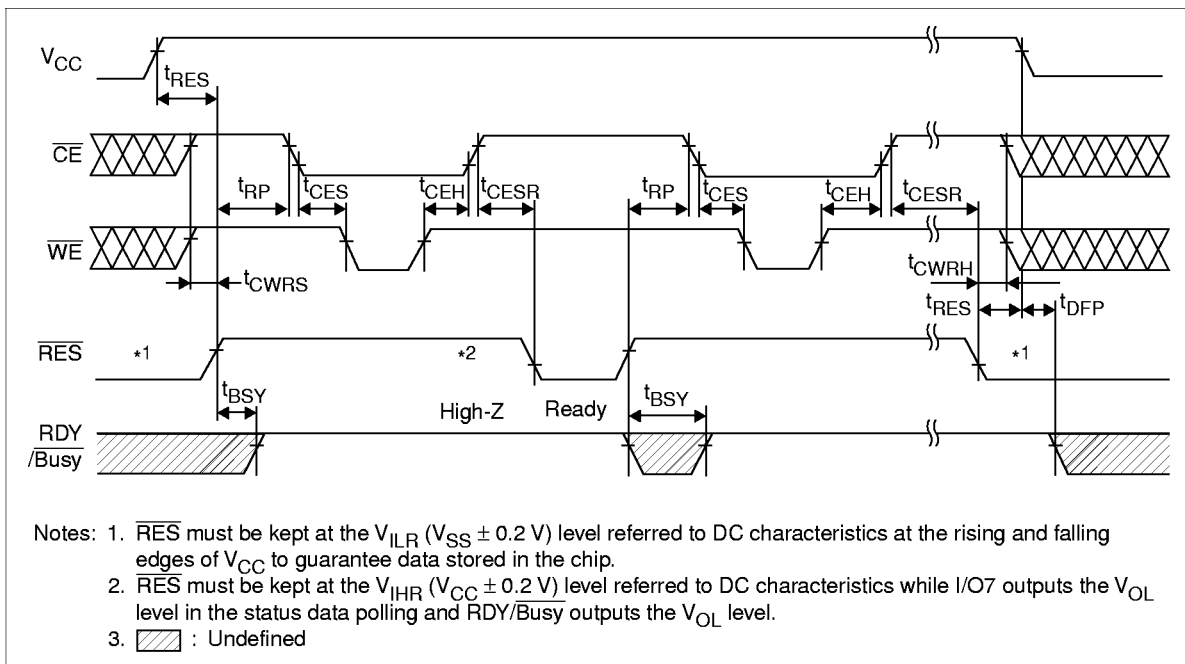
## HN29W12814A Series

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
$\overline{\text{CDE}}$ setup time for $\overline{\text{WE}}$	$t_{\text{CDS}}$	0	—	—	ns		
$\overline{\text{CDE}}$ hold time for $\overline{\text{WE}}$	$t_{\text{CDH}}$	20	—	—	ns		
$\overline{\text{WE}}$ to erase verify	$t_{\text{OEV}}$	20	—	—	$\mu\text{s}$		
$\overline{\text{CDE}}$ setup time for SC	$t_{\text{CDSS}}$	100	—	—	ns		
Next cycle ready time	$t_{\text{RDY}}$	0	—	—	ns		
$\overline{\text{CDE}}$ to $\overline{\text{CE}}$ , $\overline{\text{OE}}$ hold time	$t_{\text{CDCH}}$	50	—	—	ns		
$\overline{\text{CDE}}$ to output delay	$t_{\text{CDAC}}$	—	—	50	ns		
$\overline{\text{CDE}}$ to output invalid	$t_{\text{CDF}}$	0	—	—	ns		

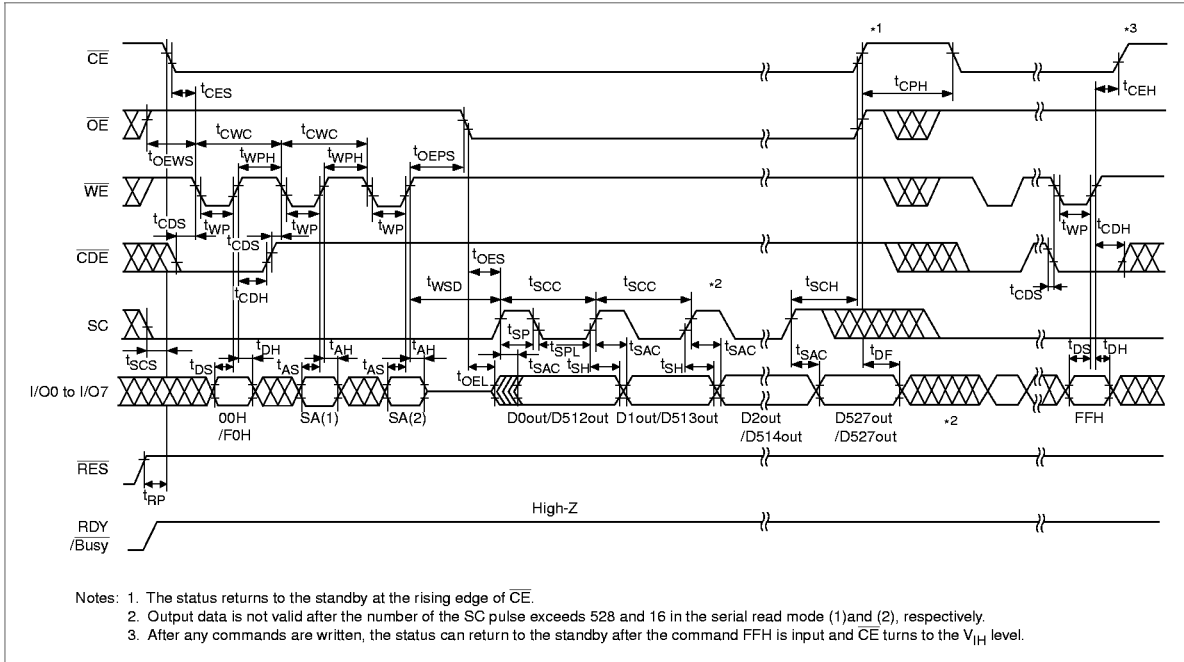
Note: 1.  $t_{\text{DF}}$  is a time after which the I/O pins become open.

## Timing Waveforms

### Power on and off Sequence

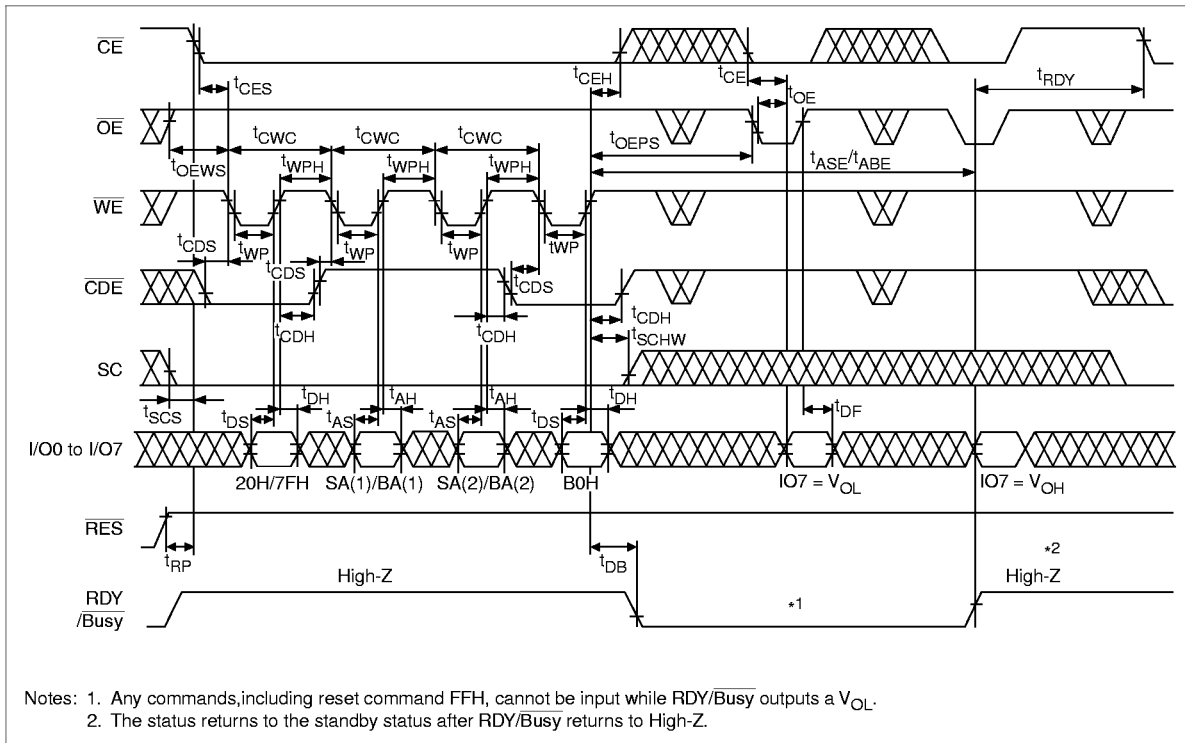


Serial Read (1) (2) Timing Waveform



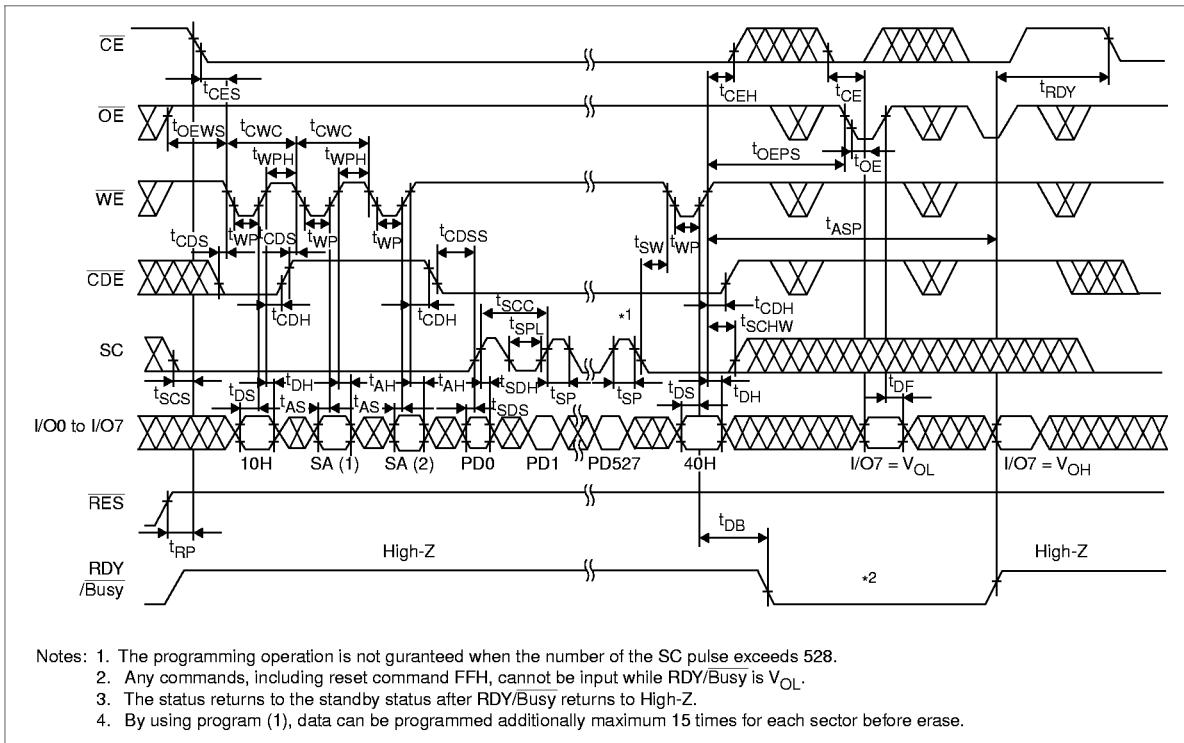
# HN29W12814A Series

## Erase and Status Data Polling Timing Waveform (Sector Erase/Block Erase)



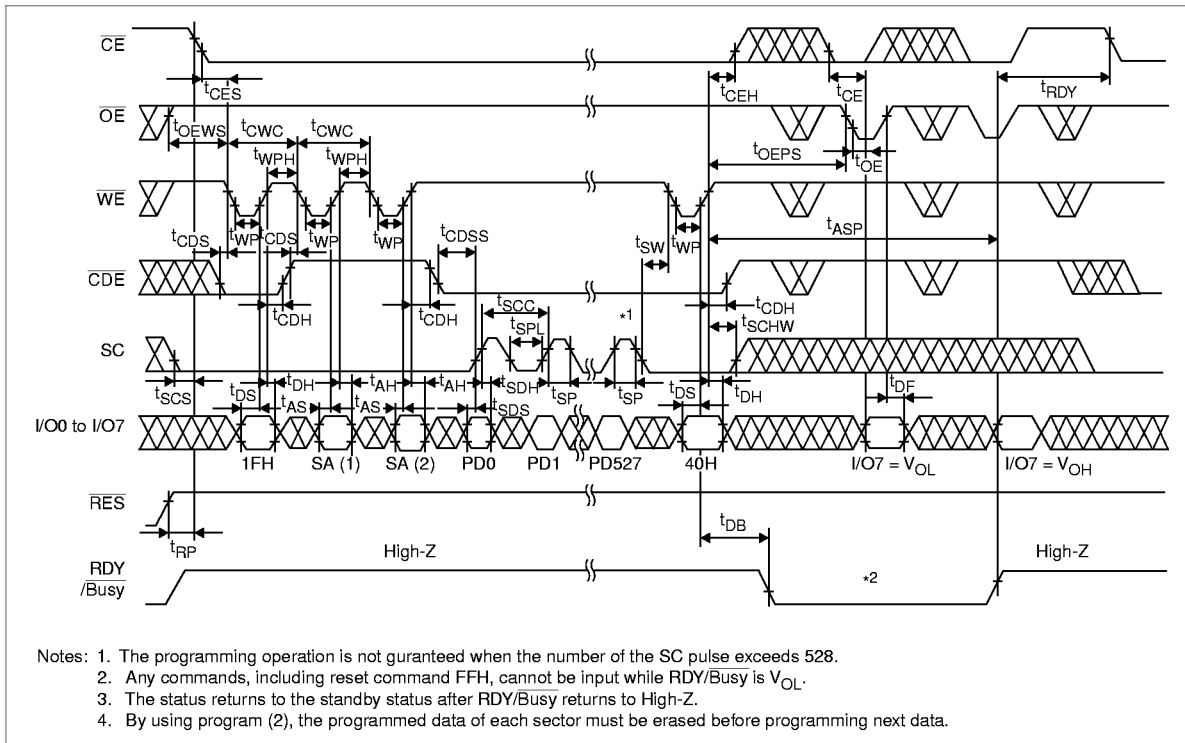


Program (1) and Status Data Polling Timing Waveform

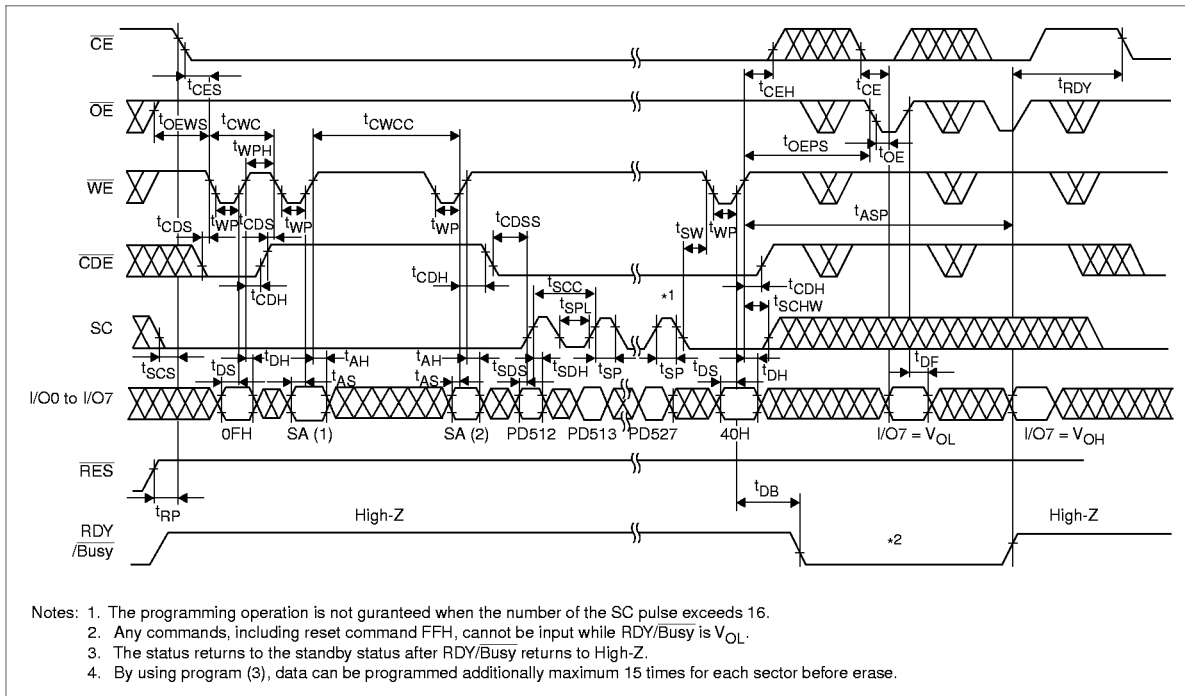


# HN29W12814A Series

## Program (2) and Status Data Polling Timing Waveform

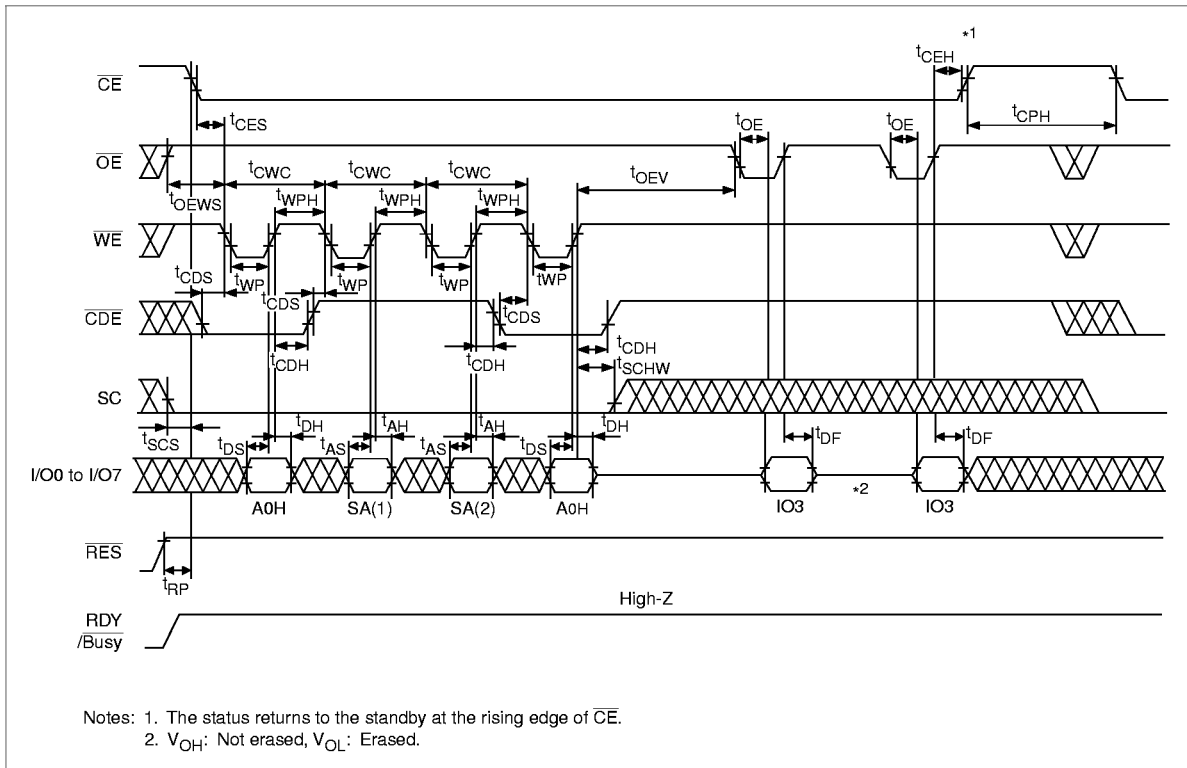


## Program (3) and Status Data Polling Timing Waveform

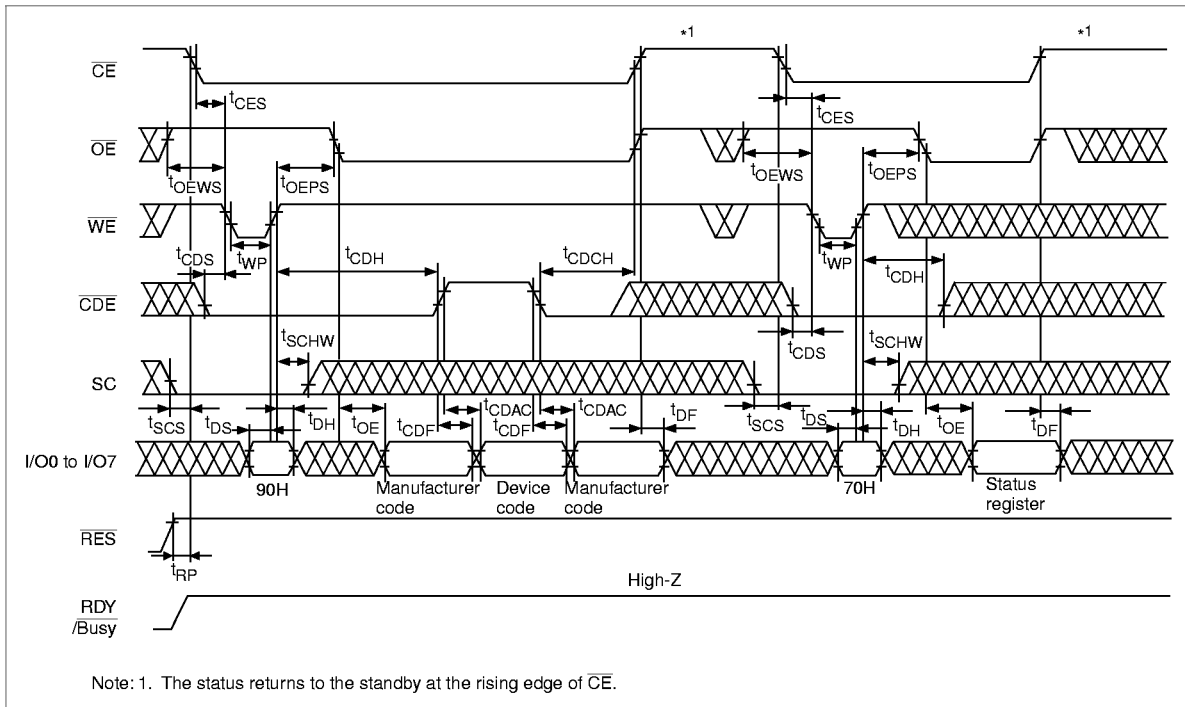


# HN29W12814A Series

## Erase Verify Timing Waveform



## ID and Status Register Read Timing Waveform



## Notes

### Unusable Sector

Initially, the HN29W12814A contains unusable sectors. Due to the nature of the device architecture, the device can also be screened and tested for partial invalid sectors for selected systems that can utilize the devices.

1. Tested for partial invalid sectors. The usable sectors were programmed the following data.

Column address	000H to 1FFH	200H	201H	202H	203H	204H	205H	206H to 20FH
Data	FFH	1CH	71H	C7H	1CH	71H	C7H	FFH

2. No erase and program for the partial invalid sectors by the system.

Item	Min
Usable sectors (initially)	32,114 (98%)

# HN29W12814A Series

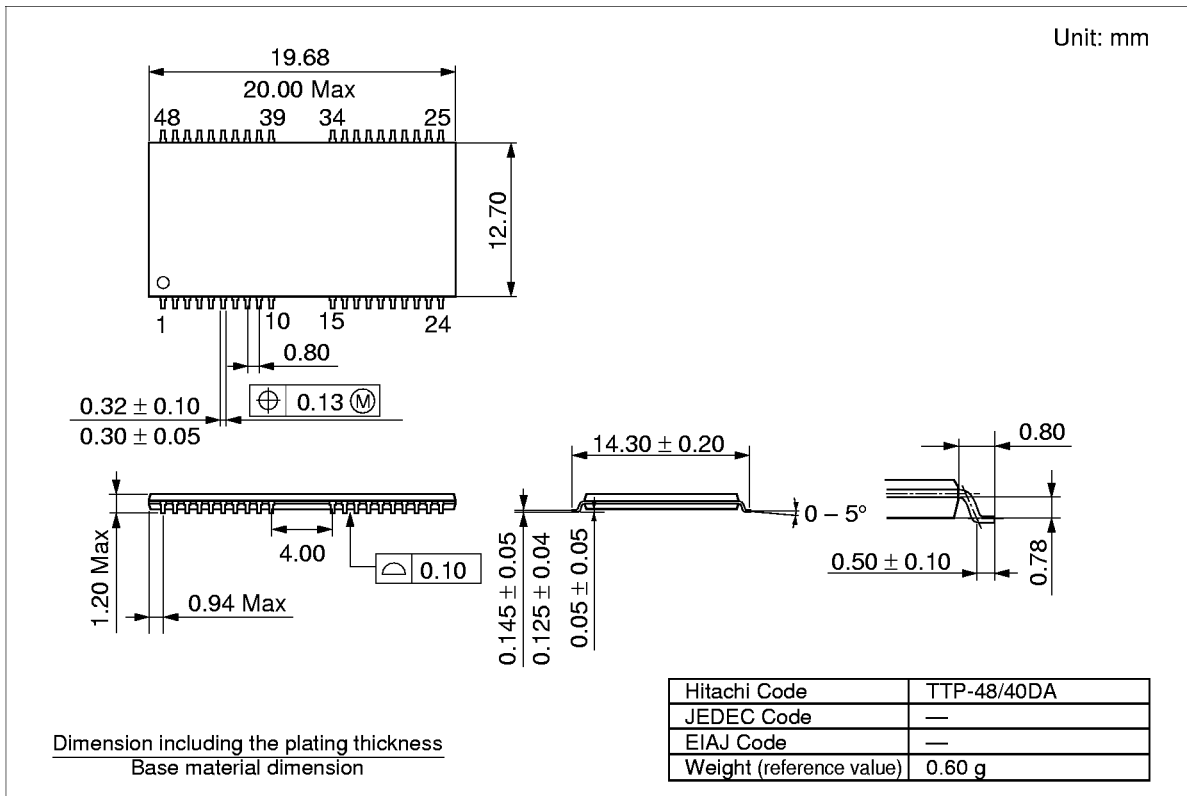
## Enable High System Reliability

The device may fail during a program or erase operation due to write or erase cycle. The following architecture will enable high system reliability if a failure occurs.

1. Error in read: Error correction that more than 1 bit error correction per each sector read is required for data reliability.
2. Error in program or erase operation: The device may fail during a program or erase operation due to write or erase cycle. The status register are indicated that the erase and program operation complete in a finite time. When the error happens in sector, try to reprogram the data into another sector. Then, prevent further system access to sector that error happens. Typically, recommended number of a spare sectors are 1.8% within initial usable 32,114 sectors by the each device.
3. Prolongation of Flash memory life: The write/erase endurance is  $3 \times 10^5$  cycles and the data retention time is more than 10 years under the condition of the error correction.

## Package Dimensions

### HN29W12814ATT Series (TTP-48/40DA)



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## HN29W12814A Series

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## Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Jul. 21, 1998	Initial issue	M. Shirai	H. Uchida
1.0	Dec. 18, 1998	AC Characteristics $t_{ASE}, t_{ABE}$ typ: 1 ms to 0.8 ms $t_{ASP}$ typ: 0.2 ms to 0.3 ms Notes Addition of Unusable sector table: 000H to 1FFH and 206H to 20FH write/erase endurance: $3 \times 10^5$ cycles to $1 \times 10^5$ cycles	M. Shirai	T. Furuno
2.0	Feb. 20, 1999	Notes write/erase endurance: $1 \times 10^5$ cycles to $3 \times 10^5$ cycles		