

Features

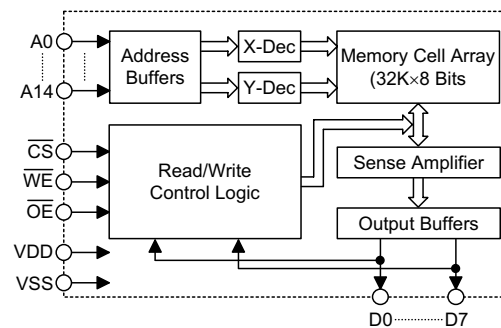
- Operation voltage: 2.7V~3.3V
- Low power consumption:
 - Operating current: 20mA max.
 - Standby current: 2μA
- High speed access time: 70ns
- Input levels are LVTTTL-compatible
- Automatic power down when chip is deselected
- Three state outputs
- Fully static operation
- Data retention supply voltage as low as 2.0V
- Easy expansion with \overline{CS} and \overline{OE} options
- 28-pin SOP/TSOP package

General Description

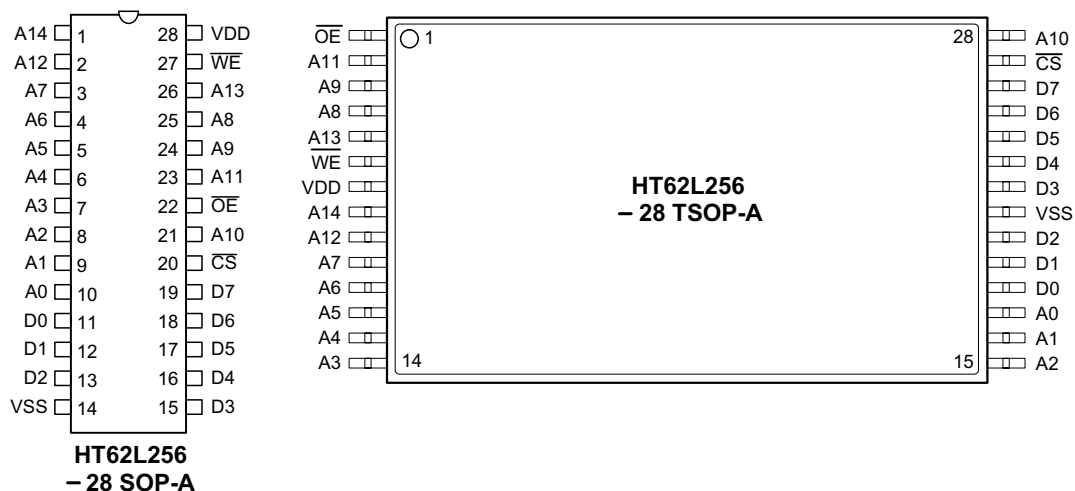
The HT62L256 is a 262,144-bit static random access memory organized into 32,768 words by 8 bits and operating from a low power range of 2.7V to 3.3V supply voltage. It is fabricated with high performance CMOS process that provides both high speed and low power feature with typical standby current of 2μA and maximum access time of 70ns.

The HT62L256 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The HT62L256 supports the JEDEC standard 28-pin SOP and TSOP package.

Block Diagram



Pin Assignment



Pin Description

Pin Name	I/O	Description
A0~A14	I	Address input pins
\overline{WE}	I	Write enable signal pin, active LOW
\overline{OE}	I	Output enable signal pin, active LOW
\overline{CS}	I	Chip select signal pin, active LOW
D0~D7	I/O	Data input and output signal pins
VDD	—	Positive power supply
VSS	—	Negative power supply, ground

Absolute Maximum Rating

V_{DD} to V_{SS} -0.5V to +3.6V Operating Temperature, T_{OP} 0°C to 70°C
 IN, IN/OUT Voltage to V_{SS} -0.5V to V_{DD}+0.5V Storage Temperature (Plastic), T_{stg} ... -55°C to 125°C
 Power Consumption, P_T 0.7W

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

T_a=25°C, V_{DD}=3.0V±10%, T_{OP}=0°C to 70°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{DD}	Operating Voltage	—	2.7	3.0	3.3	V
V _{IL}	Input Low Voltage	—	—	0	0.4	V
V _{IH}	Input High Voltage	—	0.7×V _{DD}	—	—	V
I _{LI}	Input Leakage Current	V _{IN} =0 to V _{DD}	—	—	1	μA
I _{LO}	Output Leakage Current	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, V _{OUT} =0 to V _{DD}	—	—	1	μA
V _{OL}	Output Low Voltage	V _{DD} =Max, I _{OL} =2mA	—	—	0.3	V
V _{OH}	Output High Voltage	V _{DD} =Min, I _{OH} =-1mA	V _{DD} -0.3	—	—	V
I _{DD}	Operating Current	$\overline{CS}=V_{IH}$, I _{OUT} =0mA	—	—	20	mA
I _{SB1}	Standby Current	$\overline{CS}=V_{IH}$, I _{OUT} =0mA	—	—	50	μA
I _{SB2}	Power Down Supply Current	$\overline{CS} \geq V_{DD} - 0.2V$, V _{IN} ≥0V	—	2	10	μA

A.C. Characteristics

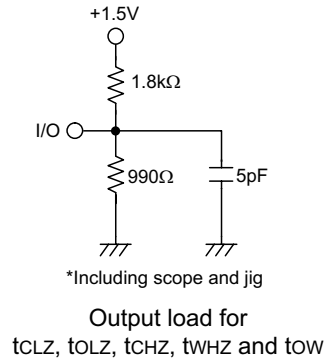
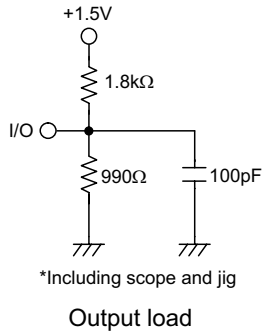
Ta=25°C, V_{DD}=3.0V±10%

Symbol	Parameter	Min.	Typ.	Max.	Unit
Read cycle					
t _{RC}	Read Cycle Time	70	—	—	ns
t _{AA}	Address Access Time	—	—	70	ns
t _{ACS}	Chip Selection Access Time	—	—	70	ns
t _{AOE}	Output Enable to Valid Outputs	—	—	35	ns
t _{CLZ} *	Chip Selection to Output in Low-Z	10	—	—	ns
t _{OLZ} *	Output Enabled to Output in Low-Z	5	—	—	ns
t _{CHZ} *	Chip Deselected to Output in High-Z	—	—	25	ns
t _{OHZ} *	Output Disable to Output in High-Z	—	—	25	ns
t _{OH}	Output Hold from Address Change	10	—	—	ns
Write cycle					
t _{WC}	Write Cycle Time	70	—	—	ns
t _{CW}	Chip Selection to End of Write	60	—	—	ns
t _{AS}	Address Setup Time	0	—	—	ns
t _{AW}	Address Valid to End of Write	60	—	—	ns
t _{WP}	Write Pulse Width	50	—	—	ns
t _{WR}	Write Recovery Time	0	—	—	ns
t _{WHZ}	Write to Output in High-Z	—	—	20	ns
t _{DW}	Data Valid to End of Write	30	—	—	ns
t _{DH}	Data Hold from End of Write	0	—	—	ns
t _{OW}	Output Active from End of Write	5	—	—	ns

- Note:
1. A write cycle occurs during the overlap of a low \overline{CS} and a low \overline{WE}
 2. \overline{OE} may be both high and low in a write cycle
 3. t_{AS} is specified from \overline{CS} or \overline{WE} , whichever occurs last
 4. t_{WP} is an overlap time of a low \overline{CS} and a low \overline{WE}
 5. t_{WR}, t_{DW} and t_{DH} are specified from \overline{CS} or \overline{WE} , whichever occurs first
 6. t_{WHZ} is specified by the time when DATA OUT is floating and not defined by the output level
 7. When the I/O pins are in data output mode, they should not be forced with inverse signals

A.C. Test Conditions

Item	Conditions
Input Pulse Level	0V to 3V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
Output Load	See figures below



Functional Description

Operation truth table

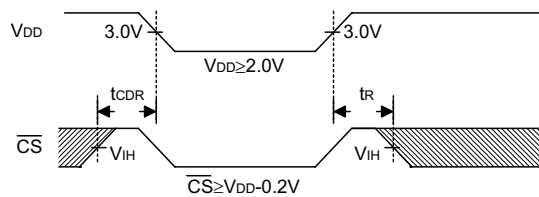
\overline{CS}	\overline{OE}	\overline{WE}	Mode	D0~D7
H	X	X	Standby	High-Z
L	H	H	Output Disable	High-Z
L	L	H	Read	Dout
L	X	L	Write	Din

Data retention characteristics

Ta=-40°C to 85°C

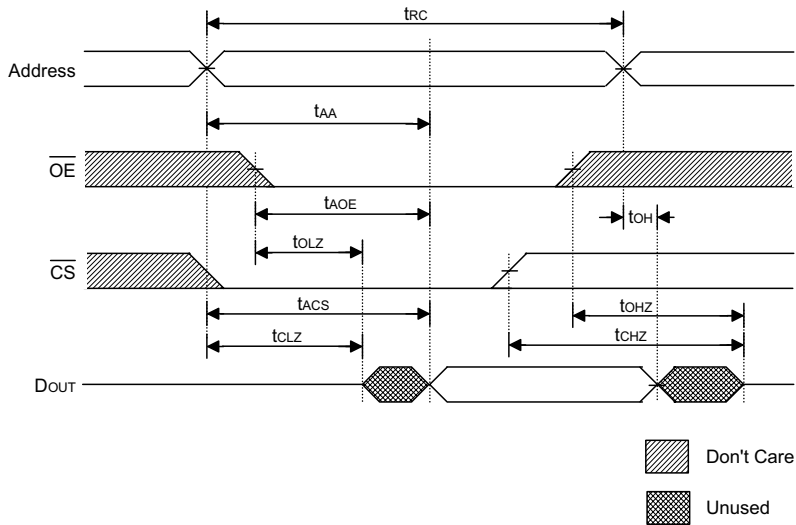
Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{DR}	V _{DD} for Data Retention	$\overline{CS} \geq V_{DD}-0.2V$ $V_{IN} \geq V_{DD}-0.2V$ or $V_{IN} \leq 0.2V$	2.0	3.3	V
I _{CCDR}	Data Retention Current	$\overline{CS} \geq V_{DD}-0.2V$ $V_{IN} \geq V_{DD}-0.2V$ or $V_{IN} \leq 0.2V$	—	2	μA
t _{CDR}	Chip Disable Data Retention Time	See retention timing	0	—	ns
t _R	Operation Recovery Time	See retention timing	t _{RC} *	—	ns

Low V_{DD} data retention timing

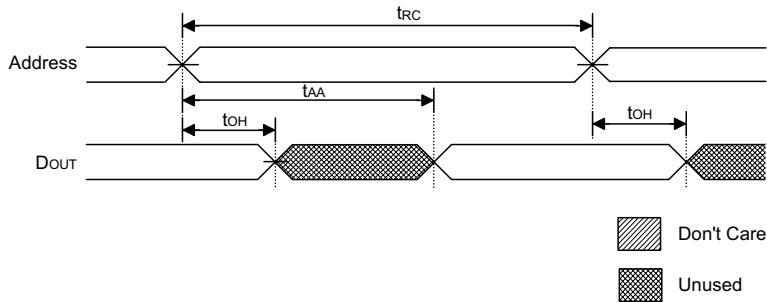


Timing Diagrams

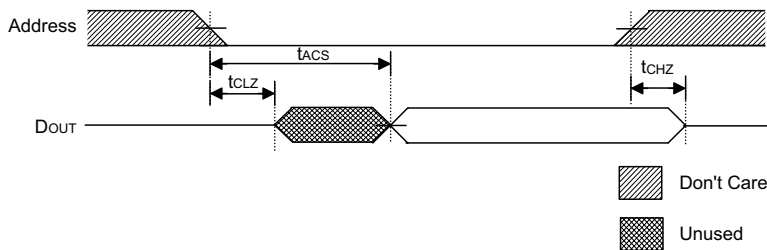
Read cycle 1 output enable controlled (1)



Read cycle 2 address controlled (1, 2, 4)

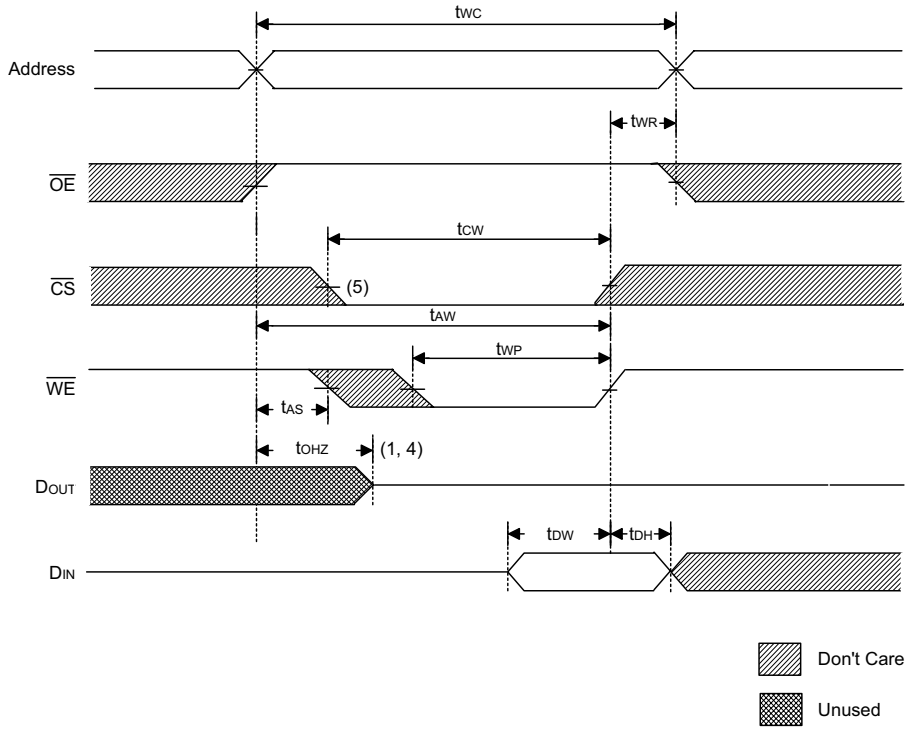


Read cycle 3 chip select controlled (1, 3, 4)

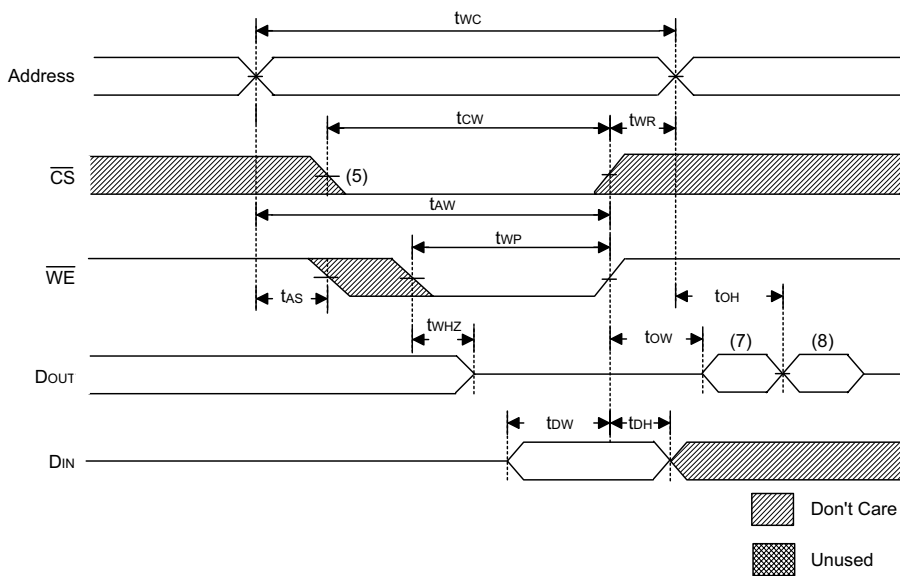


- Note:
1. \overline{WE} is high for read cycle
 2. Device is continuously enabled, $\overline{CS}=V_{IL}$
 3. Address is valid prior to or coincident with the \overline{CS} transition low
 4. $\overline{OE}=V_{IL}$
 5. Transition is measured at $\pm 500\text{mV}$ from the steady state

Write cycle 1 \overline{OE} clock (1)



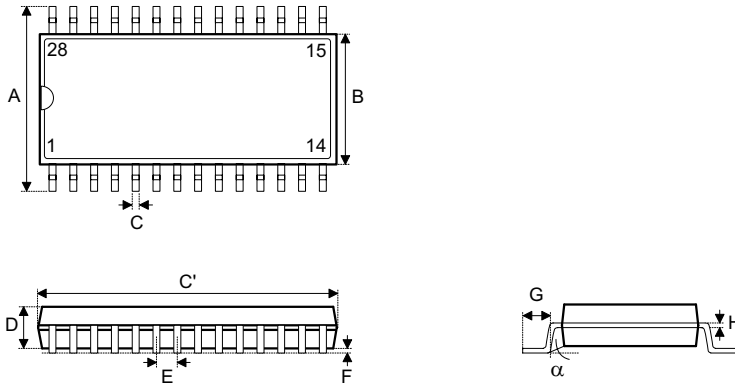
Write cycle 2 $\overline{OE}=V_{IL}$ Fixed (1, 6)



- Note:
1. \overline{WE} must be high during all address transitions
 2. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE}
 3. t_{WR} is measured from the earliest high going edge of \overline{CS} or \overline{WE} to the end of the write cycle
 4. During this period, I/O pins are in the output state, so the input signals of opposite phase to the outputs should not be applied.
 5. If the \overline{CS} low transition occurs simultaneously or after with the \overline{WE} low transition, the outputs remain in a high impedance state
 6. \overline{OE} is continuously low ($\overline{OE}=V_{IL}$)
 7. D_{OUT} is at the same phase as the write data of this write cycle
 8. D_{OUT} is the read data of the next address
 9. If CS is low during this period, then the I/O pins are in the output state and the data input signals of the opposite phase to the outputs should not be applied
 10. Transition is measured at $\pm 500\text{mV}$ from the steady state

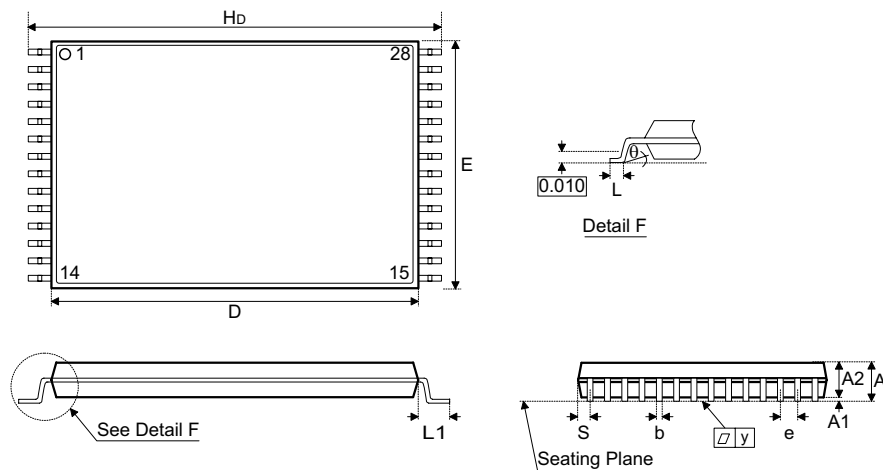
Package Information

28-pin SOP (330mil) outline dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	453	—	477
B	326	—	336
C	14	—	20
C'	700	—	728
D	92	—	104
E	—	50	—
F	4	—	—
G	32	—	38
H	4	—	12
α	0°	—	10°

28-pin TSOP (8×13.4) outline dimensions



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	—	1.25
A1	0.08	—	0.18
A2	0.95	—	1.05
b	—	0.20	—
D	11.70	—	11.90
H_D	13.20	—	13.60
E	7.90	—	8.10
e	—	0.55	—
L	—	0.50	—
L_1	—	0.8	—
θ	0°	—	5°

Holtek Semiconductor Inc. (Headquarters)

No.3, Creation Rd. II, Science-based Industrial Park, Hsinchu, Taiwan
Tel: 886-3-563-1999
Fax: 886-3-563-1189
<http://www.holtek.com.tw>

Holtek Semiconductor Inc. (Sales Office)

11F, No.576, Sec.7 Chung Hsiao E. Rd., Taipei, Taiwan
Tel: 886-2-2782-9635
Fax: 886-2-2782-9636
Fax: 886-2-2782-7128 (International sales hotline)

Holtek Semiconductor (Shanghai) Inc.

7th Floor, Building 2, No.889, Yi Shan Rd., Shanghai, China
Tel: 021-6485-5560
Fax: 021-6485-0313
<http://www.holtek.com.cn>

Holtek Semiconductor (Hong Kong) Ltd.

RM.711, Tower 2, Cheung Sha Wan Plaza, 833 Cheung Sha Wan Rd., Kowloon, Hong Kong
Tel: 852-2-745-8288
Fax: 852-2-742-8657

Holmate Semiconductor, Inc.

48531 Warm Springs Boulevard, Suite 413, Fremont, CA 94539
Tel: 510-252-9880
Fax: 510-252-9885
<http://www.holmate.com>

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