

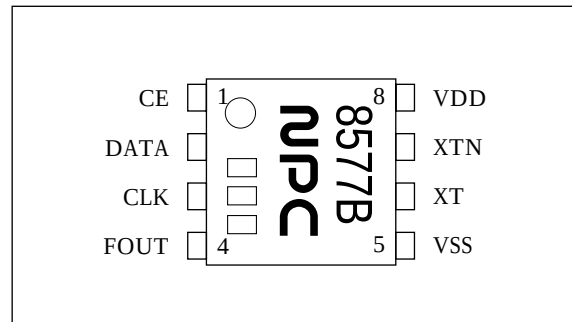
OVERVIEW

The SM8577B is a CMOS serial-interface type real-time clock IC that operates at 32.768 kHz. It employs a 3-line serial interface to transfer time and date data. It incorporates a supply-voltage detect function to determine data validity/invalidity. It features an output interrupt with 32 kHz or 1 Hz output frequency. It is available in 8-pin SOPs.

FEATURES

- 2.5 to 5.5 V operating voltage range
- 1.0 μ A at 3.0 V (typ) current consumption
- 3-line serial interface
- 1.7 ± 0.3 V supply voltage detection threshold
- Timer counters for second, minute, hour, day, day of the week, month, and year
- Automatic leap-year calendar adjustment
- 32.768 kHz and 1 Hz output interrupt selectable
- Crystal oscillator circuit built-in (C_D built-in)
- 24-hour time mode
- 8-pin SOP

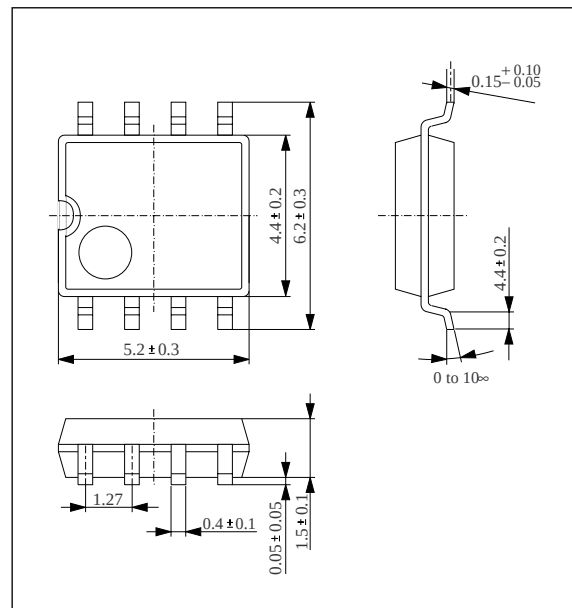
PINOUT



PACKAGE DIMENSIONS

Unit: mm

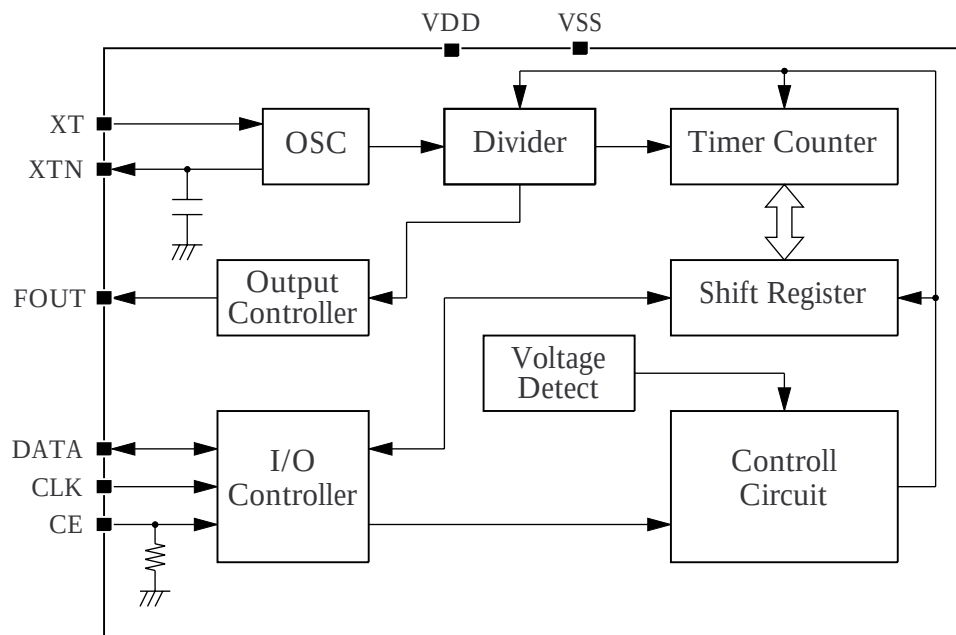
8-pin SOP



ORDERING INFORMATION

Device	Package
SM8577BS	8pin SOP

BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description
1	CE	I	Chip enable. With pull-down resistor built-in. HIGH: Enable LOW: DATA goes high impedance; input on CLK and DATA stops; and the TM bit is cleared.
2	DATA	I/O	Data read and write input/output
3	CLK	I	Serial clock input. Data is input (write mode) and output (read mode) on the rising edge of CLK.
4	FOUT	O	Frequency output (controlled by the 4th data bit of the 'week' data, FSEL). 1 Hz output when FSEL is 0, and 32.768 kHz output when FSEL is 1. In 1 Hz output mode, the 1 Hz signal is synchronized to the internal 1 second signal. FOUT output is not affected by the CE signal.
5	VSS	—	Ground
6	XT	I	Crystal oscillator element connection pin
7	XTN	O	Crystal oscillator element connection pin. Oscillator capacitor C_D is built-in.
8	VDD	—	Supply voltage. Connect a $\geq 0.1 \mu\text{F}$ capacitor between VDD and VSS.

SPECIFICATIONS

Absolute Maximum Ratings

$V_{SS} = 0\text{ V}$

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		−0.3 to 7.0	V
Input voltage range	V_{IN}		$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Output voltage range	V_{OUT}		$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Storage temperature range	T_{stg}		−55 to 125	°C
Power dissipation	P_D		150	mW
Soldering temperature	T_{sld}		255	°C
Soldering time	t_{sld}		10	s

Recommended Operating Conditions

$V_{SS} = 0\text{ V}$

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		2.5 to 5.5	V
Operating temperature range	T_{opr}		−40 to 85	°C

Oscillator Characteristics

$V_{SS} = 0\text{ V}$, $T_a = 25\text{ °C}$, $C_G = 12\text{ pF}$, Seiko Epson C-002SH crystal ($C_1 = 30\text{ k}\Omega$, $C_L = 6\text{ pF}$) unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Oscillator start time	t_{STA}	$V_{DD} = 2.5\text{ V}$	–	–	3	s
Oscillator start voltage	V_{STA}		1.5	–	–	V
Oscillator stop voltage	V_{STO}		–	–	1.5	V
Frequency voltage characteristic	f/V	$V_{DD} = 2.0$ to 5.5 V	−2	–	+2	ppm/V
Frequency accuracy	ε	$V_{DD} = 5.0\text{ V}$	−10	–	+10	ppm
Output capacitance	C_D	$V_{DD} = 5.0\text{ V}$	–	12	–	pF

DC Electrical Characteristics

$V_{SS} = 0\text{ V}$, $V_{DD} = 5.0\text{ V} \pm 10\%$, $T_a = -40$ to $85\text{ }^{\circ}\text{C}$ unless otherwise noted

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Current consumption	I _{DD1}	V _{DD} = 5.0 V	CE = V _{SS}	–	1.5	3.0	μA
	I _{DD2}	V _{DD} = 3.0 V		–	1.0	2.0	μA
HIGH-level input voltage	V _{IH}	CE, CLK, DATA		0.8V _{DD}	–	–	V
LOW-level input voltage	V _{IL}	CE, CLK, DATA		–	–	0.2V _{DD}	V
Input resistance	R _{IN}	CE: V _{IN} = 5.0 V		–	–	800	kΩ
Input OFF leakage current	I _{leak}	CLK: V _{IN} = V _{DD} or V _{SS} CE: V _{IN} = V _{SS}		–	–	0.5	μA
HIGH-level output voltage	V _{OH1}	V _{DD} = 5.0 V	DATA, FOUT: I _{OH} = –1.0 mA	4.5	–	–	V
	V _{OH2}	V _{DD} = 3.0 V		2.0	–	–	V
LOW-level output voltage	V _{OL1}	V _{DD} = 5.0 V	DATA, FOUT: I _{OL} = 1.0 mA	–	–	V _{SS} + 0.5	V
	V _{OL2}	V _{DD} = 3.0 V		–	–	V _{SS} + 0.8	V
Output leakage current	I _{OZH}	DATA, FOUT: V _{OUT} = 5.5 V		–1.0	–	1.0	μA
	I _{OZL}	DATA, FOUT: V _{OUT} = 0 V		–1.0	–	1.0	μA
Supply voltage detect threshold voltage	V _{DET}			1.4	1.7	2.0	V

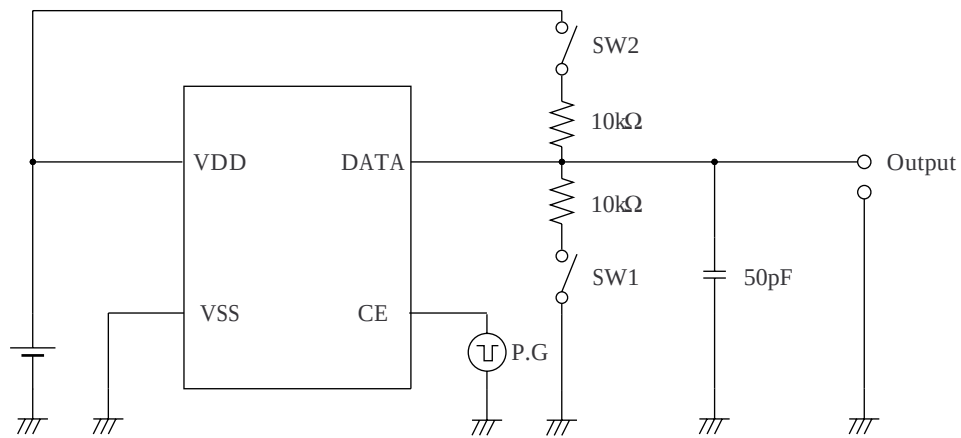
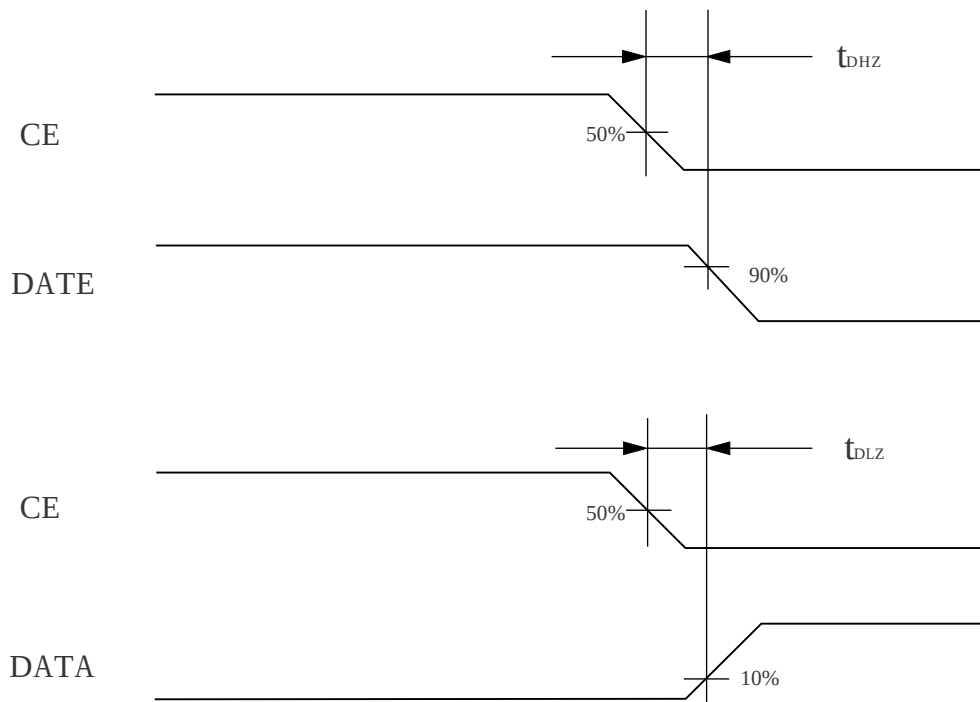
AC Characteristics

$V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -40\text{ to }85\text{ }^\circ\text{C}$, $C_L = 50\text{ pF}$ unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	max	min	
CLK clock period	t_{CLK}		0.75	–	7800	μs
CLK LOW-level pulsewidth	t_{CLKL}		0.375	–	3900	μs
CLK HIGH-level pulsewidth	t_{CLKH}		0.375	–	3900	μs
CE setup time	t_{CES}		0.375	–	3900	μs
CE hold time	t_{CEH}		0.375	–	–	μs
CE enable time	t_{CE}		–	–	0.9	s
Write data setup time	t_{SD}		0.1	–	–	μs
Write data hold time	t_{HD}		0.1	–	–	μs
DATA output delay time	t_{DATD}		–	–	0.2	μs
DATA output floating time	t_{DZ}	See measurement circuit.	–	–	0.1	μs
Clock rise time	t_{r1}		–	–	50	ns
Clock fall time	t_{f1}		–	–	50	ns
FOUT rise time	t_{r2}	$C_L = 30\text{ pF}$	–	–	100	ns
FOUT fall time	t_{f2}	$C_L = 30\text{ pF}$	–	–	100	ns
FOUT duty cycle	Duty	$C_L = 30\text{ pF}$, 32 kHz output	40	–	60	%
Wait time	t_{RCV}		0.95	–	–	μs

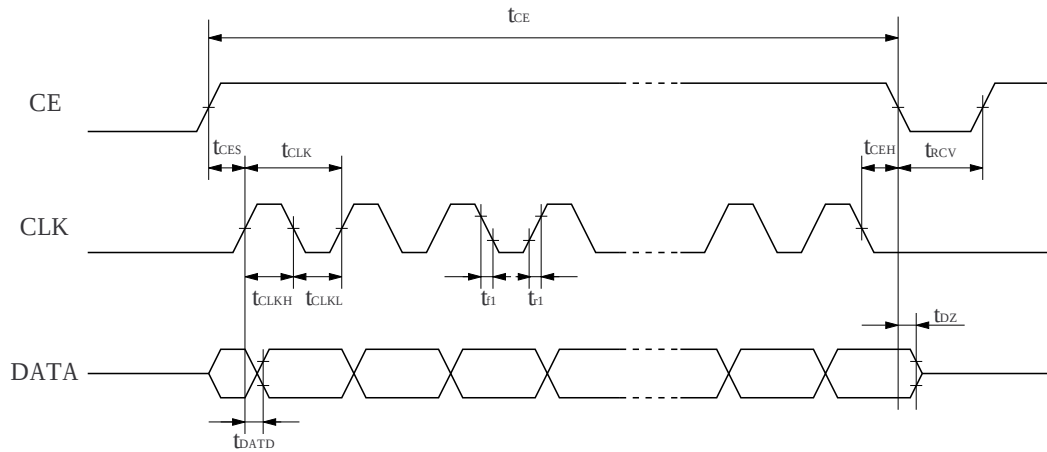
$V_{DD} = 3\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -40\text{ to }85\text{ }^\circ\text{C}$, $C_L = 50\text{ pF}$ unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	max	min	
CLK clock period	t_{CLK}		1.5	–	7800	μs
CLK LOW-level pulsewidth	t_{CLKL}		0.75	–	3900	μs
CLK HIGH-level pulsewidth	t_{CLKH}		0.75	–	3900	μs
CE setup time	t_{CES}		0.75	–	3900	μs
CE hold time	t_{CEH}		0.75	–	–	μs
CE enable time	t_{CE}		–	–	0.9	s
Write data setup time	t_{SD}		0.2	–	–	μs
Write data hold time	t_{HD}		0.1	–	–	μs
DATA output delay time	t_{DATD}		–	–	0.4	μs
DATA output floating time	t_{DZ}	See measurement circuit.	–	–	0.2	μs
Clock rise time	t_{r1}		–	–	100	ns
Clock fall time	t_{f1}		–	–	100	ns
FOUT rise time	t_{r2}	$C_L = 30\text{ pF}$	–	–	200	ns
FOUT fall time	t_{f2}	$C_L = 30\text{ pF}$	–	–	200	ns
FOUT duty cycle	Duty	$C_L = 30\text{ pF}$, 32 kHz output	40	–	60	%
Wait time	t_{RCV}		1.9	–	–	μs

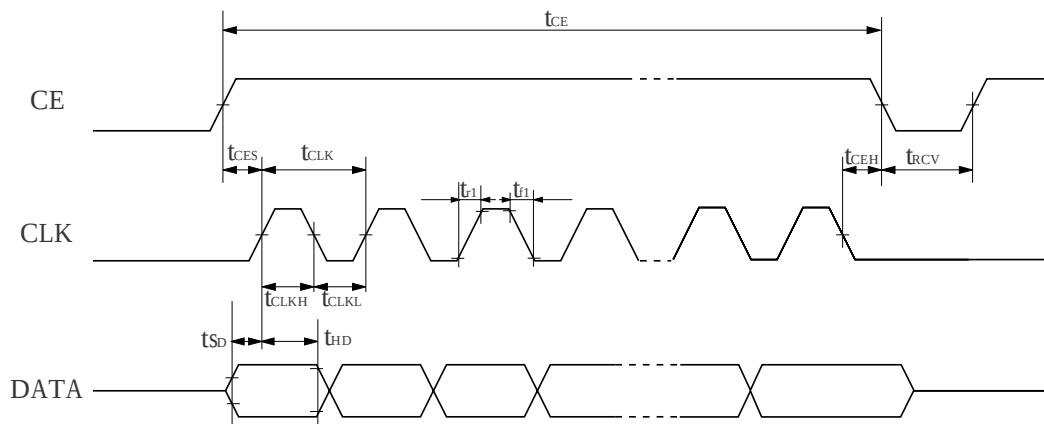
Measurement Circuit**DATA Output Floating Timing**

Timing Diagrams

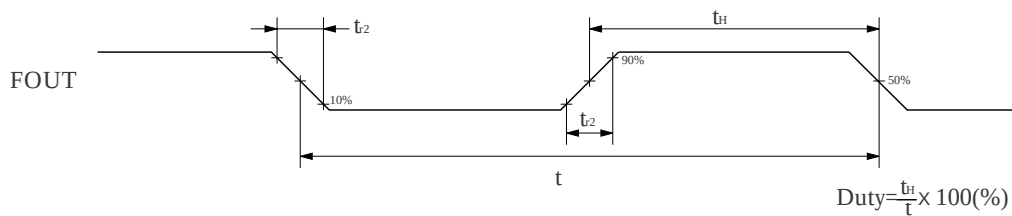
Data read



Data write



FOUT output



Note that the 1 Hz and 32 kHz oscillators are not synchronized to each other, so switching between 1 Hz and 32 kHz output temporarily shortens the duty cycle. Accordingly, a wait time ($\geq$ output frequency period) should be incorporated when switching during normal operation.

FUNCTIONAL DESCRIPTION

Timer Data Configuration

Counter data is stored in BCD format. The IC performs long/short month and leap-year adjustment automatically. Leap-year adjustment occurs:

- when the decade digit is odd and the year digit is a 2 or 6, and

- when the decade digit is even and the year digit is a 0, 4 or 8.

The time display is 24-hour mode. All data is written and read with the LSB first.

	MSB				LSB			
Second (0 to 59)	FDT	s40	s20	s10	s8	s4	s2	s1
Minute (0 to 59)	*	mi40	mi20	mi10	mi8	mi4	mi2	mi1
Hour (0 to 23)	*	*	h20	h10	h8	h4	h2	h1
Week (1 to 7)					FSEL	W4	W2	W1
Day (1 to 31)	*	*	d20	d10	d8	d4	d2	d1
Month (1 to 12)	TM	*	*	mo10	mo8	mo4	mo2	mo1
Year (0 to 99)	y80	y40	y20	y10	y8	y4	y2	y1

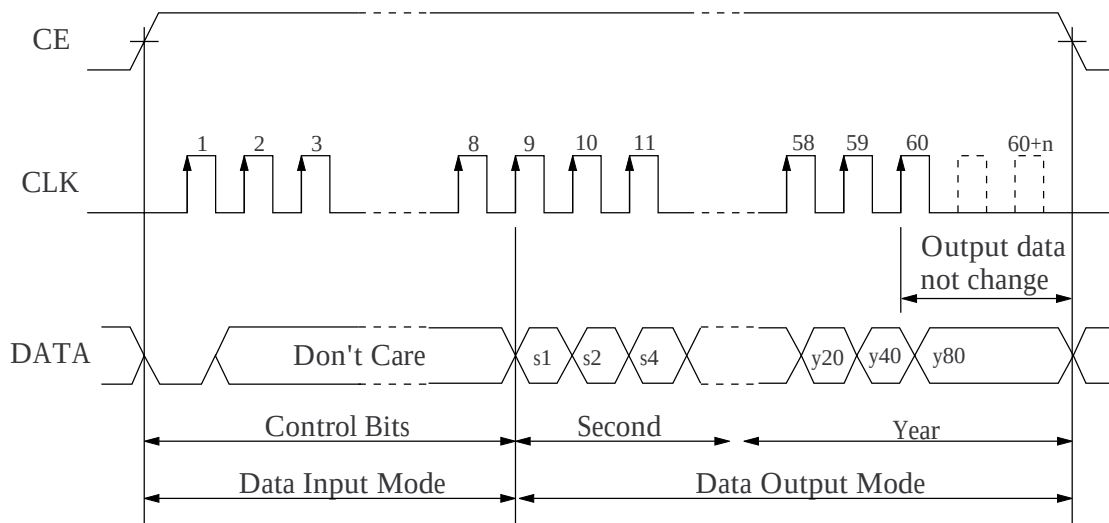
* bits are don't care write bits.

FDT is the supply voltage detect bit. FDT is set to 1 when the voltage between VDD and VSS falls below 1.7 ± 0.3 V. It is reset to 0 for data reads longer than 56 bits. Note that the FDT bit is not reset to 0 for data reads of 55 bits or less. The read/write data bits should initially be set to 0. After the supply voltage is first applied, the FDT bit should also be set to 0.

FSEL is the FOUT output frequency switch control bit. 1 Hz output is selected when FSEL is 0, and 32 kHz output is selected when FSEL is 1. After power is first applied, 1 Hz default mode is selected.

TM is the factory test bit. It should be set to 0 for normal use.

Data Read



When CE is HIGH, data read mode starts from the first rising edge of CLK for which DATA is LOW. Valid data is then output on DATA from the 9th rising edge of CLK. Time and date data is loaded into the shift register on the 8th falling edge of CLK and then output on DATA in sync with the rising edge of CLK, starting with the seconds' digit LSB. Data is loaded and shifted in the sequence second, minute, hour, week, day, and month. The output data is valid for the first 60 rising edges of CLK. Output data does not change after the 60th rising edge, even if clock input continues.

Within the 60 cycles of valid data output, partial data output can be obtained by taking CE LOW after the

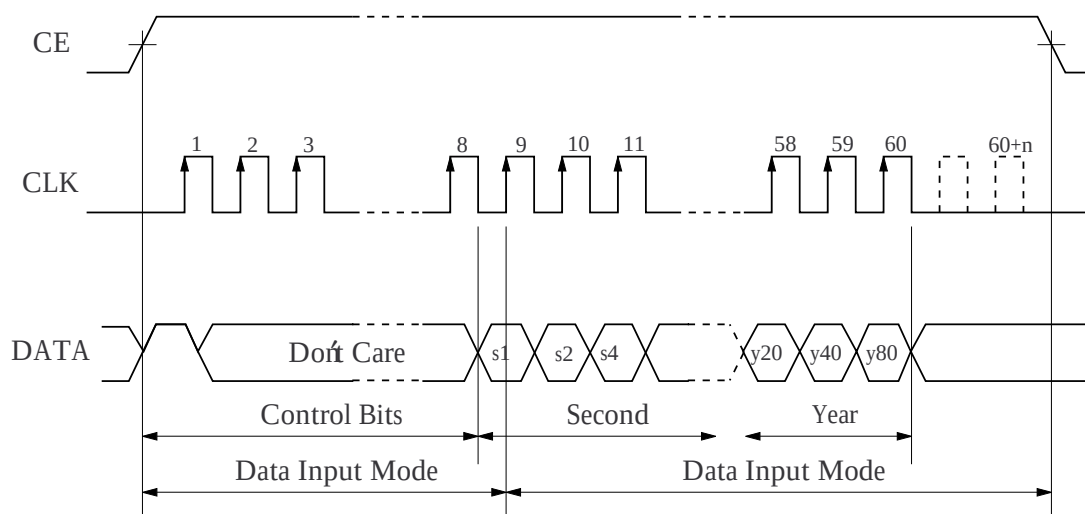
corresponding number of cycles. For example, if only the 'second' to 'week' data output is required, then that data only is output if CE goes LOW after 36 clock cycles.

For continuous data reads, a wait time (t_{RCV}) is required before the next data cycle after CE goes LOW.

Note that if a timer counter update operation (a 1 s carry) occurs during a data read cycle, the data in the shift register is not updated and, as a result, the output data contains an error of -1 s.

The data read cycle should be completed within $t_{CE} \leq 0.9$ s.

Data Write



When CE is HIGH, data write mode starts from the first rising edge of CLK for which DATA is HIGH. Valid data is then input on DATA from the 9th rising edge of CLK. Time and date data is loaded into the shift register in sync with the rising edge of CLK, starting with the seconds' digit LSB. Data is loaded and shifted in the sequence second, minute, hour, week, day, and month. After 60 rising edges of CLK, the shift register contents are then transferred to the timer counters.

Note that a data write cycle must contain 60 bits of input data. If CE goes LOW before 60 bits are input, the input data is invalid. If the input data exceeds 60 bits, data from the 61st bit is ignored (the first 60 bits remain valid).

During a data write cycle, timer counter operation stops on the first falling edge of CLK, and the 1 Hz to 128 Hz frequency divider step counters are reset. The 1 s counter increment signal is stopped and does not restart until CE goes LOW. The divider step counters are reset during the interval between the first falling edge of CLK and the 2nd rising edge of CLK.

The data write cycle should be completed within $t_{CE} \leq 0.9$ s.

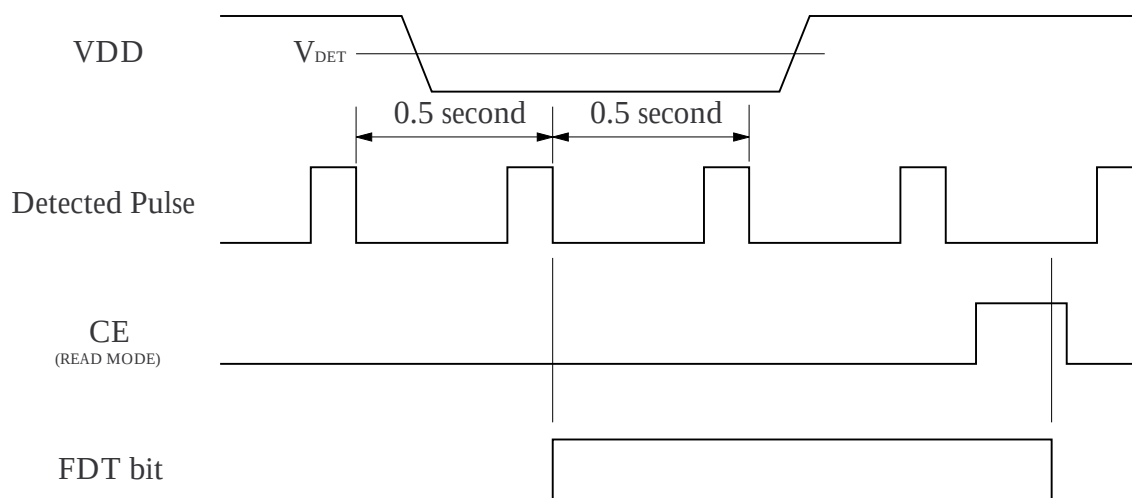
If a data read cycle occurs immediately after a data write cycle, a wait time (t_{RCV}) is required after CE goes LOW.

Note that activating a read cycle when no valid data is present will cause incorrect operation. All bits must be valid data bits.

Supply Voltage Detection

The supply voltage detector tests the level of the supply voltage once every 0.5 seconds. If the supply voltage falls below the detector threshold, the FDT bit is set to 1. The FDT bit is reset to 0 after a data

read cycle that contains at least 56 data bits. The FDT bit is not reset for data read cycles of 55 bits or less.



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