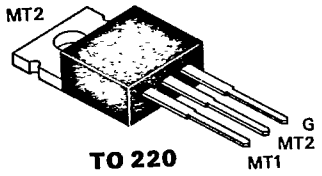
TAG SEMICONDUCTORS LTD

T1013BH – T1013NH TRIACS

10.0 A 200–800 V
50/50/50/75 mA



TO 220

The T1013 series of TRIAC's are high performance glass passivated PNPN devices. These parts are intended for general purpose applications where high gate insensitivity is required.

Absolute Maximum Ratings

$T_A = 25\,°C$ unless otherwise noted

Parameter	Part Nr.	Symbol	Min.	Max.	Unit	Test Conditions
Repetitive Peak Off State Voltage	**T1013BH**	V_{DRM}	200		V	
	T1013DH		400		V	$T_j = -40\,°C$ to $125\,°C$, $R_{GK} = 1\,K\Omega$
	T1013MH		600		V	
	T1013NH		800		V	
On-State Current		$I_{T(RMS)}$	10		A	All Conduction Angles $T_C = 85\,°C$
Nonrept. On-State Current		I_{TSM}	110		A	Half Cycle, 60 Hz
Nonrept. On-State Current		I_{TSM}	100		A	Half Cycle, 50 Hz
Fusing Current		I^2t	50		A^2s	t = 10 ms
Peak Gate Current		I_{GM}	4		A	10µs max.
Peak Gate Dissipation		P_{GM}	10		W	10µs max.
Gate Dissipation		$P_{G(AV)}$	1		W	20 ms max.
Operating Temperature		T_j	–40	125	°C	
Storage Temperature		T_{stg}	–40	125	°C	
Soldering Temperature		T_{sld}		250	°C	1.6 mm from case, 10 s max.

Electrical Characteristics

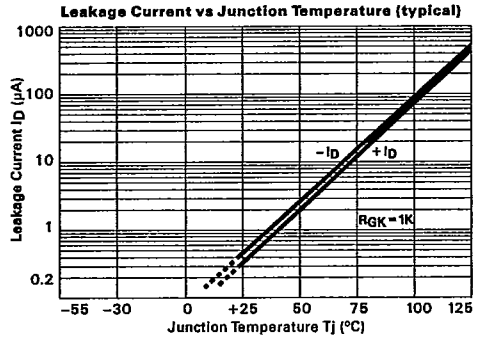
$T_A = 25\,°C$ unless otherwise noted

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Off-State Leakage Current	I_{DRM}		2	mA	$V_D = V_{DRM}$ $R_{GK} = 1\,K\Omega$ $T_j = 125\,°C$
Off-State Leakage Current	I_{DRM}		10	µA	$V_D = V_{DRM}$ $R_{GK} = 1\,K\Omega$ $T_j = 25\,°C$
On-State Voltage	V_T		1.75	V	at $I_T = 15$ A, $T_j = 25\,°C$
On-State Threshold Voltage	$V_{T(TO)}$		1.05	V	$T_j = 125\,°C$
On-State Slope Resistance	r_T		52	mΩ	$T_j = 125\,°C$
Gate Trigger Current	I_{GT} I+ (1)		50	mA	$V_D = 12$ V
	I_{GT} I– (2)		50	mA	$V_D = 12$ V
	I_{GT} III– (3)		50	mA	$V_D = 12$ V
	I_{GT} III+ (4)		75	mA	$V_D = 12$ V
Gate Trigger Voltage	V_{GT}		2.5	V	$V_D = 12$ V All Quadrants
Holding Current	I_H		75	mA	$R_{GK} = 1\,K\Omega$
Critical Rate of Voltage Rise	dv/dt	500		V/µs	$V_D = .67 \times V_{DRM}$ $R_{GK} = 1\,K\Omega$ $T_j = 125\,°C$
Critical Rate of Rise, Off-State	dv/dt_c	5		V/µs	$I_T = 10$ A di/dt = 4.45 A/ms $T_C = 85\,°C$
Thermal Resistance junc. to case	$R_{\Theta jc}$		2.5	K/W	
Thermal Resistance junc. to amb.	$R_{\Theta ja}$		60	K/W	

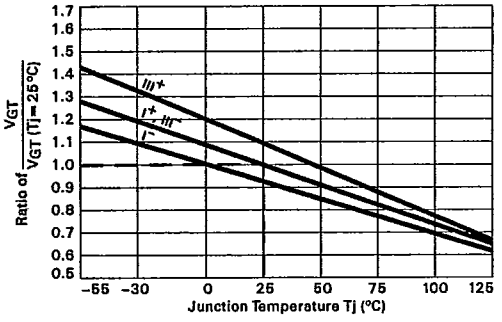
T10

Typical Characteristics
T10 – Chips

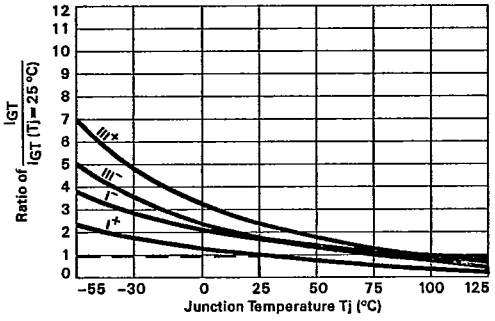
Leakage Current vs Junction Temperature (typical)



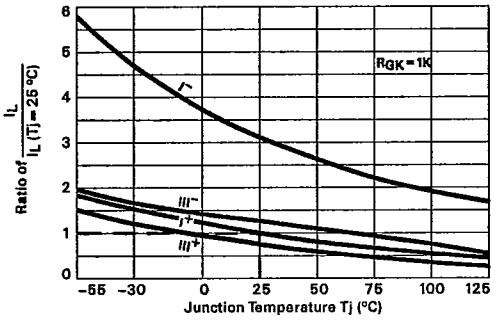
Normalized DC Gate Trigger Voltage vs Junction Temperature (typical)



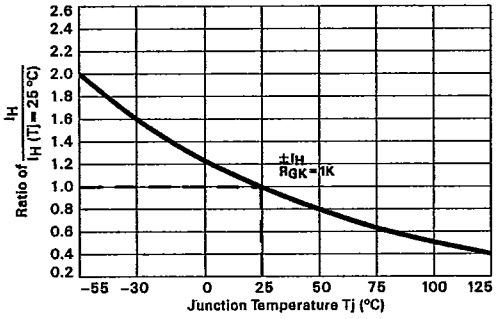
Normalized DC Gate Trigger Current vs Junction Temperature (typical)



Normalized DC Latching Current vs Junction Temperature (typical)



Normalized DC Holding Current vs Junction Temperature (typical)



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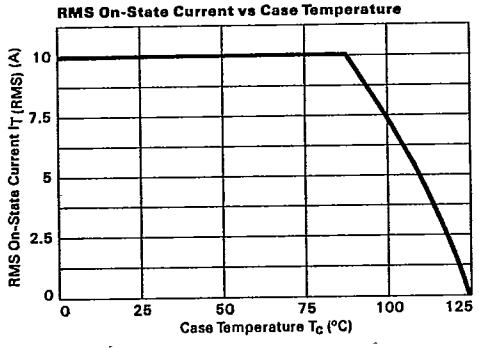
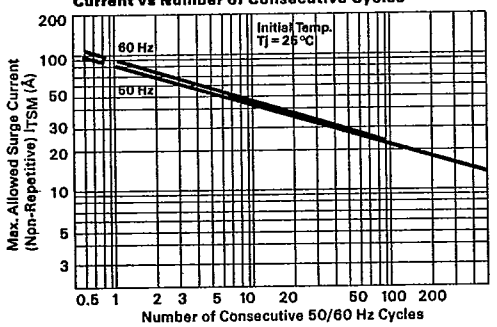
Typical Characteristics
T10 – Packaged Parts

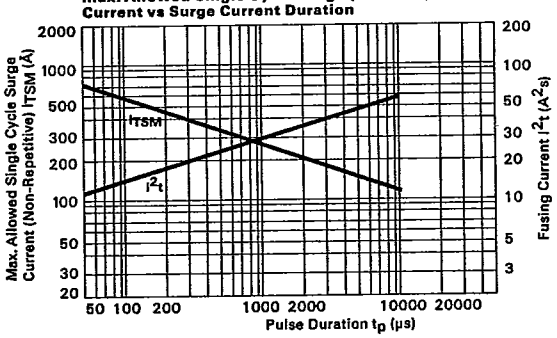
RMS On-State Current vs Case Temperature



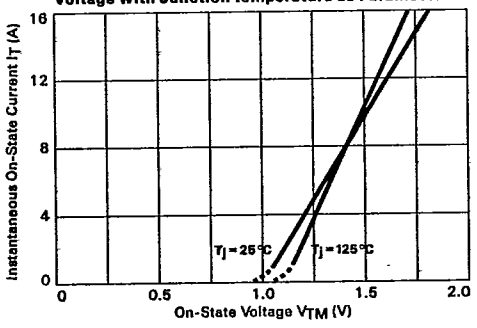
Max. Allowed Multi Cycle Surge (On-State) Current vs Number of Consecutive Cycles



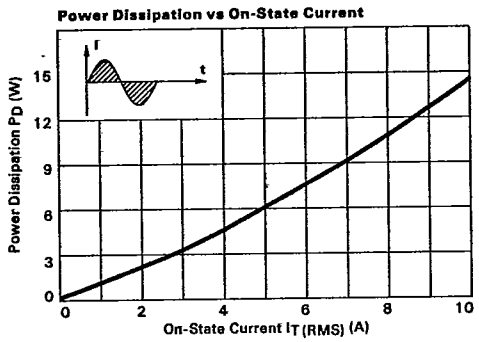
Max. Allowed Single Cycle Surge (On-State) Current vs Surge Current Duration



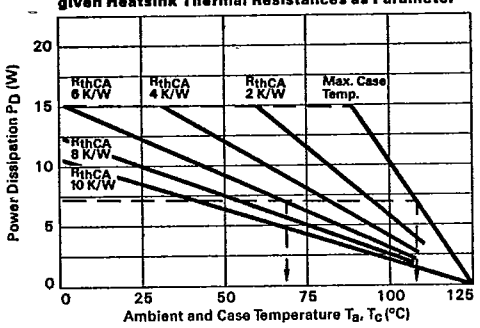
Instantaneous On-State Current vs On-State Voltage with Junction Temperature as Parameter



Power Dissipation vs On-State Current



Max. All. Power Dissip. vs Ambient Temp. with given Heatsink Thermal Resistances as Parameter



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