WM8771

24-bit, 192kHz 8-Channel Codec

DESCRIPTION

The WM8771 is a high performance, multi-channel audio codec. The WM8771 is ideal for surround sound processing applications for home hi-fi, automotive and other audio visual equipment.

A stereo 24-bit multi-bit sigma delta ADC is used with a three channel input selector. Each channel has analogue domain mute and programmable gain control. Digital audio output word lengths from 16-32 bits and sampling rates from 8kHz to 96kHz are supported.

Four stereo 24-bit multi-bit sigma delta DACs are used with oversampling digital interpolation filters. Digital audio input word lengths from 16-32 bits and sampling rates from 8kHz to 192kHz are supported. Each DAC channel has independent digital attenuation and mute control. The audio data interface supports I2S, left justified, right justified and DSP digital audio formats.

The device is controlled via a 3 wire serial interface. The interface provides access to all features including channel selection, volume controls, mutes, de-emphasis and power management facilities. The device is available in a 64-pin TQFP package.

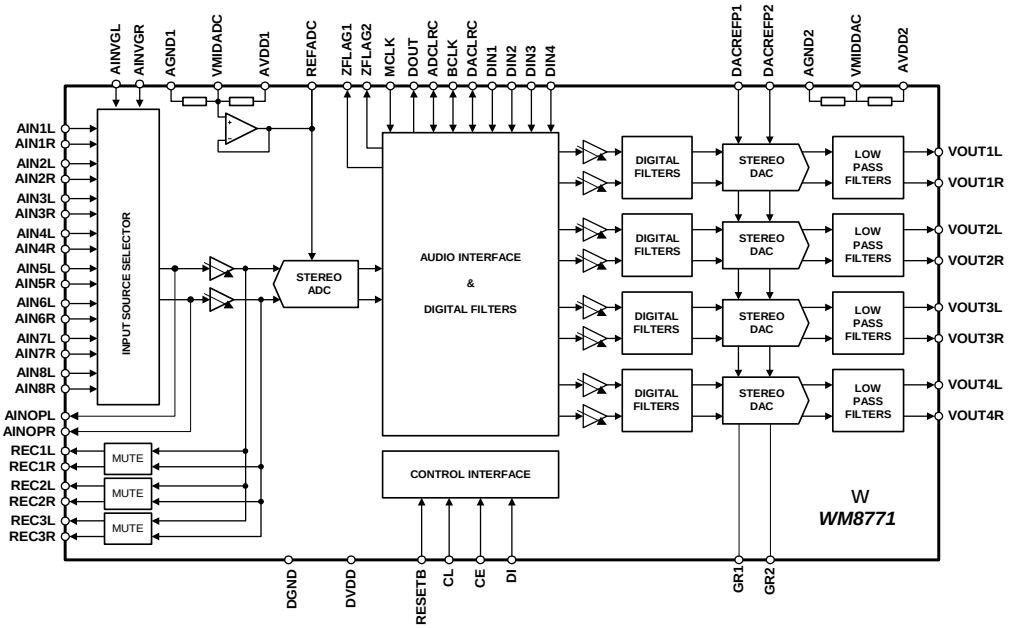
FEATURES

- Audio Performance
  - 108dB SNR ('A' weighted @ 48kHz) DAC
  - 97dB SNR ('A' weighted @ 48kHz) ADC
- DAC Sampling Frequency: 8kHz – 192kHz
- ADC Sampling Frequecncy: 8kHz – 96kHz
- 3-Wire SPI or CCB MPU Serial Control Interface
- Master or Slave Clocking Mode
- Programmable Audio Data Interface Modes
  - I^2S, Left, Right Justified or DSP
  - 16/20/24/32 bit Word Lengths
- Four Independent Stereo DAC Audio Outputs
- Eight stereo ADC inputs with analogue gain adjust from +19dB to –12dB in 1dB steps
- 2.7V to 5.5V Analogue, 2.7V to 3.6V Digital supply Operation
- 5V tolerant digital inputs
- 64-Pin TQFP Package

APPLICATIONS

- Surround Sound Processors
- Automotive Audio

BLOCK DIAGRAM



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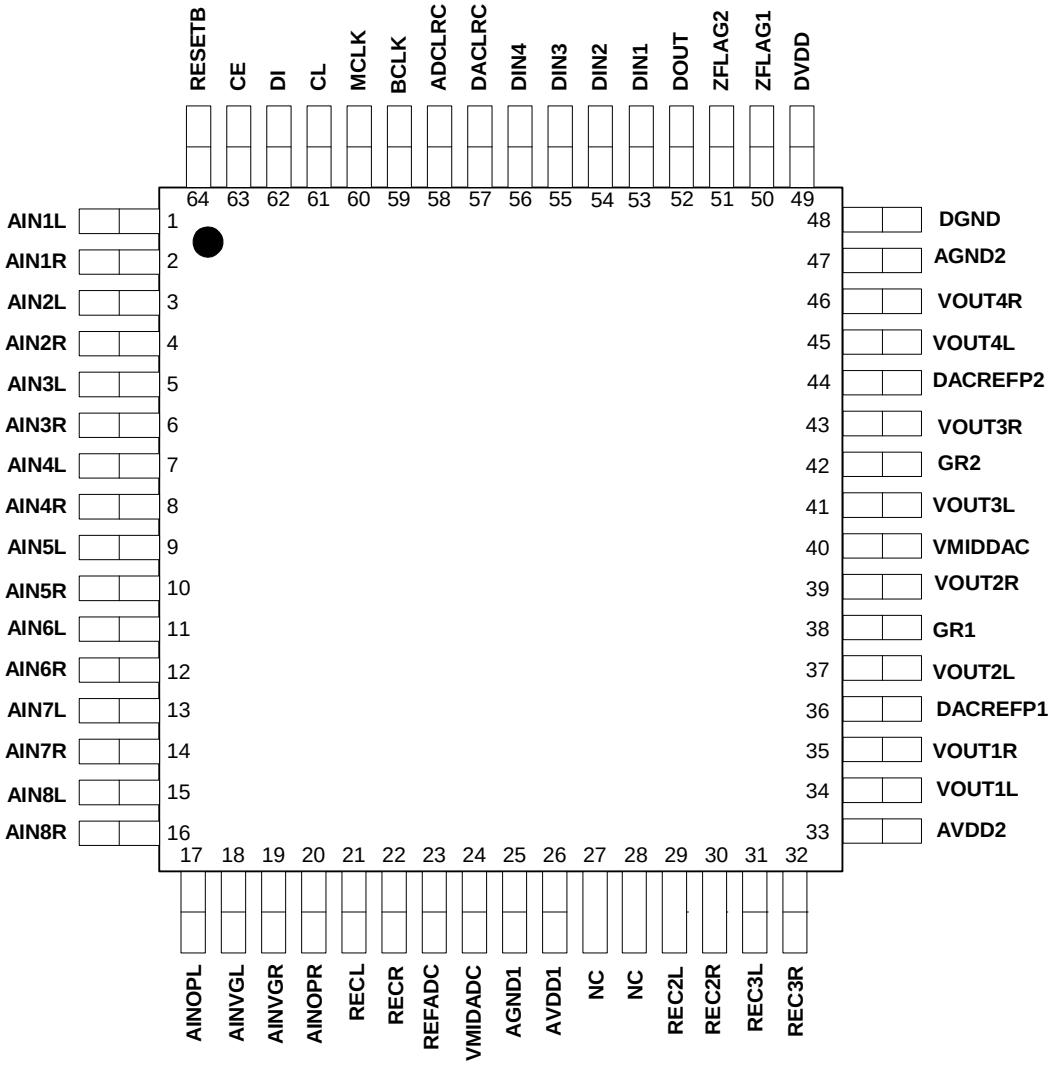
CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM8771IFT/V	-40 to + 85°C	64-pin TQFP

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AIN1L	Analogue Input	Channel 1 left input multiplexor virtual ground
2	AIN1R	Analogue Input	Channel 1 right input multiplexor virtual ground
3	AIN2L	Analogue Input	Channel 2 left input multiplexor virtual ground
4	AIN2R	Analogue Input	Channel 2 right input multiplexor virtual ground
5	AIN3L	Analogue Input	Channel 3 left input multiplexor virtual ground
6	AIN3R	Analogue Input	Channel 3 right input multiplexor virtual ground
7	AIN4L	Analogue Input	Channel 4 left input multiplexor virtual ground
8	AIN4R	Analogue Input	Channel 4 right input multiplexor virtual ground
9	AIN5L	Analogue Input	Channel 5 left input multiplexor virtual ground
10	AIN5R	Analogue Input	Channel 5 right input multiplexor virtual ground
11	AIN6L	Analogue Input	Channel 6 left input multiplexor virtual ground
12	AIN6R	Analogue Input	Channel 6 right input multiplexor virtual ground
13	AIN7L	Analogue Input	Channel 7 left input multiplexor virtual ground
14	AIN7R	Analogue Input	Channel 7 right input multiplexor virtual ground
15	AIN8L	Analogue Input	Channel 8 left input multiplexor virtual ground
16	AIN8R	Analogue Input	Channel 8 right input multiplexor virtual ground
17	AINOPL	Analogue Output	Left channel multiplexor output
18	AINVGL	Analogue Input	Left channel multiplexor virtual ground
19	AINVGR	Analogue Input	Right channel multiplexor virtual ground
20	AINOPR	Analogue Output	Right channel multiplexor output
21	REC1L	Analogue Output	Left channel input mux select output 1
22	REC1R	Analogue Output	Right channel input mux select output 1
23	REFADC	Analogue Output	ADC reference buffer decoupling pin; 10uF external decoupling
24	VMIDADC	Analogue Output	ADC midrail divider decoupling pin; 10uF external decoupling
25	AGND1	Supply	Analogue negative supply and substrate connection
26	AVDD1	Supply	Analogue positive supply
27	NC	No Connect	
28	NC	No Connect	
29	REC2L	Analogue Output	Left channel input mux select output 2
30	REC2R	Analogue Output	Right channel input mux select output 2
31	REC3L	Analogue Output	Left channel input mux select output 3
32	REC3R	Analogue Output	Right channel input mux select output 3
33	AVDD2	Supply	Analogue positive supply
34	VOUT1L	Analogue output	DAC channel 1 left output
35	VOUT1R	Analogue output	DAC channel 1 right output
36	DACREFP1	Supply	DAC positive reference supply
37	VOUT2L	Analogue output	DAC channel 2 left output
38	GR1	Supply	DAC ground reference
39	VOUT2R	Analogue output	DAC channel 2 right output
40	VMIDDAC	Analogue output	DAC midrail decoupling pin ; 10uF external decoupling
41	VOUT3L	Analogue output	DAC channel 3 left output
42	GR2	Supply	DAC ground reference
43	VOUT3R	Analogue output	DAC channel 3 right output
44	DACREFP2	Supply	DAC positive reference supply
45	VOUT4L	Analogue output	DAC channel 4 left output
46	VOUT4R	Analogue output	DAC channel 4 right output
47	AGND2	Supply	Analogue negative supply and substrate connection
48	DGND	Supply	Digital negative supply
49	DVDD	Supply	Digital positive supply
50	ZFLAG1	Digital output	DAC Zero Flag output
51	ZFLAG2	Digital output	DAC Zero Flag output

PIN	NAME	TYPE	DESCRIPTION
52	DOUT	Digital output	ADC data output
53	DIN1	Digital Input	DAC channel 1 data input
54	DIN2	Digital Input	DAC channel 2 data input
55	DIN3	Digital Input	DAC channel 3 data input
56	DIN4	Digital Input	DAC channel 4 data input
57	DACLRC	Digital input/output	DAC left/right word clock
58	ADCLRC	Digital input/output	ADC left/right word clock
59	BCLK	Digital input/output	ADC and DAC audio interface bit clock
60	MCLK	Digital input	Master DAC and ADC clock; 256, 384, 512 or 768fs (fs = word clock frequency)
61	SCLK	Digital input	Serial interface clock (5V tolerant)
62	SDIN	Digital input	Serial interface data (5V tolerant)
63	LATCH	Digital input	Serial interface Latch signal (5V tolerant)
64	RESETB	Digital input	Device reset input (mutes DAC outputs, resets gain stages to 0dB) (5V tolerant)

Note: Digital input pins have Schmitt trigger input buffers and are 5V tolerant.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+3.63V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs (DI, CL, CE & RESETB)	DGND -0.3V	+7V
Voltage range digital inputs (MCLK, DIN[3:0], ADCLRC, DACLRC & BCLK)	DGND -0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Master Clock Frequency		37MHz
Operating temperature range, T_A	-40°C	+85°C
Storage temperature	-65°C	+150°C
Package body temperature (soldering 10 seconds)		+240°C
Package body temperature (soldering 2 minutes)		+183°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		2.7		3.6	V
Analogue supply range	AVDD		2.7		5.5	V
Ground	AGND, DGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V

Note: digital supply DVDD must never be more than 0.3V greater than AVDD.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (TTL Levels)						
Input LOW level	V_{IL}				0.8	V
Input HIGH level	V_{IH}		2.0			V
Output LOW	V_{OL}	I_{OL}=1mA			0.1 x VDD	V
Output HIGH	V_{OH}	I_{OH}=1mA	0.9 x VDD			V
Analogue Reference Levels						
Reference voltage	V_{VMID}		AVDD/2 – 50mV	AVDD/2	AVDD/2 + 50mV	V
Potential divider resistance	R_{VMID}	AVDD to VMID and VMID to AGND	40k	50k	60k	Ohms
DAC Performance (Load = 10k ohms, 50pF)						
0dBFs Full scale output voltage				1.0 x AVDD/5		Vrms
SNR (Note 1,2)		A-weighted, @ fs = 48kHz	104	108		dB
SNR (Note 1,2)		A-weighted @ fs = 96kHz		108		dB
Dynamic Range (Note 2)	DNR	A-weighted, -60dB full scale input	104	108		dB
Total Harmonic Distortion (THD)		1kHz, 0dBFs		-97	-90	dB
DAC channel separation				100		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
ADC Performance						
Input Signal Level (0dB)				1.0 x AVDD/5		Vrms
SNR (Note 1,2)		A-weighted, 0dB gain @ fs = 48kHz	93	97		dB
SNR (Note 1,2)		A-weighted, 0dB gain @ fs = 96kHz		94		dB
Dynamic Range (Note 2)		A-weighted, -60dB full scale input		97		dB
Total Harmonic Distortion (THD)		kHz, 0dBFs		-90	-87	dB
		1kHz, -3dBFs		-95	-90	dB
ADC Channel Separation		1kHz Input		90		dB

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Programmable Gain Step Size			0.5	1.0	1.5	dB
Programmable Gain Range		1kHz Input	-12	0	+19	dB
Mute Attenuation		1kHz Input, 0dB gain		97		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Supply Current						
Analogue supply current		AVDD = 5V		100		mA
Digital supply current		DVDD = 3.3V		20		mA

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
6. Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

MASTER CLOCK TIMING

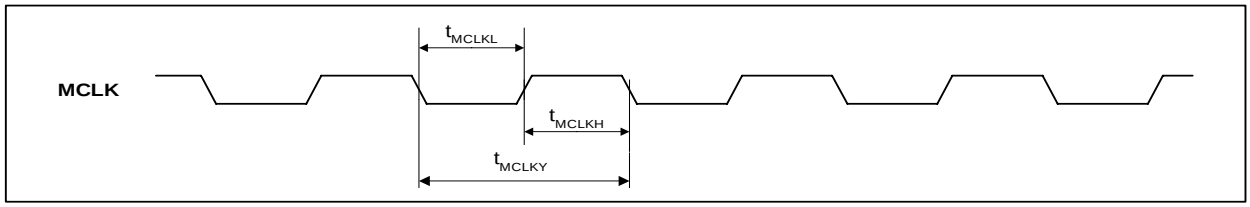


Figure 1 Master Clock Timing Requirements

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK System clock pulse width high	t_{MCLKH}		11			ns
MCLK System clock pulse width low	t_{MCLKL}		11			ns
MCLK System clock cycle time	t_{MCLKY}		28			ns
MCLK Duty cycle			40:60		60:40	

Table 1 Master Clock Timing Requirements

DIGITAL AUDIO INTERFACE – MASTER MODE

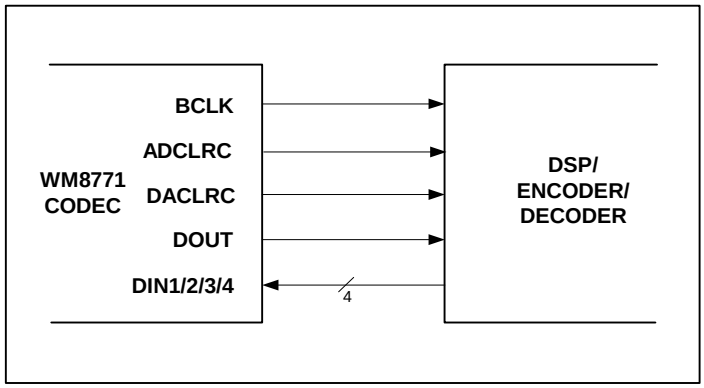


Figure 2 Audio Interface - Master Mode

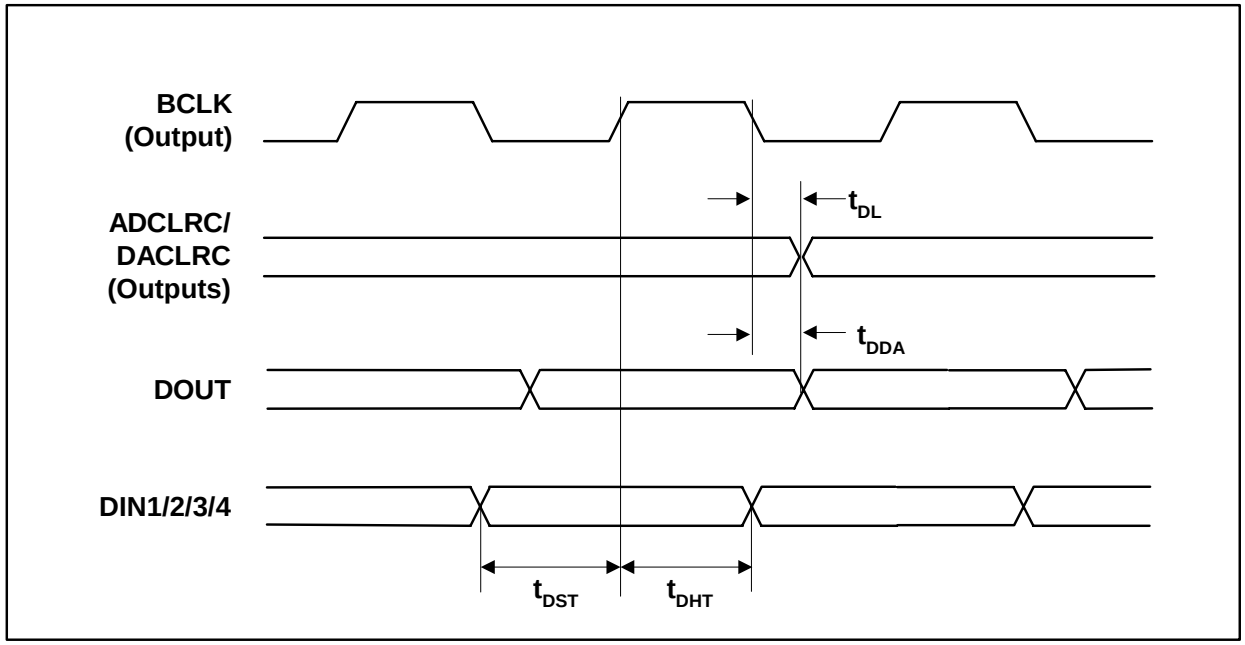


Figure 3 Digital Audio Data Timing – Master Mode

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, T_A = +25°C, Master Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
ADCLRC/DACLRC propagation delay from BCLK falling edge	t_{DL}		0		10	ns
DOUT propagation delay from BCLK falling edge	t_{DDA}		0		10	ns
DIN1/2/3/4 setup time to BCLCK rising edge	t_{DST}		10			ns
DIN1/2/3/4 hold time from BCLK rising edge	t_{DHT}		10			ns

Table 2 Digital Audio Data Timing – Master Mode

DIGITAL AUDIO INTERFACE – SLAVE MODE

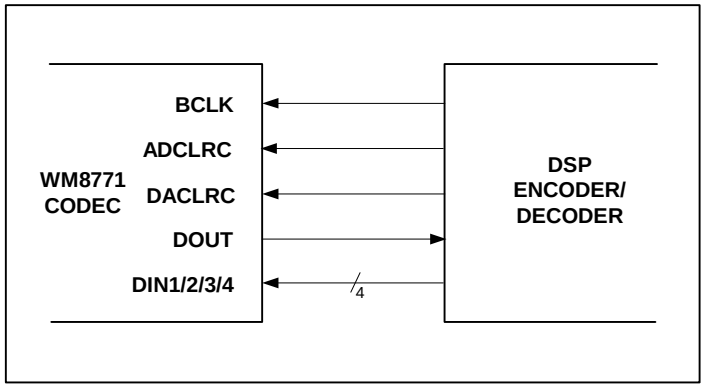


Figure 4 Audio Interface – Slave Mode

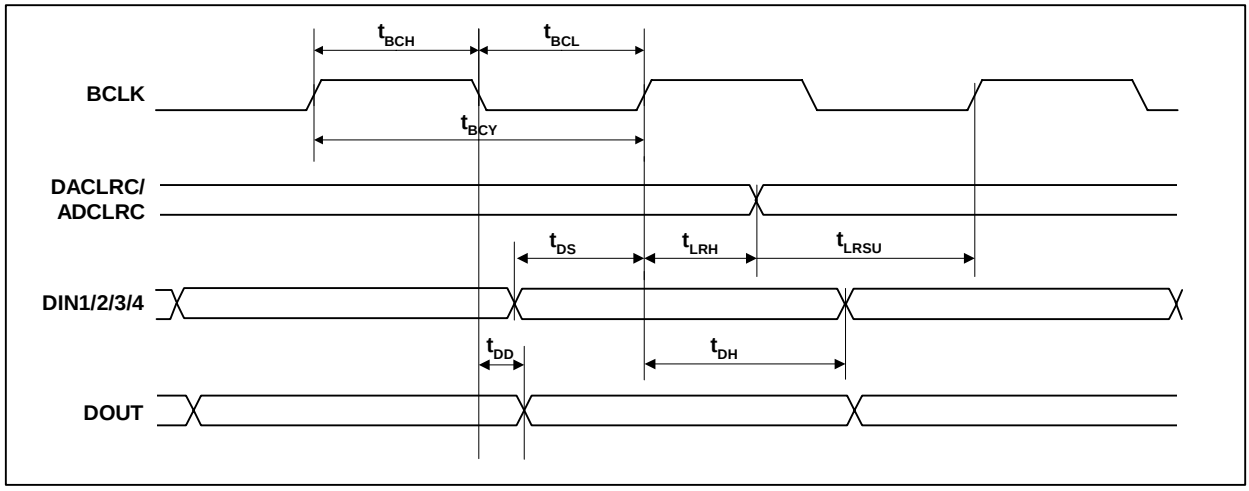


Figure 5 Digital Audio Data Timing – Slave Mode

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCLK cycle time	t_{BCY}		50			ns
BCLK pulse width high	t_{BCH}		20			ns
BCLK pulse width low	t_{BCL}		20			ns
DACLRC/ADCLRC set-up time to BCLK rising edge	t_{LRSU}		10			ns
DACLRC/ADCLRC hold time from BCLK rising edge	t_{LRH}		10			ns
DIN1/2/3/4 set-up time to BCLK rising edge	t_{DS}		10			ns
DIN1/2/3/4 hold time from BCLK rising edge	t_{DH}		10			ns
DOUT propagation delay from BCLK falling edge	t_{DD}		0		10	ns

Table 3 Digital Audio Data Timing – Slave Mode

Note: ADCLRC and DACLRC should be synchronous with MCLK, although the WM8771 interface is tolerant of phase variations or jitter on these signals.

MPU INTERFACE TIMING

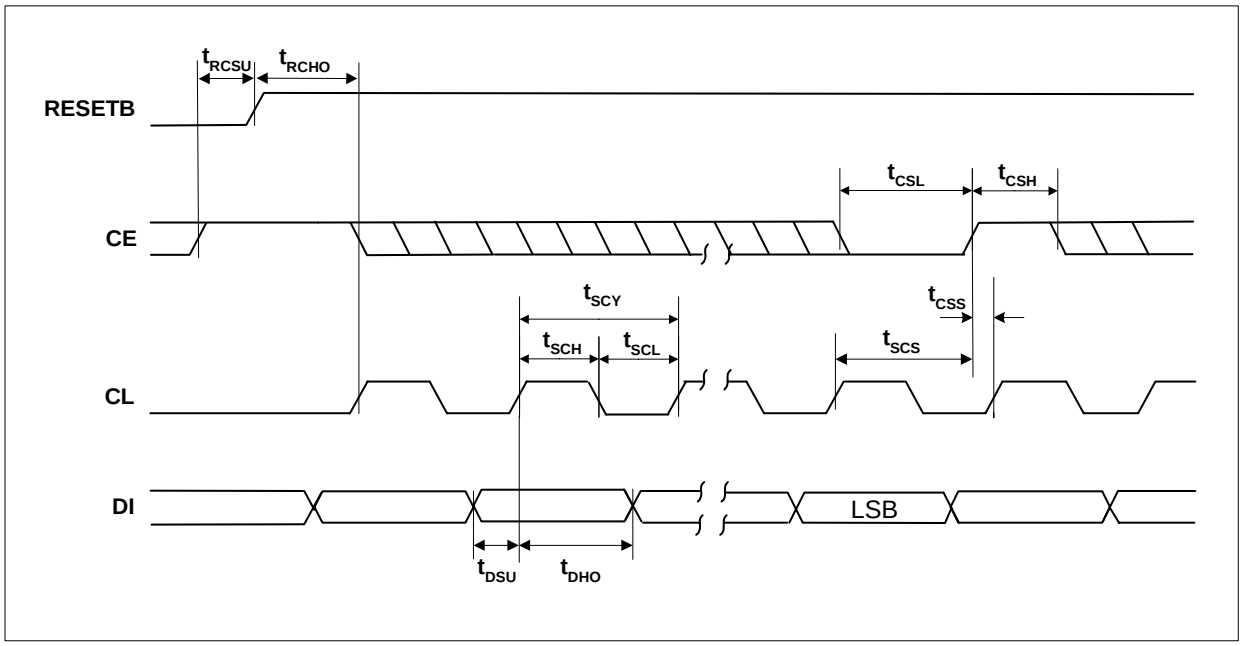


Figure 6 SPI compatible Control Interface Input Timing

Test Conditions AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated					
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
CE to RESETB hold time	t_{RCSU}	20			ns
RESETB to CL setup time	t_{RCHO}	20			ns
CL rising edge to CE rising edge	t_{SCS}	60			ns
CL pulse cycle time	t_{SCY}	80			ns
CL pulse width low	t_{SCL}	30			ns
CL pulse width high	t_{SCH}	30			ns
DI to CL set-up time	t_{DSU}	20			ns
CL to DI hold time	t_{DHO}	20			ns
CE pulse width low	t_{CSL}	20			ns
CE pulse width high	t_{CSH}	20			ns
CE rising to CL rising	t_{CSS}	20			ns

Table 4 3 wire SPI compatible Control Interface Input Timing Information

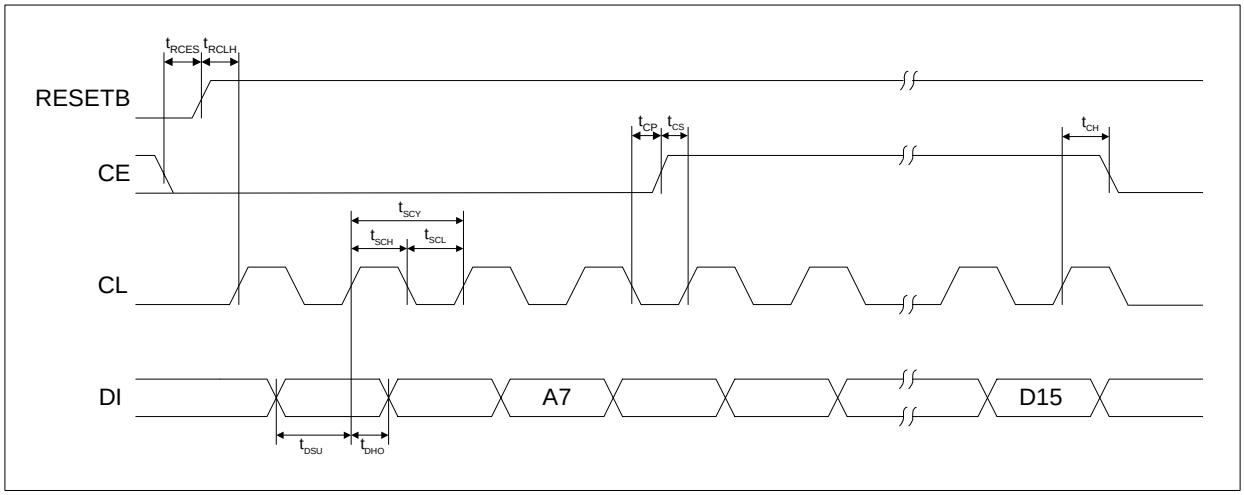


Figure 7 3 wire CCB compatible Interface Input Timing Information – CL stopped low

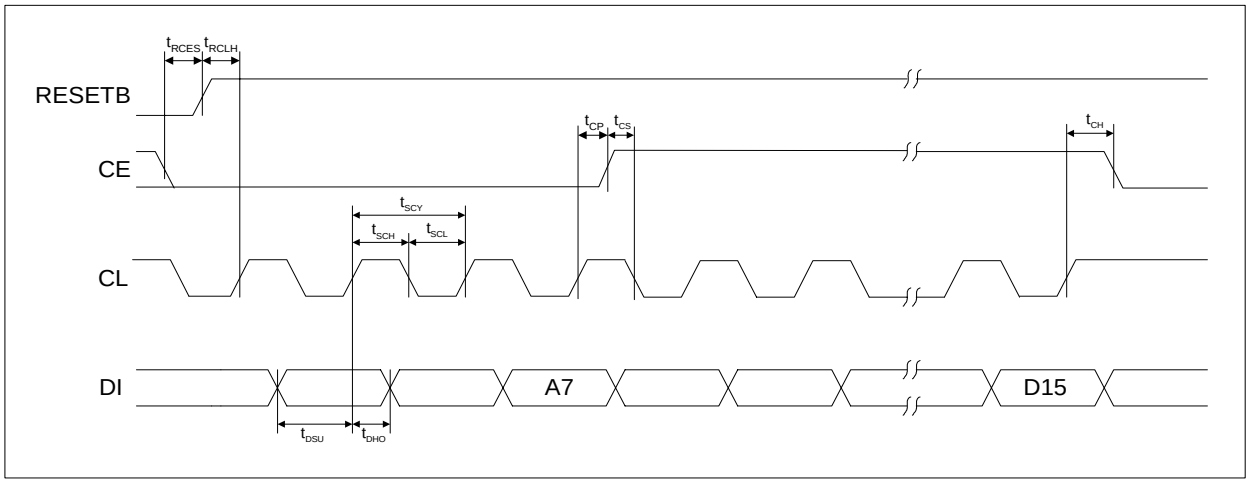


Figure 8 3 wire CCB compatible Interface Input Timing Information – CL stopped high

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CE to RESETB setup time	t_{RCES}	20			ns
RESETB to CL hold time	t_{RCLH}	20			ns
DI to CL setup time	t_{DSU}	20			ns
CL to DI hold time	t_{DHO}	20			ns
CL to CE setup time	t_{CS}	20			ns
CE to CL wait time	t_{CP}	20			ns
CL to CE hold time	t_{CH}	20			ns
CL pulse width high	t_{SCH}	30			ns
CL pulse width low	t_{SCL}	30			ns
CL pulse cycle time	t_{SCY}	80			ns

Table 5 3 wire CCB compatible Interface Input Timing Information

DEVICE DESCRIPTION

INTRODUCTION

WM8771 is a complete 8-channel DAC, 2-channel ADC audio codec, including digital interpolation and decimation filters, multi-bit sigma delta stereo ADC, and switched capacitor multi-bit sigma delta DACs with digital volume controls on each channel and output smoothing filters.

The device is implemented as four separate stereo DACs and a stereo ADC with flexible input multiplexor, in a single package and controlled by a single interface.

The four stereo channels may either be used to implement a 5.1 channel surround system, with additional stereo channel for a stereo mix down channel, or for a complete 7.1 channel surround system.

Each stereo DAC has its own data input DIN1/2/3/4. DAC word clock DACLRC is shared between them. The stereo ADC has it's own data output DOUT, and word clock ADCLRC. BITCLK and MCLK are shared between the ADCs and DACs. The Audio Interface may be configured to operate in either master or slave mode. In Slave mode ADCLRC, DACLRC and BCLK are all inputs. In Master mode ADCLRC, DACLRC and BCLK are all outputs.

The input multiplexor to the ADC is configured to allow large signal levels to be input to the ADC, using external resistors to reduce the amplitude of larger signals to within the normal operating range of the ADC. The ADC input PGA also allows input signals to be gained up to +19dB and attenuated down to -12dB. This allows the user maximum flexibility in the use of the ADC.

Three individually selectable stereo record outputs are also provided on REC1/2/3. It is intended that the REC1/2/3 outputs are only used to drive high impedance buffers.

Each DAC has its own digital volume control. In addition a zero cross detect circuit is provided for each DAC. The digital volume control detects a transition through the zero point before updating the volume. This minimises audible clicks and 'zipper' noise as the gain values change.

Control of internal functionality of the device is by 3-wire serial control interface. An SPI or CCB type interface may used, selectable by the state of the CE pin on the rising edge of RESETB. The control interface may be asynchronous to the audio data interface as control data will be re-synchronised to the audio processing internally.

Operation using system clock of 128fs, 192fs, 256fs, 384fs, 512fs or 768fs is provided. In Slave mode selection between clock rates is automatically controlled. In master mode the master clock to sample rate ratio is set by control bits ADCRATE and DACRATE. ADC and DAC may run at different rates within the constraint of a common master clock for the ADC and DACs. For example with master clock at 24.576MHz, a DAC sample rate of 96kHz (256fs mode) and an ADC sample rate of 48kHz (512fs mode) can be accommodated. Master clock sample rates (fs) from less than 8ks/s up to 192ks/s are allowed, provided the appropriate system clock is input.

The audio data interface supports right, left and I^2S interface formats along with a highly flexible DSP serial port interface.

AUDIO DATA SAMPLING RATES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master system clock can be applied directly through the MCLK input pin with no software configuration necessary. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the ADC and DAC.

The master clock for WM8771 supports audio sampling rates from 128fs to 768fs, where fs is the audio sampling frequency (DACLRC or ADCLRC) typically 32kHz, 44.1kHz, 48kHz, 96kHz or 192kHz (for DAC operation only). The master clock is used to operate the digital filters and the noise shaping circuits.

In Slave mode the WM8771 has a master clock detection circuit that automatically determines the relationship between the system clock frequency and the sampling rate (to within +/- 32 system clocks). If there is a greater than 32 clocks error the interface is disabled and maintains the output level at the last sample. The master clock must be synchronised with ADCLRC/DACLRC, although the WM8771 is tolerant of phase variations or jitter on this clock.

SAMPLING RATE (DACLRC/ ADCLRC)	System Clock Frequency (MHz)					
	128fs	192fs	256fs	384fs	512fs	768fs
32kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1kHz	5.6448	8.467	11.2896	16.9340	22.5792	33.8688
48kHz	6.114	9.216	12.288	18.432	24.576	36.864
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable

Table 6 System Clock Frequencies Versus Sampling Rate

In Master mode BCLK, DACLRC and ADCLRC are generated by the WM8771. The frequencies of ADCLRC and DACLRC are set by setting the required ratio of MCLK to DACLRC and ADCLRC using the DACRATE and ADCRATE control bits (Table 7).

ADCRATE[2:0]/ DACRATE[2:0]	MCLK:ADCLRC/DACLRC RATIO
000	128fs
001	192fs
010	256fs
011	384fs
100	512fs
101	768fs

Table 7 Master Mode MCLK:ADCLRC/DACLRC ratio select

SAMPLING RATE (DACLRC/ ADCLRC)	System Clock Frequency (MHz)					
	128fs	192fs	256fs	384fs	512fs	768fs
	ADCRATE/ DACRATE =000	ADCRATE/ DACRATE =001	ADCRATE/ DACRATE =010	ADCRATE/ DACRATE =011	ADCRATE/ DACRATE =100	ADCRATE/ DACRATE =101
32kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1kHz	5.6448	8.467	11.2896	16.9340	22.5792	33.8688
48kHz	6.114	9.216	12.288	18.432	24.576	36.864
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable

Table 8 Master Mode ADC/DACLRC frequency selection

BCLK is also generated by the WM8771. The frequency of BCLK depends on the mode of operation.

In 128/192fs modes (ADCRATE/DACRATE=000 or 001) BCLK = MCLK/2. In 256/384/512fs modes (ADCRATE/DACRATE=010 or 011 or 100) BCLK = MCLK/4. However if DSP mode is selected as the audio interface mode then BCLK=MCLK. This is to ensure that there are sufficient BCLKs to clock in all eight channels. Note that DSP mode cannot be used in 128fs mode for word lengths greater than 16 bits or in 192fs mode for word lengths greater than 24 bits.

ZERO DETECT

The WM8770 has a zero detect circuit for each DAC channel which detects when 1024 consecutive zero samples have been input. Two zero flag outputs (ZFLAG1 and ZFLAG2) may be programmed to output the zero detect signals (see Table 9) which may then be used to control external muting circuits. A '1' on ZFLAG1 or ZFLAG2 indicates a zero detect. The zero detect may also be used to automatically enable the PGA mute by setting IZD. The zero flag output may be disabled by setting DZFM to 0000. The zero flag signal for a DAC channel will only be enabled if that channel is enabled as an input to the output summing stage.

DZFM[3:0]	ZFLAG1	ZFLAG2
0000	Zero flag disabled	Zero flag disabled
0001	All channels zero	All channels zero
0010	Left channels zero	Right channels zero
0011	Channel 1 zero	Channels 2-4 zero
0100	Channel 1 zero	Channel 2 zero
0101	Channel 1 zero	Channel 3 zero
0110	Channel 1 zero	Channel 4 zero
0111	Channel 2 zero	Channel 3 zero
1000	Channel 2 zero	Channel 4 zero
1001	Channel 3 zero	Channel 4 zero
1010	Channels 1-3 zero	Channel 4 zero
1011	Channel 1 zero	Channels 2 & 3 zero
1100	Channel 1 left zero	Channel 1 right zero
1101	Channel 2 left zero	Channel 2 right zero
1110	Channel 3 left zero	Channel 3 right zero
1111	Channel 4 left zero	Channel 4 right zero

Table 9 Zero Flag Output Select

POWERDOWN MODES

The WM8771 has powerdown control bits allowing specific parts of the WM8771 to be powered off when not being used. The 8-channel input source selector and input buffer may be powered down using control bit AINPD. When AINPD is set all inputs to the source selector (AIN1l/R to AIN8L/R) are switched to a buffered VMIDADC. Control bit ADCPD powers off the ADC and also the ADC input PGAs. The four stereo DACs each have a separate powerdown control bit, DACPD[3:0] allowing individual stereo DACs to be powered off when not in use. The analogue output buffer may also be powered down by setting OUTPD[3:0]. OUTPD[3:0] also switches the analogue outputs VOUTL/R to VMIDDAC to maintain a dc level on the output. Setting AINPD, ADCPD, DACPD[3:0] and OUTPD[3:0] will powerdown everything except the references VMIDADC, ADCREF and VMIDDAC. These may be powered down by setting PDWN. Setting PDWN will override all other powerdown control bits. It is recommended that the 8-channel input mux and buffer, ADC, DAC and output buffers are powered down before setting PDWN. The default is for all powerdown bits to be set except PDWN.

DIGITAL AUDIO INTERFACE

MASTER AND SLAVE MODES

The audio interface operates in either Slave or Master mode, selectable using the MS control bit. In both Master and Slave modes DACDAT is always an input to the WM8771 and ADCDAT is always an output. The default is Slave mode.

In Slave mode (MS=0) ADCLRC, DACLRC and BCLK are inputs to the WM8771 (Figure 9). DIN1/2/3/4, ADCLRC and DACLRC are sampled by the WM8771 on the rising edge of BCLK. ADC data is output on DOUT and changes on the falling edge of BCLK. By setting control bit BCLKINV the polarity of BCLK may be reversed so that DIN1/2/3/4, ADCLRC and DACLRC are sampled on the falling edge of BCLK and DOUT changes on the rising edge of BCLK.

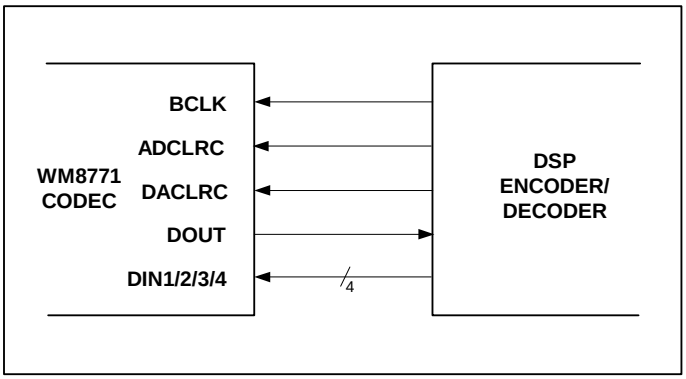


Figure 9 Slave Mode

In Master mode (MS=1) ADCLRC, DACLRC and BCLK are outputs from the WM8771 (Figure 10). ADCLRC, DACLRC and BITCLK are generated by the WM8771. DIN1/2/3/4 are sampled by the WM8771 on the rising edge of BCLK so the controller must output DAC data that changes on the falling edge of BCLK. ADCDAT is output on DOUT and changes on the falling edge of BCLK. By setting control bit BCLKINV the polarity of BCLK may be reversed so that DIN1/2/3/4 are sampled on the falling edge of BCLK and DOUT changes on the rising edge of BCLK.

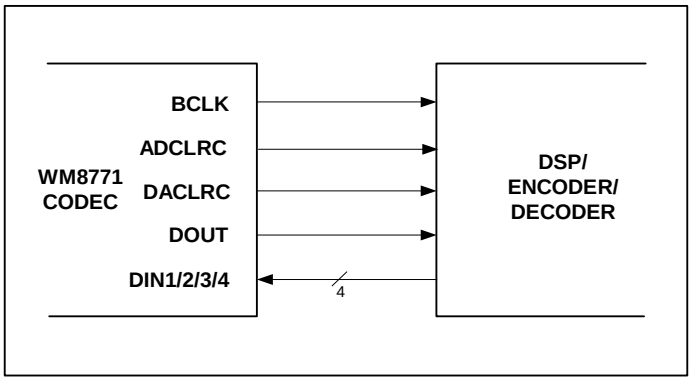


Figure 10 Master Mode

AUDIO INTERFACE FORMATS

Audio data is applied to the internal DAC filters, or output from the ADC filters, via the Digital Audio Interface. 5 popular interface formats are supported:

- Left Justified mode
- Right Justified mode
- I2S mode
- DSP Early mode
- DSP Late mode

All 5 formats send the MSB first and support word lengths of 16, 20, 24 and 32 bits, with the exception of 32 bit right justified mode, which is not supported.

In left justified, right justified and I2S modes, the digital audio interface receives DAC data on the DIN1/2/3/4 inputs and outputs ADC data on DOUT. Audio Data for each stereo channel is time multiplexed with ADCLRC/DACLRC indicating whether the left or right channel is present. ADCLRC/DACLRC is also used as a timing reference to indicate the beginning or end of the data words.

In left justified, right justified and I2S modes, the minimum number of BCLKs per DACLRC/ADCLRC period is 2 times the selected word length. ADCLRC/DACLRC must be high for a minimum of word length BCLKs and low for a minimum of word length BCLKs. Any mark to space ratio on ADCLRC/DACLRC is acceptable provided the above requirements are met.

In DSP early or DSP late mode, all 8 DAC channels are time multiplexed onto DIN1. DACLRC is used as a frame sync signal to identify the MSB of the first word. The minimum number of BCLKs per DACLRC period is 8 times the selected word length. Any mark to space ratio is acceptable on DACLRC provided the rising edge is correctly positioned. The ADC data may also be output in DSP early or late modes, with ADCLRC used as a frame sync to identify the MSB of the first word. The minimum number of BCLKs per ADCLRC period is 2 times the selected word length

LEFT JUSTIFIED MODE

In left justified mode, the MSB of DIN1/2/3/4 is sampled by the WM8771 on the first rising edge of BCLK following a DACLRC transition. The MSB of the ADC data is output on DOUT and changes on the same falling edge of BCLK as ADCLRC and may be sampled on the rising edge of BCLK. ADCLRC and DACLRC are high during the left samples and low during the right samples (Figure 11).

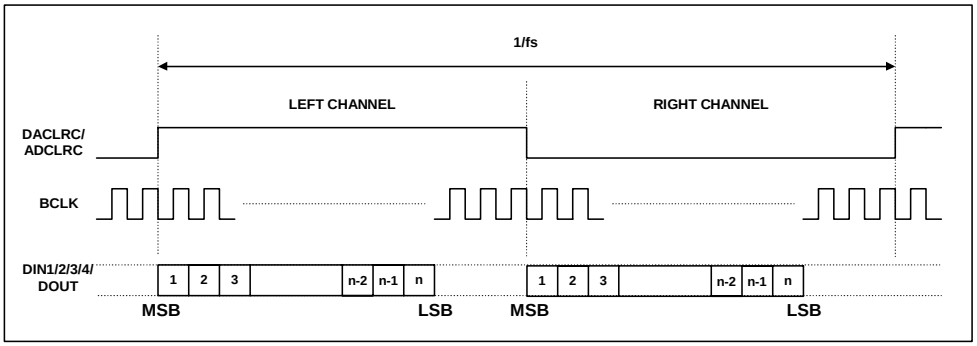


Figure 11 Left Justified Mode TIming Diagram

RIGHT JUSTIFIED MODE

In right justified mode, the LSB of DIN1/2/3/4 is sampled by the WM8771 on the rising edge of BCLK preceding a DACLRC transition. The LSB of the ADC data is output on DOUT and changes on the falling edge of BCLK preceding an ADCLRC transition and may be sampled on the rising edge of BCLK. ADCLRC and DACLRC are high during the left samples and low during the right samples (Figure 12).

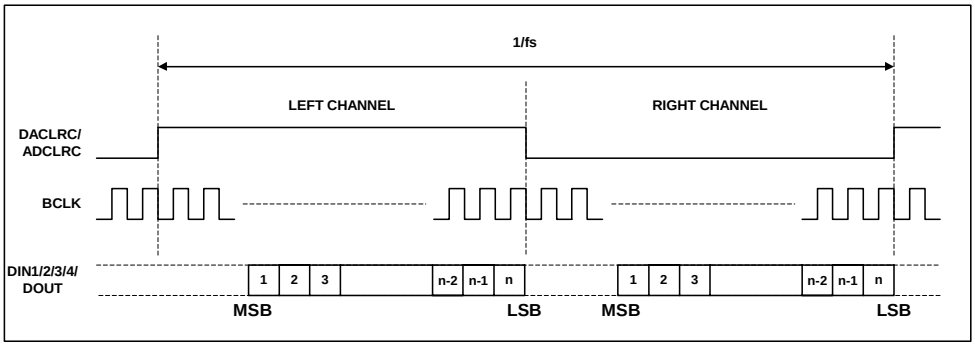


Figure 12 Right Justified Mode TIming Diagram

I2S MODE

In I2S mode, the MSB of DIN1/2/3/4 is sampled by the WM8771 on the second rising edge of BCLK following a DACLRC transition. The MSB of the ADC data is output on DOUT and changes on the first falling edge of BCLK following an ADCLRC transition and may be sampled on the rising edge of BCLK. ADCLRC and DACLRC are low during the left samples and high during the right samples.

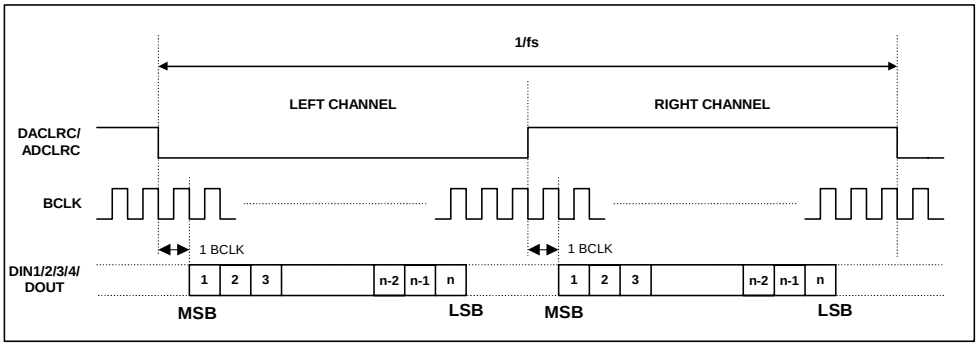


Figure 13 I2S Mode TIming Diagram

DSP EARLY MODE

In DSP early mode, the MSB of DAC channel 1 left data is sampled by the WM8771 on the second rising edge on BCLK following a DACLRC rising edge. DAC channel 1 right and DAC channels 2, 3 and 4 data follow DAC channel 1 left data (Figure 14).

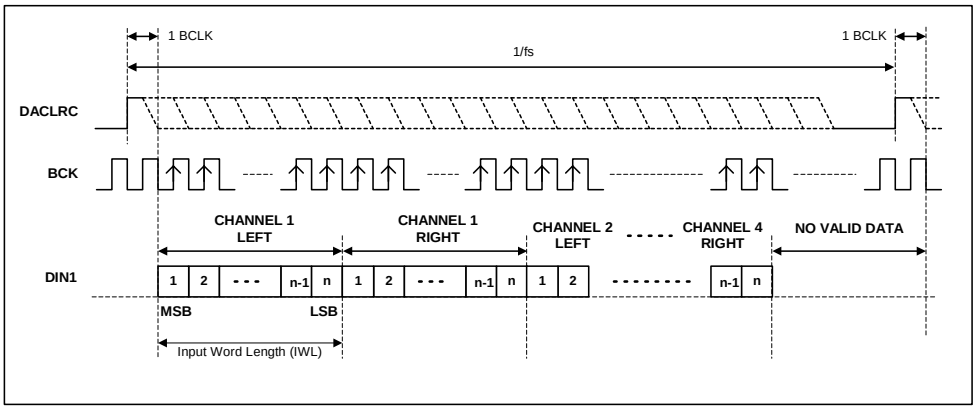


Figure 14 DSP Early Mode Timing Diagram – DAC data input

The MSB of the left channel ADC data is output on DOUT and changes on the first falling edge of BCLK following a low to high ADCLRC transition and may be sampled on the rising edge of BCLK. The right channel ADC data is contiguous with the left channel data (Figure 15)

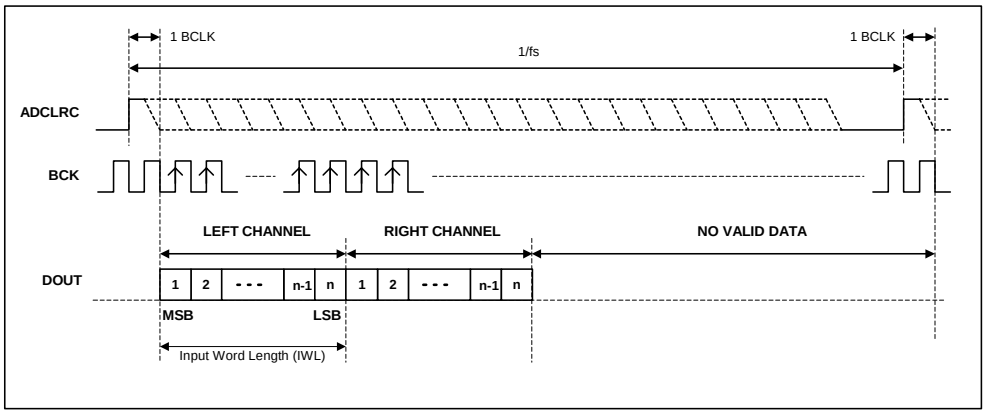


Figure 15 DSP Early Mode Timing Diagram – ADC data output

DSP LATE MODE

In DSP late mode, the MSB of DAC channel 1 left data is sampled by the WM8771 on the first BCLK rising edge following a DACLRC rising edge. DAC channel 1 right and DAC channels 2, 3 and 4 data follow DAC channel 1 left data (Figure 16).

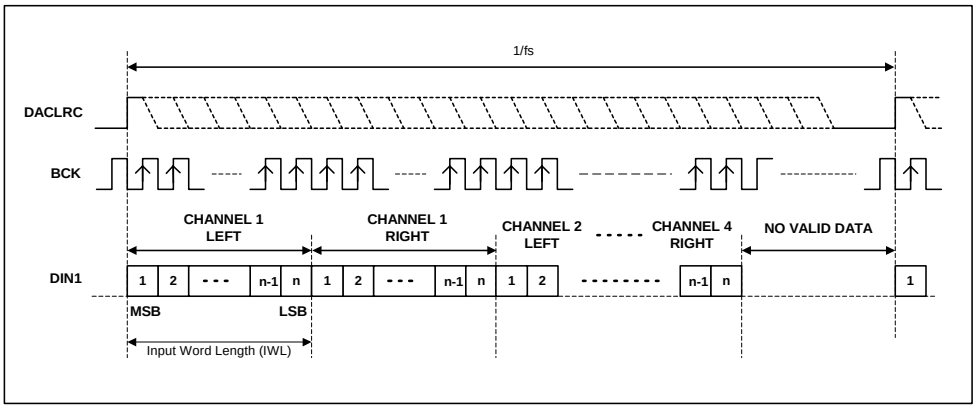


Figure 16 DSP Late Mode Timing Diagram – DAC data input

The MSB of the left channel ADC data is output on DOUT and changes on the same falling edge of BCLK as the low to high ADCLRC transition and may be sampled on the rising edge of BCLK. The right channel ADC data is contiguous with the left channel data (Figure 17).

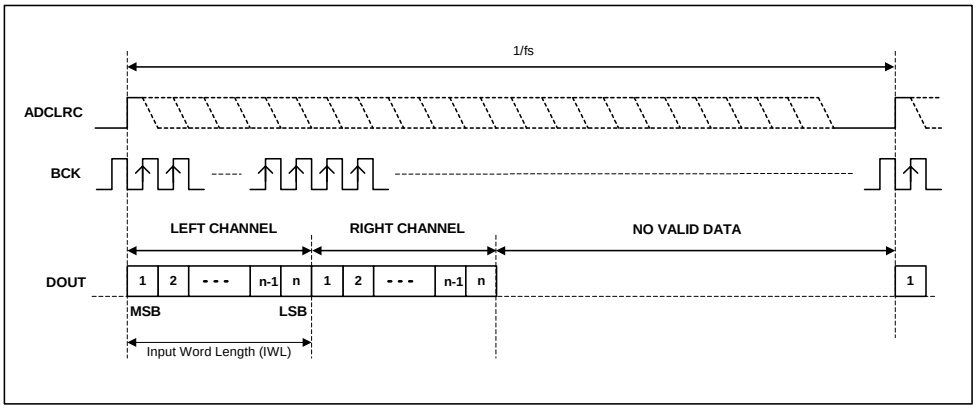


Figure 17 DSP Late Mode Timing Diagram – ADC data output

In both early and late DSP modes, DACL1 is always sent first, followed immediately by DACR1 and the data words for the other 6 channels. No BCLK edges are allowed between the data words. The word order is DAC1 left, DAC1 right, DAC2 left, DAC2 right, DAC3 left, DAC3 right, DAC4 left, DAC4 right.

CONTROL INTERFACE OPERATION

The WM8771 is controlled using a 3-wire serial interface in either an SPI compatible configuration or a CCB (Computer Control Bus) configuration.

The interface configuration is determined by the state of the CE pin on the rising edge of the RESETB pin. If the CE pin is low on the rising edge of RESETB, CCB configuration is selected. If CE is high on the rising edge of RESETB, SPI compatible configuration is selected.

The control interface is 5V tolerant, meaning that the control interface input signals CE, CL and DI may have an input high level of 5V while DVDD is 3V. Input thresholds are determined by DVDD. RESETB and DACMUTE are also 5V tolerant.

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE

DI is used for the program data, CL is used to clock in the program data and CE is used to latch the program data. DI is sampled on the rising edge of CL. The 3-wire interface protocol is shown in Figure 18.

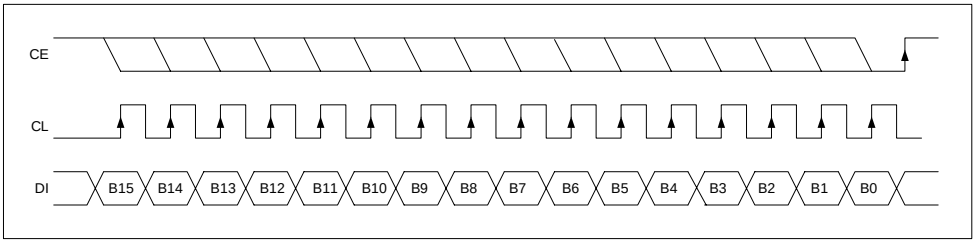


Figure 18 3-wire SPI compatible Interface

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits
3. CE is edge sensitive – the data is latched on the rising edge of CE.

CCB INTERFACE MODE

CCB Interface mode allows multiple devices to be controlled off a common 3-wire bus. Each device on the 3-wire bus has its own identifying address. The WM8771 supports write only CCB interface mode.

DI is used for the device address and program data and CL is used to clock in the address and data on DI. DI is sampled on the rising edge of CL. CE indicates whether the data on DI is the device address or program data. The eight clocks before a rising edge on CE will clock in the device address. The device address is latched on the rising edge of CE. The sixteen clocks before a falling edge on CE will clock in the program data. The program data is latched on the falling edge of CE.

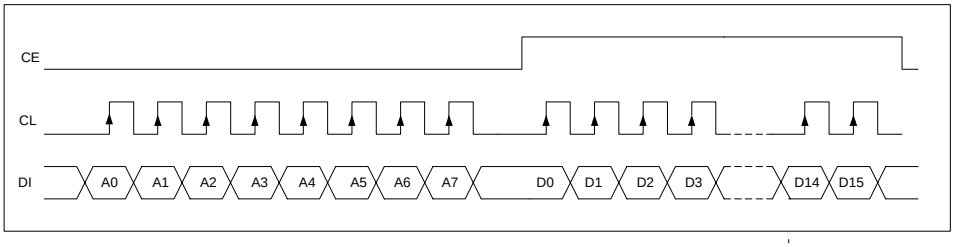


Figure 19 CCB Interface – CL stopped low

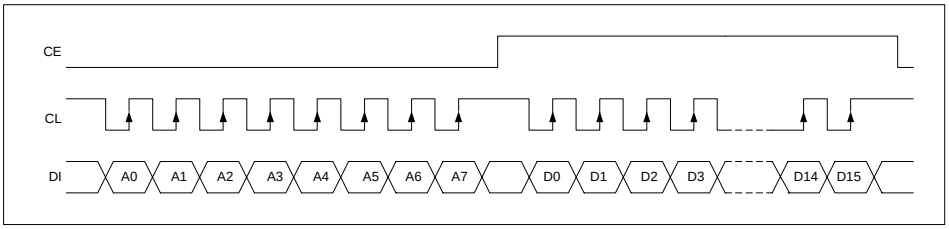


Figure 20 CCB Interface – CL stopped high

1. A[7:0] are Device Address bits
2. D[15:9] are Control Address bits
3. D[8:0] are Control Data bits

The address A[7:0] for WM8771 is 8Ch (10001100).

CONTROL INTERFACE REGISTERS

DIGITAL AUDIO INTERFACE CONTROL REGISTER

Interface format is selected via the FMT[1:0] register bits:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
10110 Interface Control	1:0	FMT[1:0]	10	Interface format Select 00 : right justified mode 01: left justified mode 10: I2S mode 11: DSP (early or late) mode

In left justified, right justified or I2S modes, the LRP register bit controls the polarity of ADCLRC/DACLRC. If this bit is set high, the expected polarity of ADCLRC/DACLRC will be the opposite of that shown Figure 11, Figure 12 and Figure 13. Note that if this feature is used as a means of swapping the left and right channels, a 1 sample phase difference will be introduced. In DSP modes, the LRP register bit is used to select between early and late modes.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
10110 Interface Control	2	LRP	0	In left/right/i2s modes: ADCLRC/DACLRC Polarity (normal) 0 : normal ADCLRC/DACLRC polarity 1: inverted ADCLRC/DACLRC polarity
				In DSP mode: 0 : Early DSP mode 1: Late DSP mode

By default, ADCLRC/DACLRC and DIN1/2/3/4 are sampled on the rising edge of BCLK and should ideally change on the falling edge. Data sources that change ADCLRC/DACLRC and DIN1/2/3/4 on the rising edge of BCLK can be supported by setting the BCP register bit. Setting BCP to 1 inverts the polarity of BCLK to the inverse of that shown in Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16 and Figure 17.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
10110 Interface Control	3	BCP	0	BCLK Polarity (DSP modes) 0 : normal BCLK polarity 1: inverted BCLK polarity

The IWL[1:0] bits are used to control the input word length.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
10110 Interface Control	5:4	WL[1:0]	10	Input Word Length 00 : 16 bit data 01: 20 bit data 10: 24 bit data 11: 32 bit data

Note: If 32-bit mode is selected in right justified mode, the WM8771 defaults to 24 bits.

In all modes, the data is signed 2's complement. The digital filters always input 24-bit data. If the DAC is programmed to receive 16 or 20 bit data, the WM8771 pads the unused LSBs with zeros. If the DAC is programmed into 32 bit mode, the 8 LSBs are ignored.

Note: In 24 bit I2S mode, any width of 24 bits or less is supported provided that ADCLRC/DACLRC is high for a minimum of 24 BCLKs and low for a minimum of 24 BCLKs.

A number of options are available to control how data from the Digital Audio Interface is applied to the DAC channels.

Control bit MS selects between audio interface Master and Slave Modes. In Master mode ADCLRC, DACLRC and BCLK are outputs and are generated by the WM8771. In Slave mode ADCLRC, DACLRC and BCLK are inputs to WM8771.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
10111 Interface Control	8	MS	0	Audio Interface Master/Slave Mode select: 0 : Slave Mode 1: Master Mode

MASTER MODE ADCLRC/DACLRC FREQUENCY SELECT

In Master mode the WM8771 generates ADCLRC, DACLRC and BCLK. These clocks are derived from master clock and the ratio of MCLK to ADCLRC and DACLRC are set by ADCRATE and DACRATE.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
10111 ADCLRC and DACLRC frequency select	2:0	ADCRATE[2:0]	010	Master Mode MCLK:ADCLRC ratio select: 000: 128fs 001: 192fs 010: 256fs 011: 384fs 100: 512fs 101: 768fs
	6:4	DACRATE[2:0]	010	Master Mode MCLK:DACLRC ratio select: 000: 128fs 001: 192fs 010: 256fs 011: 384fs 100: 512fs 101: 768fs

ADC OVERSAMPLING RATE SELECT

For ADC operation at 96kHz it is recommended that the user set the ADCOSR bit. This changes the ADC signal processing oversample rate to 64fs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
10111 ADC Oversampling Rate	3	ADCOSR	0	ADC oversampling rate select 0: 128x oversampling 1: 64x oversampling

MUTE MODES

The WM8771 has individual mutes for each of the four DAC channels. Setting MUTE for a channel will apply a 'soft' mute to the input of the digital filters of the channel muted. The WM8770 has individual mutes for each of the four DAC channels. Setting MUTE for a channel will apply a 'soft' mute to the input of the digital filters of the channel muted. DMUTE[0] mutes DAC channel 1, DMUTE[1] mutes DAC channel 2, DMUTE[2] mutes DAC channel 3 & DMUTE[3] mutes DAC channel 4.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
10100 DAC Mute	3:0	DMUTE[3:0]	0	DAC Soft Mute select 0 : Normal Operation 1: Soft mute enabled

Setting the MUTEALL register bit will apply a 'soft' mute to the input of all the DAC digital filters:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
10100 DAC Mute	4	MUTEALL	0	Soft Mute select 0 : Normal Operation 1: Soft mute all channels

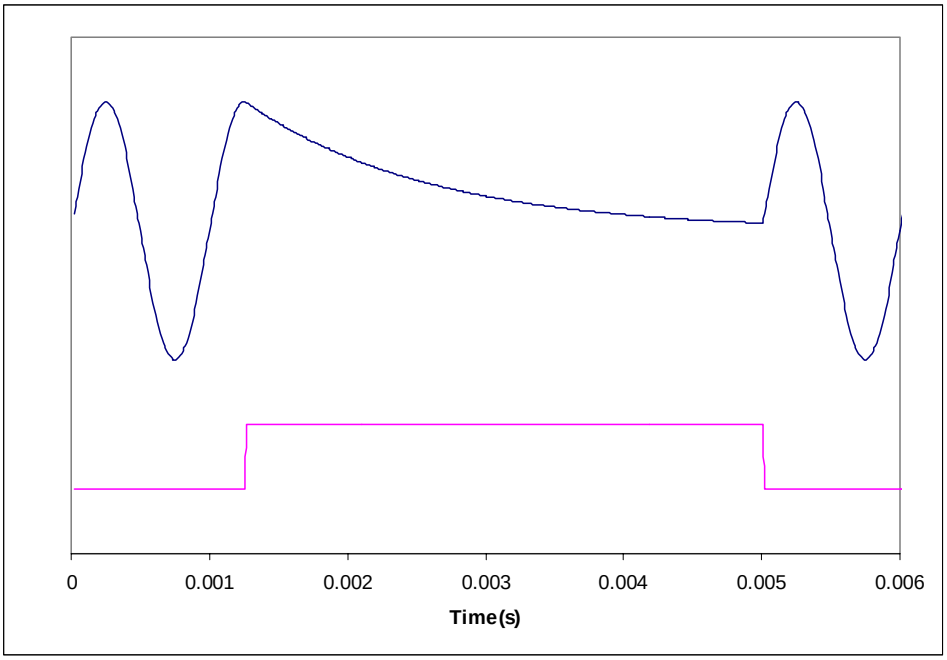


Figure 21 Application and Release of Soft Mute

Figure 21 shows the application and release of MUTE whilst a full amplitude sinusoid is being played at 48kHz sampling rate. When MUTE (lower trace) is asserted, the output (upper trace) begins to decay exponentially from the DC level of the last input sample. The output will decay towards V_{MID} with a time constant of approximately 64 input samples. If MUTE is applied to all channels for 1024 or more input samples the outputs will be connected directly to Vmid, if IZD is set. When MUTE is de-asserted, the output will restart immediately from the current input sample.

Note that all other means of muting the DAC channels: setting the PL[3:0] bits to 0, setting the PDWN bit or setting attenuation to 0 will cause much more abrupt muting of the output.

Each ADC channel also has an individual mute control bit, which mutes the input to the ADC. In addition both channels may be muted by setting ADCMUTE.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
11001 ADC Mute	7	ADCMUTE	0	ADC MUTE Left and Right 0 : Normal Operation 1: mute ADC left and ADC right
11001 ADC Mute Left	5	MUTE	0	ADC Mute select 0 : Normal Operation 1: mute ADC left
11010 ADC Mute Right	5	MUTE	0	ADC Mute select 0 : Normal Operation 1: mute ADC right

The Record outputs may be enabled by setting RECEN[2:0], where RECEN[0] mutes the REC1L and REC1R outputs, RECEN[1] mutes the REC2L and REC2R outputs and RECEN[2] mutes the REC3L and REC3R outputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
10100 REC Enable	[7:5]	RECMUTE[2:0]	000	REC Output Enable 0 : REC output disabled 1: REC output enabled

DE-EMPHASIS MODE

A digital De-emphasis filter may be applied to each DAC channel. The De-emphasis filter for each stereo channel is enabled under the control of DEEMP[3:0]. DEEMP[0] enables the de-emphasis filter for channel 1, DEEMP[1] enables the de-emphasis filter for channel 2, DEEMP[2] enables the de-emphasis filter for channel 3 and DEEMP[3] enables the de-emphasis filter for channel 4.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
10101 DAC De-emphasis Control	[3:0]	DEEMPH[3:0]	0000	De-emphasis mode select: 0 : Normal Mode 1: De-emphasis Mode

Refer to Figure 29, Figure 30, Figure 31, Figure 32, Figure 33 and Figure 34 for details of the De-Emphasis modes at different sample rates.

POWERDOWN MODE AND ADC/DAC DISABLE

Setting the PDWN register bit immediately powers down the WM8771. All trace of the previous input samples are removed, but all control register settings are preserved. When PDWN is cleared the digital filters will be reinitialised. . It is recommended that the 8-channel input mux and buffer, ADC, DAC and output buffers are powered down before setting PDWN.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION

11000 Powerdown Control	0	PDWN	0	Power Down Mode Select: 0 : Normal Mode 1: Power Down Mode

The ADC and DACs may also be powered down by setting the ADCD and DACD disable bits. Setting ADCD will disable the ADC and select a low power mode. The ADC digital filters will be reset and will reinitialise when ADCD is reset. Each Stereo DAC channel has a separate disable DACD[3:0]. Setting DACD for a channel will disable the DACs and select a low power mode, also connecting the DAC outputs to VMID. Resetting DACD will reinitialise the digital filters.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
11000 Powerdown Control	1	ADCD	1	ADC Disable: 0 : Normal Mode 1: Power Down Mode
	5:2	DACD[3:0]	1	DAC Disable: 0 : Normal Mode 1: Power Down Mode

ATTENUATOR CONTROL MODE

Setting the ATC register bit causes the left channel attenuation settings to be applied to both left and right channel DACs from the next audio input sample. No update to the attenuation registers is required for ATC to take effect.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
10011 DAC Channel Control	1	ATC	0	Attenuator Control Mode: 0 : Right channels use Right attenuations 1: Right Channels use Left attenuations

INFINITE ZERO DETECT

Setting the IZD register bit will enable the internal infinite zero detect function:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
10011 DAC Channel Control	2	IZD	0	Infinite zero Mute Enable 0 : disable infinite zero mute 1: enable infinite zero Mute

With IZD enabled, applying 1024 consecutive input samples to all 8 DAC channels will cause all outputs to be muted to V_{MID}. Mute will be removed as soon as any channel receives a non-zero input.

ZERO FLAG OUTPUT

The DZFM control bits allow the selection of the eight DAC channel zero flag bits for output on the ZFLAG1 and ZFLAG2 pins. A '1' on ZFLAG1 or ZFLAG2 indicates 1024 consecutive zero input samples to the channels selected.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
10101 Zero Flag Select	7:4	DZFM[3:0]	0000	Selects the output for ZFLG1 and ZFLG2 pins (see Table 9). A '1' indicates 1024 consecutive zero input samples on the channels selected.

DAC OUTPUT CONTROL

The DAC output control word determines how the left and right inputs to the audio Interface are applied to the left and right DACs:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION		
10011 DAC Control	7:4	PL[3:0]	1001	PL[3:0]	Left Output	Right Output
				0000	Mute	Mute
				0001	Left	Mute
				0010	Right	Mute
				0011	(L+R)/2	Mute
				0100	Mute	Left
				0101	Left	Left
				0110	Right	Left
				0111	(L+R)/2	Left
				1000	Mute	Right
				1001	Left	Right
				1010	Right	Right
				1011	(L+R)/2	Right
				1100	Mute	(L+R)/2
				1101	Left	(L+R)/2
				1110	Right	(L+R)/2
				1111	(L+R)/2	(L+R)/2

DAC DIGITAL VOLUME CONTROL

The DAC volume may be adjusted in the digital domain using independent digital attenuation control registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
01001 Digital Attenuation DACL1	7:0	LDA1[7:0]	11111111 (0dB)	Digital Attenuation data for Left channel DACL1 in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store LDA1 in intermediate latch (no change to output) 1: Store LDA1 and update attenuation on all channels
01010 Digital Attenuation DACR1	7:0	RDA1[6:0]	11111111 (0dB)	Digital Attenuation data for Right channel DACR1 in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store RDA1 in intermediate latch (no change to output) 1: Store RDA1 and update attenuation on all channels.
01011 Digital Attenuation DACL2	7:0	LDA2[7:0]	11111111 (0dB)	Digital Attenuation data for Left channel DACL2 in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store LDA2 in intermediate latch (no change to output) 1: Store LDA2 and update attenuation on all channels.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
01100 Digital Attenuation DACR2	7:0	RDA2[7:0]	11111111 (0dB)	Digital Attenuation data for Right channel DACR2 in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store RDA2 in intermediate latch (no change to output) 1: Store RDA2 and update attenuation on all channels.
01101 Digital Attenuation DACL3	7:0	LDA3[7:0]	11111111 (0dB)	Digital Attenuation data for Left channel DACL3 in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store LDA3 in intermediate latch (no change to output) 1: Store LDA3 and update attenuation on all channels.
01110 Digital Attenuation DACR3	7:0	RDA3[7:0]	11111111 (0dB)	Digital Attenuation data for Right channel DACR3 in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store RDA3 in intermediate latch (no change to output) 1: Store RDA3 and update attenuation on all channels.
01111 Digital Attenuation DACL4	7:0	LDA4[7:0]	11111111 (0dB)	Digital Attenuation data for Left channel DACL4 in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store LDA4 in intermediate latch (no change to output) 1: Store LDA4 and update attenuation on all channels.
10000 Digital Attenuation DACR4	7:0	RDA4[7:0]	11111111 (0dB)	Digital Attenuation data for Right channel DACR4 in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store RDA4 in intermediate latch (no change to output) 1: Store RDA4 and update attenuation on all channels.
10001 Master Digital Attenuation (all channels)	7:0	MASTDA[7:0]	11111111 (0dB)	Digital Attenuation data for all DAC channels in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store gain in intermediate latch (no change to output) 1: Store gain and update attenuation on all channels.

L/RDAX[7:0]	ATTENUATION LEVEL
00(hex)	-∞ dB (mute)
01(hex)	-127.5dB
:	:
:	:
:	:
FE(hex)	-0.5dB
FF(hex)	0dB

Table 10 Digital Volume Control Attenuation Levels

The Digital volume control also incorporates a zero cross detect circuit which detects a transition through the zero point before updating the digital volume control with the new volume. This is enabled by control bit DZCEN.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
10011 DAC Control	0	DZCEN	0	DAC Digital Volume Zero Cross Enable: 0: Zero cross detect disabled 1: Zero cross detect enabled

DAC OUTPUT PHASE

The DAC Phase control word determines whether the output of each DAC is non-inverted or inverted

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION		
10010 DAC Phase	7:0	PH[7:0]	00000000	Bit	DAC	Phase
				0	DAC1L	1 = invert
				1	DAC1R	1 = invert
				2	DAC2L	1 = invert
				3	DAC2R	1 = invert
				4	DAC3L	1 = invert
				5	DAC3R	1 = invert
				6	DAC4L	1 = invert
				7	DAC4R	1 = invert

ADC GAIN CONTROL

Control bits LAG[4:0] and RAG[4:0] control the ADC input gain, allowing the user to attenuate the ADC input signal to match the full-scale range of the ADC. The gain is independently adjustable on left and right inputs. Left and right inputs may also be independently muted. The LRBOTH control bit allows the user to write the same attenuation value to both left and right volume control registers. The ADC volume and mute also applies to the bypass signal path

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
11001 Attenuation ADCL	4:0	LAG[4:0]	01100 (0dB)	Attenuation data for Left channel ADC gain in 1dB steps. See Table 11
	5	MUTE	0	Mute for Left channel ADC: 0: Mute off 1: Mute on
	6	LRBOTH	0	Setting LRBOTH will write the same gain value to LAG[4:0] and RAG[4:0]
11010 Attenuation ADCR	4:0	RAG[4:0]	01100 (0dB)	Attenuation data for right channel ADC gain in 1dB steps. See Table 11
	5	MUTE	0	Mute for Right channel ADC: 0: Mute off]1: Mute on
	6	LRBOTH	0	Setting LRBOTH will write the same gain value to RAG[4:0] and LAG[4:0]

ADC INPUT GAIN

Registers LAG and RAG control the left and right channel gain into the stereo ADC in 1dB steps from +19dB to –12dB Table 8 shows how the attenuation levels are selected from the 5-bit words.

L/RAG[6:0]	ATTENUATION LEVEL
0	-12dB
:	:
01100	0dB
:	:
11111	+19dB

Table 11 ADC gain control

ADC HIGHPASS FILTER DISABLE

The ADC digital filters contain a digital highpass filter. This defaults to enabled and can be disabled using software control bit ADCHPD.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
10110 ADC control	8	ADCHPD	0	ADC Highpass filter disable: 0: Highpass filter enabled 1: Highpass filter disabled

ADC INPUT MUX AND POWERDOWN CONTROL

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
11011 ADC mux and powerdown control	2:0	LMX[2:0]	000	ADC left channel input mux control bits (see Figure 35)
	6:4	RMX[2:0]	000	ADC right channel input mux control bits (see Figure 35)
	8	AINPD	1	Input mux and buffer powerdown 0: Input mux and buffer enabled 1: Input mux and buffer powered down

Register bits LMX and RMX control the left and right channel inputs into the stereo ADC. The default is AIN1. However if the analogue input buffer is powered down, by setting AINPD, then all 8-channel mux inputs are switched to buffered VMIDADC.

LMX[2:0]	LEFT ADC INPUT	RMX[2:0]	RIGHT ADC INPUT
000	AIN1L	000	AIN1L
001	AIN2L	001	AIN2L
010	AIN3L	010	AIN3L
011	AIN4L	011	AIN4L
100	AIN5L	100	AIN5L
101	AIN6L	101	AIN6L
110	AIN7L	110	AIN7R
111	AIN8L	111	AIN8R

Table 12 ADC input mux control

The DAC output buffers can be powered down under control of OUTPD[3:0]. Each stereo channel may be powered down separately. Setting OUTPD[3:0] will power off the output buffer and switch the analogue outputs VOUTL/R to VMIDDAC to maintain a dc level on the output.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
11100 Output Powerdown control	8:7	OUTPD[1:0]	11	DAC Output Powerdown select 0: output buffer enabled 1: output buffer powered down

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
11101 Output Powerdown control	8:7	OUTPD[3:2]	11	DAC Output Powerdown select 0: output buffer enabled 1: output buffer powered down

SOFTWARE REGISTER RESET

Writing to register 11111 will cause a register reset, resetting all register bits to their default values.

REGISTER MAP

The complete register map is shown below. The detailed description can be found in the relevant text of the device description. These can be controlled using the Control Interface. All unused bits should be set to '0'.

REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
R9(09h)	0	0	0	1	0	0	1	UPDATE	LDA1[7:0]								X11111111
R10(0Ah)	0	0	0	1	0	1	0	UPDATE	RDA1[7:0]								X11111111
R11(0Bh)	0	0	0	1	0	1	1	UPDATE	LDA2[7:0]								X11111111
R12(0Ch)	0	0	0	1	1	0	0	UPDATE	RDA2[7:0]								X11111111
R13(0Dh)	0	0	0	1	1	0	1	UPDATE	LDA3[7:0]								X11111111
R14(0Eh)	0	0	0	1	1	1	0	UPDATE	RDA3[7:0]								X11111111
R15(0Fh)	0	0	0	1	1	1	1	UPDATE	LDA4[7:0]								X11111111
R16(10h)	0	0	1	0	0	0	0	UPDATE	RDA4[7:0]								X11111111
R17(11h)	0	0	1	0	0	0	1	UPDATE	MASTDA[7:0]								X11111111
R18(12h)	0	0	1	0	0	1	0	0	PHASE[8:0]								000000000
R19(13h)	0	0	1	0	0	1	1	0	PL[3:0]				0	IZD	ATC	DZCEN	010010000
R20(14h)	0	0	1	0	1	0	0	0	RECMUTE[2:0]			MUTEALL	DMUTE[3:0]				000000000
R21(15h)	0	0	1	0	1	0	1	0	DZFM[3:0]				DEEMP[3:0]				000000000
R22(16h)	0	0	1	0	1	1	0	ADCHPD	0	0	WL[1:0]		BCP	LRP	FMT[1:0]		000100010
R23(17h)	0	0	1	0	1	1	1	MS	0	DACRATE[2:0]			ADCOSR	ADCRATE[2:0]			000010010
R24(18h)	0	0	1	1	0	0	0	0	0	0	DACD[3:0]				ADCD	PWDN	000111110
R25(19h)	0	0	1	1	0	0	1	0	0	LRBOTH	MUTE	LAG					000001100
R26(1Ah)	0	0	1	1	0	1	0	0	0	LRBOTH	MUTE	RAG					000001100
R27(1Bh)	0	0	1	1	0	1	1	AINPD	0	RMX			0	LMX			100000000
R28(1Ch)	0	0	1	1	1	0	0	OUTPD[1:0]		0	0	0	0	0	0	0	110000000
R29i1Dh)	0	0	1	1	1	0	1	OUTPD[3:2]		0	0	0	0	0	0	0	110000000
R31(1Fh)	0	0	1	1	1	1	1	RESET									Not reset
	ADDRESS							DATA									DEFAULT

01001 Digital Attenuation DACL1	7:0	LDA1[7:0]	11111111 (0dB)	Digital Attenuation data for Left channel DACL1 in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store LDA1 in intermediate latch (no change to output) 1: Store LDA1 and update attenuation on all channels
01010 Digital Attenuation DACR1	7:0	RDA1[6:0]	11111111 (0dB)	Digital Attenuation data for Right channel DACR1 in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store RDA1 in intermediate latch (no change to output) 1: Store RDA1 and update attenuation on all channels.
01011 Digital Attenuation DACL2	7:0	LDA2[7:0]	11111111 (0dB)	Digital Attenuation data for Left channel DACL2 in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store LDA2 in intermediate latch (no change to output) 1: Store LDA2 and update attenuation on all channels.
01100 Digital Attenuation DACR2	7:0	RDA2[7:0]	11111111 (0dB)	Digital Attenuation data for Right channel DACR2 in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store RDA2 in intermediate latch (no change to output) 1: Store RDA2 and update attenuation on all channels.
01101 Digital Attenuation DACL3	7:0	LDA3[7:0]	11111111 (0dB)	Digital Attenuation data for Left channel DACL3 in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store LDA3 in intermediate latch (no change to output) 1: Store LDA3 and update attenuation on all channels.
01110 Digital Attenuation DACR3	7:0	RDA3[7:0]	11111111 (0dB)	Digital Attenuation data for Right channel DACR3 in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store RDA3 in intermediate latch (no change to output) 1: Store RDA3 and update attenuation on all channels.
01111 Digital Attenuation DACL4	7:0	LDA4[7:0]	11111111 (0dB)	Digital Attenuation data for Left channel DACL4 in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store LDA4 in intermediate latch (no change to output) 1: Store LDA4 and update attenuation on all channels.
10000 Digital Attenuation DACR4	7:0	RDA4[7:0]	11111111 (0dB)	Digital Attenuation data for Right channel DACR4 in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store RDA4 in intermediate latch (no change to output) 1: Store RDA4 and update attenuation on all channels.
10001 Master Digital Attenuation (all channels)	7:0	MASTDA[7:0]	11111111 (0dB)	Digital Attenuation data for all DAC channels in 0.5dB steps. See Table 10
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store gain in intermediate latch (no change to output) 1: Store gain and update attenuation on all channels.

<table>
<tr><td>10010
Phase swaps</td><td>7:0</td><td>PHASE</td><td>00000000</td><td>Controls phase of DAC outputs
0: Sets non inverted output phase
1: inverts phase of DAC output</td></tr>
<tr><td rowspan="5">10011
DAC Control</td><td>0</td><td>DZCEN</td><td>0</td><td>DAC Digital Volume Zero Cross Enable:
0: Zero Cross detect disabled
1: Zero Cross detect enabled</td></tr>
<tr><td>1</td><td>ATC</td><td>0</td><td>Attenuator Control
0: All DACs use attenuations as programmed.
1: Right channel DACs use corresponding left DAC attenuations</td></tr>
<tr><td>2</td><td>IZD</td><td>0</td><td>Infinite zero detection circuit control and automute control
0: Infinite zero detect disabled
1: Infinite zero detect enabled</td></tr>
<tr><td>7:4</td><td>PL[3:0]</td><td>1001</td><td>DAC Output Control
<table>
<tr><td>PL[3:0]</td><td>Left Output</td><td>Right Output</td><td>PL[3:0]</td><td>Left Output</td><td>Right Output</td></tr>
<tr><td>0000</td><td>Mute</td><td>Mute</td><td>1000</td><td>Mute</td><td>Right</td></tr>
<tr><td>0001</td><td>Left</td><td>Mute</td><td>1001</td><td>Left</td><td>Right</td></tr>
<tr><td>0010</td><td>Right</td><td>Mute</td><td>1010</td><td>Right</td><td>Right</td></tr>
<tr><td>0011</td><td>(L+R)/2</td><td>Mute</td><td>1011</td><td>(L+R)/2</td><td>Right</td></tr>
<tr><td>0100</td><td>Mute</td><td>Left</td><td>1100</td><td>Mute</td><td>(L+R)/2</td></tr>
<tr><td>0101</td><td>Left</td><td>Left</td><td>1101</td><td>Left</td><td>(L+R)/2</td></tr>
<tr><td>0110</td><td>Right</td><td>Left</td><td>1110</td><td>Right</td><td>(L+R)/2</td></tr>
<tr><td>0111</td><td>(L+R)/2</td><td>Left</td><td>1111</td><td>(L+R)/2</td><td>(L+R)/2</td></tr>
</table></td></tr>
<tr><td rowspan="3">10100
DAC and REC Mute</td><td>3:0</td><td>DMUTE[3:0]</td><td>0000</td><td>DAC channel soft mute enables:
0: mute disabled
1: mute enabled</td></tr>
<tr><td>4</td><td>MUTEALL</td><td>0</td><td>DAC channel master soft mute. Mutes all DAC channels:
0: mute disabled
1: mute enabled</td></tr>
<tr><td>7:5</td><td>RECEN[2:0]</td><td>000</td><td>REC output enable
0 : REC outputs muted
1: REC outputs enabled</td></tr>
<tr><td rowspan="2">10101
DAC Control</td><td>7:4</td><td>DZFM</td><td>0000</td><td>Selects the ouput for ZFLG1 and ZFLG2 pins (see Table 9).
1: indicates 1024 consecutive zero input samples on the channels selected
0: indicates at least one of selected channels has non zero sample in last 1024 inputs</td></tr>
<tr><td>3:0</td><td>DEEMP</td><td>0000</td><td>De-emphasis mode select:
0 : Normal Mode
1: De-emphasis Mode</td></tr>
<tr><td></td><td>1:0</td><td>FMT[1:0]</td><td>00</td><td>Interface format select</td></tr>
</table>

	2	LRP	0	ADCLRC/DACLRC Polarity or DSP Early/Late mode select	
				Left Justified / Right Justified / I2S 0: Standard DACLRC Polarity 1: Inverted DACLRC Polarity	DSP Mode 0: Data in-line with ADCLRC/DACLRC 1: Data delayed by 1 BCLK
	3	BCP	0	BITCLK Polarity 0: Normal - DIN[3:0], DACLRC & ADCLRC sampled on rising edge of BCLK; DOUT changes on falling edge of BCLK. 1: Inverted - DIN[3:0], DACLRC & ADCLRC sampled on falling edge of BCLK; DOUT changes on rising edge of BCLK.	
	5:4	WL[1:0]	10	Input Word Length 00: 16-bit Mode 01: 20-bit Mode 10: 24-bit Mode 11: 32-bit Mode (not supported in right justified mode)	
	8	ADCHPD	0	ADC Highpass Filter Disable: 0: Highpass Filter enabled 1: Highpass Filter disabled	
10111 Master Mode control	2:0	ADCRATE[2:0]	010	Master Mode MCLK:ADCLRC ratio select: 000: 128fs 001: 192fs 010: 256fs 011: 384fs 100: 512fs	
	3	ADCOSR	0	ADC oversample rate select 0: 128x oversampling 1: 64x oversapmling	
	6:4	DACRATE[2:0]	010	Master Mode MCLK:DACLRC ratio select: 000: 128fs 001: 192fs 010: 256fs 011: 384fs 100: 512fs	
	8	MS	0	Maser/Slave interface mode select 0: Slave Mode – ADCLRC, DACLRC and BCLK are inputs 1: Master Mode – ADCLRC, DACLRC and BCLK are outputs	
11000 Powerdown Control	0	PWDN	0	Chip Powerdown Control (works in tandem with ADCD and DACD):	
	1	ADCD	1	ADC powerdown:	
	5:2	DACD[3:0]	1111	DAC powerdown	
11001 Attenuation ADCL	4:0	LAG[4:0]	01100	Attenuation data for left channel ADC gain in 1dB steps	
	5	MUTE	0	Mute for Left channel ADC: 0: Mute off 1: Mute on	
	6	LRBOTH	0	Setting LRBOTH will write the same gain value to LAG[4:0 and RAG[4:0]	

	7	ADCMUTE	0	Mute for Left and Right channel ADC: 0: Mute off 1: Mute on
11010 Attenuation ADCR	4:0	RAG[4:0]	01100 (0dB)	Attenuation data for right channel ADC gain in 1dB steps
	5	MUTE	0	Mute for Right channel ADC: 0: Mute off 1: Mute on
	6	LRBOTH	0	Setting LRBOTH will write the same gain value to RAG[4:0 and LAG[4:0]
11011 ADC mux and powerdown control	2:0	LMX[2:0]	000	ADC left channel input mux control bits (see Table 12)
	6:4	RMX[2:0]	000	ADC right channel input mux control bits (see Table 12)
	8	AINPD	1	Input mux and buffer powerdown 0: Input mux and buffer enabled 1: Input mux and buffer powered down
11100 Output powerdown control	8:7	OUTPD[1:0]	11	DAC Output Powerdown select 0: output buffer enabled 1: output buffer powered down
11101 Output powerdown control	8:7	OUTPD[3:2]	11	DAC Output Powerdown select 0: output buffer enabled 1: output buffer powered down
11111 Software reset	[8:0]	RESET	Not reset	Writing to this register will apply a reset to the device registers.

Table 13 Register Map Description

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	±0.01 dB	0		0.4535fs	
	-6dB		0.5fs		
Passband ripple				±0.01	dB
Stopband		0.5465fs			
Stopband Attenuation	f > 0.5465fs	-65			dB
Group Delay			22		fs
DAC Filter					
Passband	±0.05 dB			0.444fs	
	-3dB		0.487fs		
Passband ripple				±0.05	dB
Stopband		0.555fs			
Stopband Attenuation	f > 0.555fs	-60			dB
Group Delay			16		fs

Table 14 Digital Filter Characteristics

DAC FILTER RESPONSES

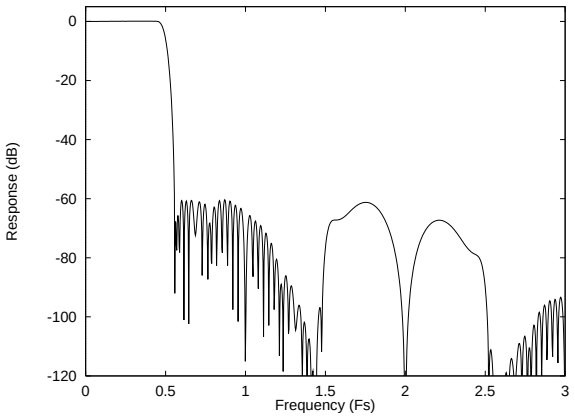


Figure 22 DAC Digital Filter Frequency Response – 44.1, 48 and 96kHz

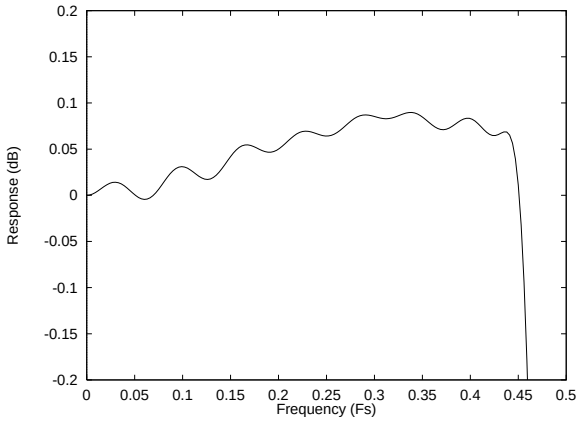


Figure 23 DAC Digital Filter Ripple – 44.1, 48 and 96kHz

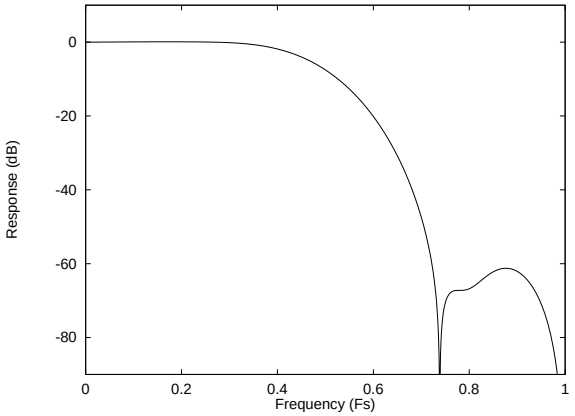


Figure 24 DAC Digital Filter Frequency Response – 192kHz

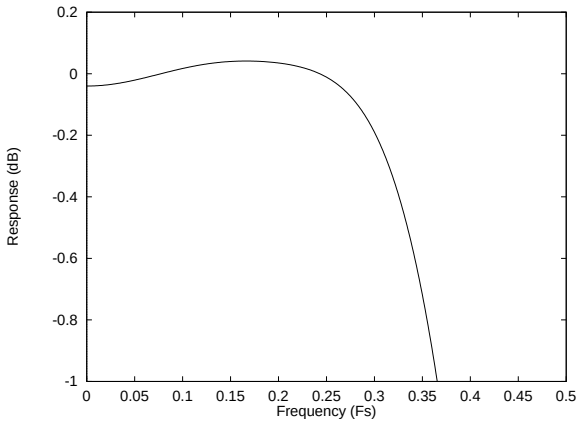


Figure 25 DAC Digital filter Ripple – 192kHz

ADC FILTER RESPONSES

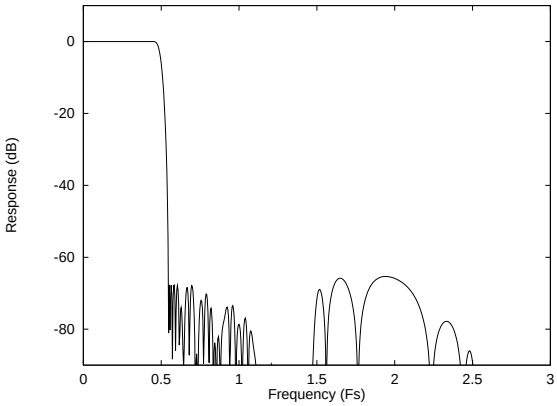


Figure 26 ADC Digital Filter Frequency Response

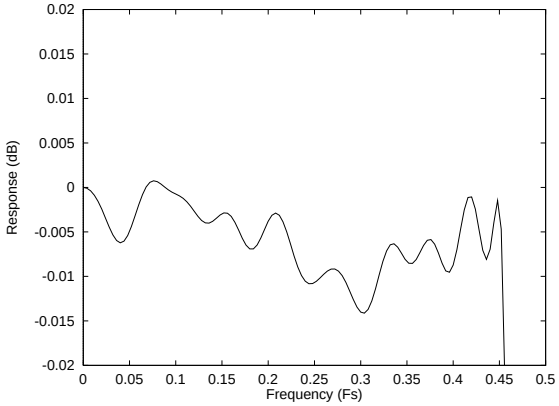


Figure 27 ADC Digital Filter Ripple

ADC HIGH PASS FILTER

The WM8771 has a selectable digital highpass filter to remove DC offsets. The filter response is characterised by the following polynomial.

$$H(z) = \frac{1 - z^{-1}}{1 - 0.9995z^{-1}}$$

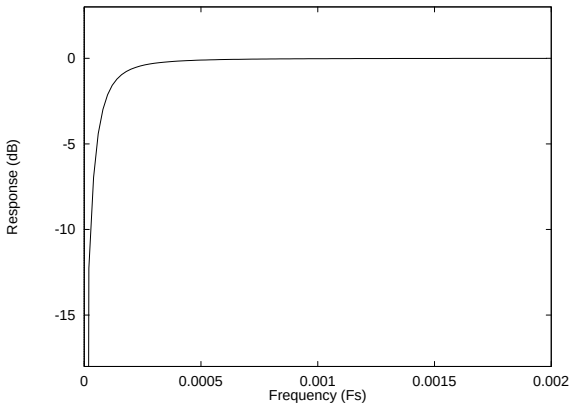


Figure 28 ADC Highpass Filter Response

DIGITAL DE-EMPHASIS CHARACTERISTICS

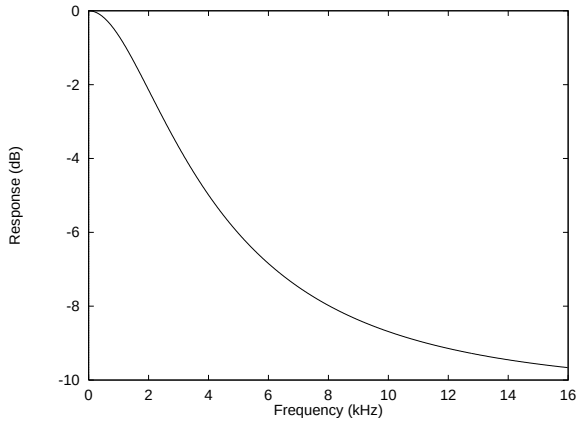


Figure 29 De-Emphasis Frequency Response (32kHz)

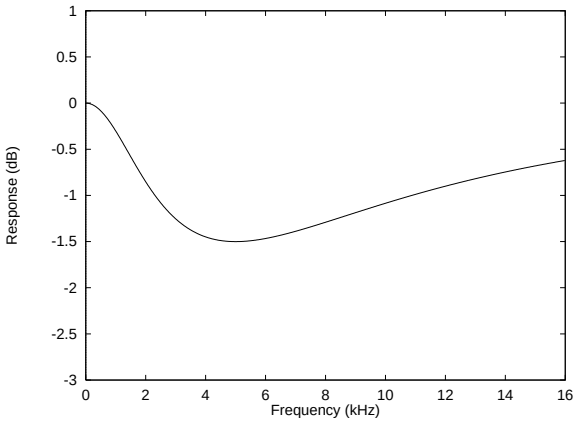


Figure 30 De-Emphasis Error (32KHz)

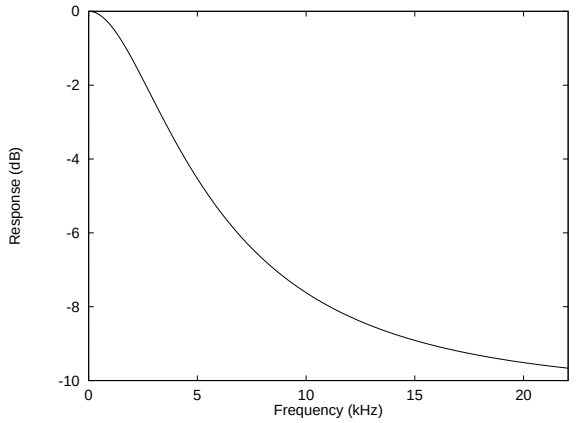


Figure 31 De-Emphasis Frequency Response (44.1KHz)

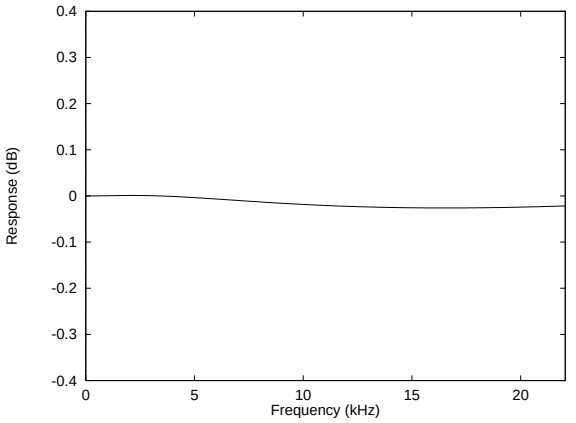


Figure 32 De-Emphasis Error (44.1KHz)

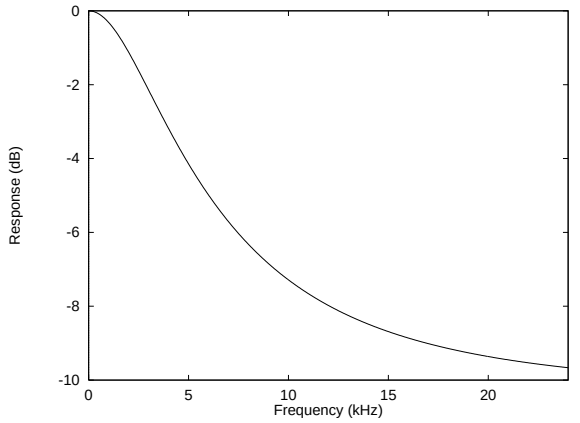


Figure 33 De-Emphasis Frequency Response (48kHz)

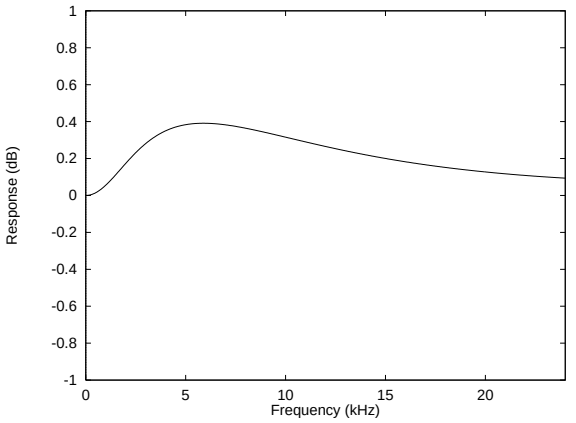


Figure 34 De-Emphasis Error (48kHz)

EXTERNAL CIRCUIT CONFIGURATION

In order to allow the use of 2V rms and larger inputs to the ADC and AUX inputs, a structure is used that uses external resistors to drop these larger voltages. This also increases the robustness of the circuit to external abuse such as ESD pulse.

Figure 35 shows the ADC input multiplexor circuit with external components allowing 2Vrms inputs to be applied.

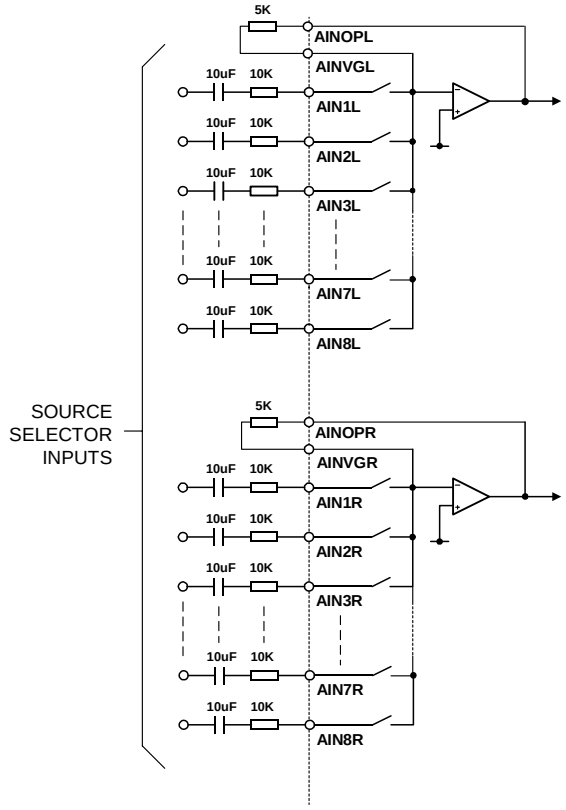


Figure 35 ADC input multiplexor confiuration

RECOMMENDED EXTERNAL COMPONENTS

It is recommended that a lowpass filter be applied to the output from each DAC channel for Hi-Fi applications. Typically a second order filter is suitable and provides sufficient attenuation of high frequency components (the unique low order, high bit count multi-bit sigma delta DAC structure used in WM8771 produces much less high frequency output noise than competitors devices). This filter is typically also used to provide the 2x gain needed to provide the standard 2Vrms output level from most consumer equipment. Figure 24 shows a suitable post DAC filter circuit, with 2x gain. Alternative inverting filter architectures might also be used with as good results.

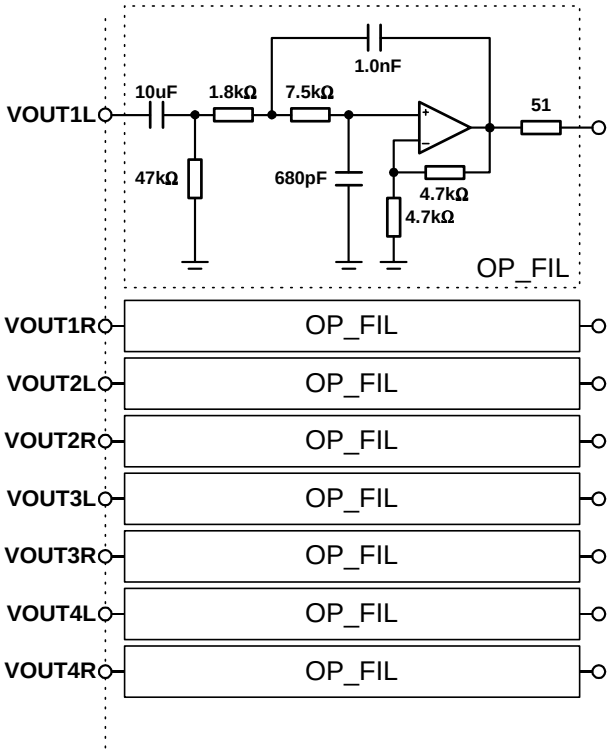
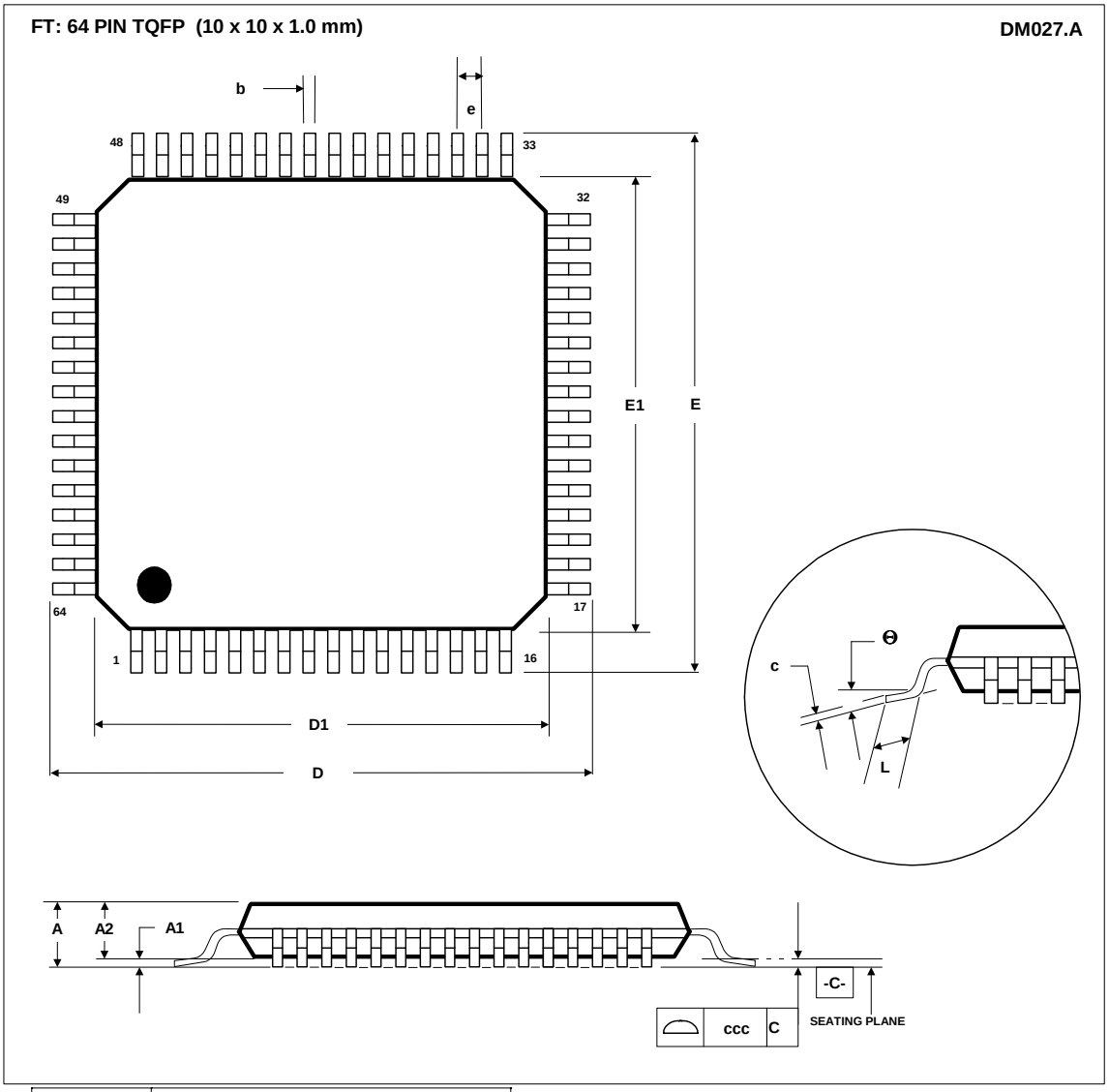


Figure 36 Recommended post DAC filter circuit

PACKAGE DIMENSIONS

FT: 64 PIN TQFP (10 x 10 x 1.0 mm) **DM027.A**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	1.20
A_1	0.05	-----	0.15
A_2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	-----	0.20
D	12.00 BSC		
D_1	10.00 BSC		
E	12.00 BSC		
E_1	10.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
Θ	0^o	3.5^o	7^o
Tolerances of Form and Position			
ccc	0.08		
REF:	JEDEC.95, MS-026		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MS-026, VARIATION = ACD. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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