2 X 2 PROTECTION CROSSPOINT SWITCH

SuperLite™
SY55854U

FEATURES

- Guaranteed f_{MAX} >2.5GHz over temperature
- 2.3V to 5.7V power supply
- Non-blocking "switch architecture"
- Guaranteed <15ps channel-to-channel skew
- Guaranteed <480ps propagation delay over temperature
- Configurable as 2:1 mux, 1:2 fan-out buffer, dual buffer, or 2 x 2 switch
- Accepts CML, PECL, LVPECL inputs
- Fully differential inputs/outputs
- Source terminated CML outputs for fast edge rates
- Wide operating temperature range: –40°C to +85°C
- Available in a tiny 16-pin EPAD-QSOP package

SuperLite™

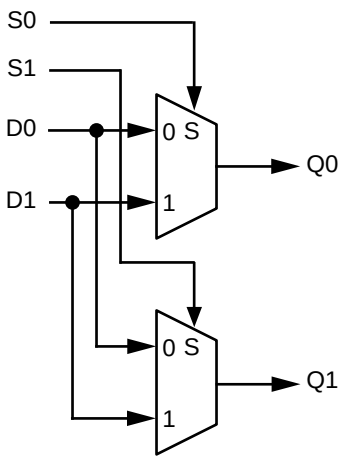
DESCRIPTION

The SY55854U is a fully differential, CML, 2 x 2-crosspoint switch. The non-blocking design allows any input to be connected to any output. Varying the state of the select inputs allows SY55854U to be used in backup, fault tolerant, protection, and backplane distribution applications.

SY55854U inputs can be terminated with a single resistor between the true and the complement pins of a given input.

The SY55854U is a member of Micrel's new SuperLite™ family of high-speed logic devices. This family features very small packaging, high signal integrity, and flexible supply voltage operation.

FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS

- High-speed logic
- Data communications systems
- Wireless communications systems
- Telecom systems
- Backplane redundancy

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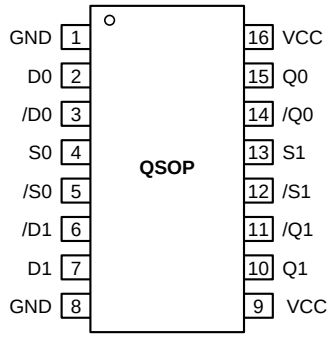
PACKAGE/ORDERING INFORMATION



16-Pin EPAD-QSOP
(Y16-1)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY55854UYI	Y16-1	Industrial	854U	Sn-Pb
SY55854UYITR[2]	Y16-1	Industrial	854U	Sn-Pb
SY55854UYY[3]	Y16-1	Industrial	854U with Pb-Free bar line indicator	NiPdAu Pb-Free
SY55854UYYTR[2, 3]	Y16-1	Industrial	854U with Pb-Free bar line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
2, 3	D0, /D0	CML/PECL/LVPECL Input (Differential). This is one of the data inputs to the crosspoint. It will be switched either to the Q0 output, the Q1 output, both outputs, or neither output, depending on the state of the S0 and S1 inputs.
4, 5	S0, /S0	CML/PECL/LVPECL Input (Differential). This selects input chooses which data input switches to the Q0 output. S0 logic low selects the D0 input, while S0 logic high selects the B input.
6, 7	/D1, D1	CML/PECL/LVPECL Input (Differential). This is the other data input to the crosspoint. It will be switched either to the Q0 output, the Q1 output, both outputs, or neither output, depending on the state of the S0 and S1 inputs.
1, 8	GND	Ground.
9, 16	VCC	Power Supply.
10, 11	Q1, /Q1	CML Output (Differential). This is the other output from the crosspoint. Input S1 selects either the D0 or D1 input to be switched to this output.
12, 13	/S1, S1	CML/PECL/LVPECL Input (Differential). This select input chooses which data input switches to the Q1 output. S1 logic low selects the D0 input, while S1 logic high selects the D1 input.
14, 15	/Q0, Q0	CML Output (Differential). This is one output from the crosspoint. Input S0 selects either the D0 or the D1 input to be switched to this output.

FUNCTIONAL DESCRIPTION

Establishing Static Logic Inputs

The true pin of an input pair is internally biased to ground through a 75kΩ resistor. The complement pin of an input pair is internally biased halfway between V_{CC} and ground by a voltage divider consisting of two 75kΩ resistors. In this way, unconnected inputs appear as logic zeros. To keep an input at static logic zero at V_{CC} > 3.0V, leave both inputs unconnected. For $V_{CC} \leq$ 3.0V, connect the complement input to V_{CC} and leave the true input unconnected. To make an input static logic one, connect the true input to V_{CC}, leave the complement input unconnected. These are the only two safe ways to cause inputs to be at a static value. In particular, no input pin should be directly connected to ground. All NC (no connect) pins should be unconnected.

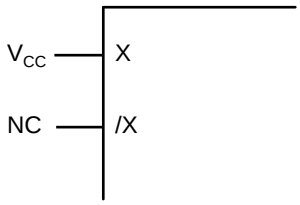


Figure 1. Hard Wiring a Logic "1" (1)

Note 1. X is either D0, D1, S0, or S1 input. /X is either /D0, /D1, /S0, or /S1 input.

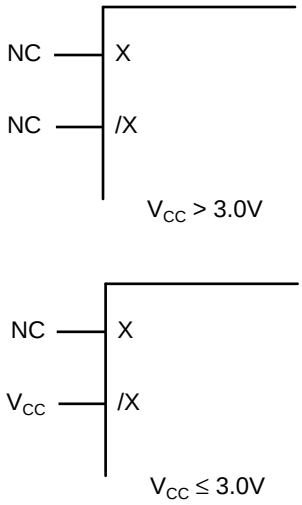


Figure 2. Hard Wiring a Logic "0" (1)

Usage

SY55854U is very versatile. Tying its select inputs in various ways varies its functionality. For example, tying the select inputs together turns SY55854U into a redundant distributor. Either input will be switched to both outputs simultaneously. This is very useful in redundant backplane applications. By cross-tying the select inputs, SY55854U becomes a true crosspoint, selecting between "straight through" and "cross connected" operation. Also, using the select inputs independently, SY55854U functions as two multiplexers. Setting the select inputs to static values turns SY55854U into a dual buffer, or a fan-out buffer.

To make larger crosspoints, cascade SY55854U devices, either in a tree or in a Banyan structure, as appropriate for your application.

TRUTH TABLE

S0	S1	Q0	Q1	Function
0	0	D0	D0	Fan-Out Buffer
0	1	D0	D1	Dual Buffer
1	0	D1	D0	Dual Buffer
1	1	D1	D1	Fan-Out Buffer
CTL	CTL	Same	Same	Redundant Distribution
CTL	/CTL	Opposite	Opposite	Crosspoint

CML TERMINATION

All inputs accept the output from any other member of this family. All outputs are source terminated 100Ω CML differential drivers as shown in Figures 3 and 4. SY55854U expects the inputs to be terminated, and that good high speed design practices be adhered to. SY55854U inputs are designed to accept a termination resistor between the true and complement inputs of a differential pair. 0402 form factor chip resistors will fit with some trace fanout.

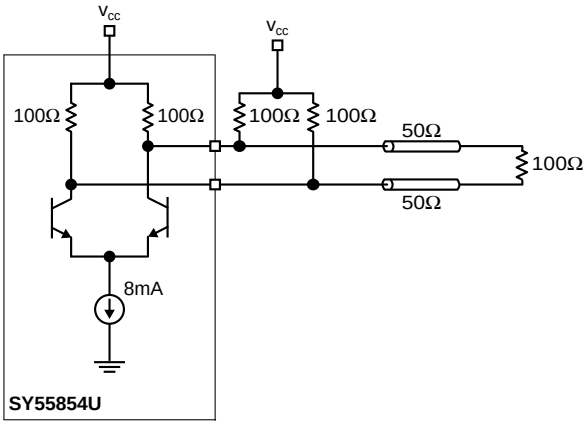


Figure 3a. Differentially Terminated (50Ω Load CML Output)

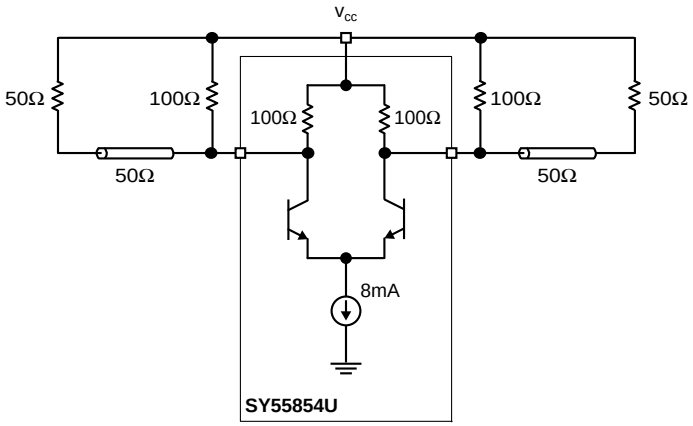


Figure 3b. Individually Terminated (50Ω Load CML Output)

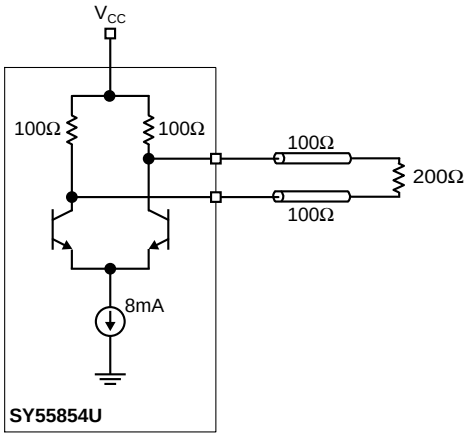


Figure 4. 100Ω Load CML Output

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{CC}	Power Supply Voltage	–0.5 to +6.0	V
V_{IN}	Input Voltage	–0.5 to V_{CC} +0.5	V
V_{OUT}	CML Output Voltage	V_{CC} –1.0 to V_{CC} +0.5	V
T_A	Operating Temperature Range	–40 to +85	°C
T_{LEAD}	Lead Temperature (soldering, 20 sec.)	260°C	°C
T_{store}	Storage Temperature Range	–65 to +150	°C

Note 1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.3V to 5.7V; GND = 0V

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{CC}	Power Supply Voltage	2.3	5.7	2.3	5.7	2.3	5.7	2.3	5.7	V
I_{CC}	Power Supply Current	—	60	—	60	—	60	—	60	mA

CML DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.3V to 5.7V; GND = 0V; T_A = –40°C to +85°C[2]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{ID}	Differential Input Voltage	100	—	—	mV	
V_{IH}	Input HIGH Voltage	1.6	—	V_{CC}	V	
V_{IL}	Input LOW Voltage	1.5	—	V_{CC} – 0.1	V	
V_{OH}	Output HIGH Voltage	V_{CC} – 0.020	V_{CC} – 0.010	V_{CC}	V	No Load
V_{OL}	Output LOW Voltage	V_{CC} – 0.97	V_{CC} – 0.825	V_{CC} – 0.660	V	No Load
V_{OS}	Output Voltage Swing[3]	0.700	0.800 0.400 0.200	0.950	V	No Load 100Ω Environment[5] 50Ω Environment[4]
R_{DRIVE}	Output Source Impedance	80	100	120	Ω	

Note 2. Equilibrium temperature.

Note 3. Actual voltage levels and differential swing will depend on customer termination scheme. Typically, a 400mV swing is available in the 100Ω environment and a 200mV swing in the 50Ω environment. Refer to the “CML Termination” diagram for more details.

Note 4. See Figure 3a and 3b.

Note 5. See Figure 4.

AC ELECTRICAL CHARACTERISTICS[1, 2]

V_{CC} = 2.3V to 5.7V; GND = 0V; T_A = –40°C to +85°C

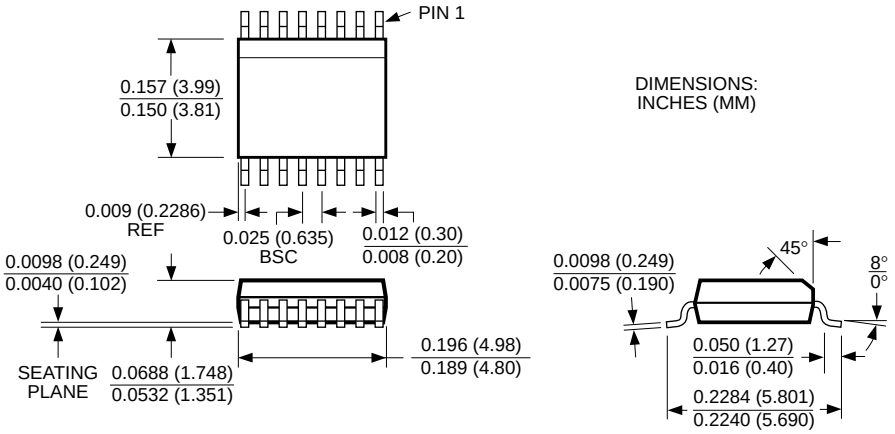
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
f_{MAX}	Max. Operating Frequency	2.5	—	—	GHz	
t_{PD}	Propagation Delay, S0, S1, D0, D1 to Q0, Q1	—	—	400	ps	
t_{SKEW}	Within-Device Skew[3] Part-to-Part Skew (Diff.)	— —	— —	15 100	ps	
t_r t_f	CML Output Rise/Fall Times (20% to 80%)	—	—	150	ps	

Note 1. Specification for packaged product only.

Note 2. Tested using environment of Figure 3b, 50Ω load CML output.

Note 3. Worst case difference between Q0 and Q1 from either A or B, when both outputs come from the same input

16-PIN EPAD-QSOP (Y16-1)



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