Integrated Circuit Systems, Inc.

ICS87949I-01

LOW SKEW ÷1, ÷2 LVCMOS / LVTTL CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS87949I-01 is a low skew, ÷1, ÷2 Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS87949I-01 has selectable single ended clock or LVPECL clock inputs. The single ended clock input accepts LVCMOS or LVTTL input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 15 to 30 by utilizing the ability of the outputs to drive two series terminated lines.

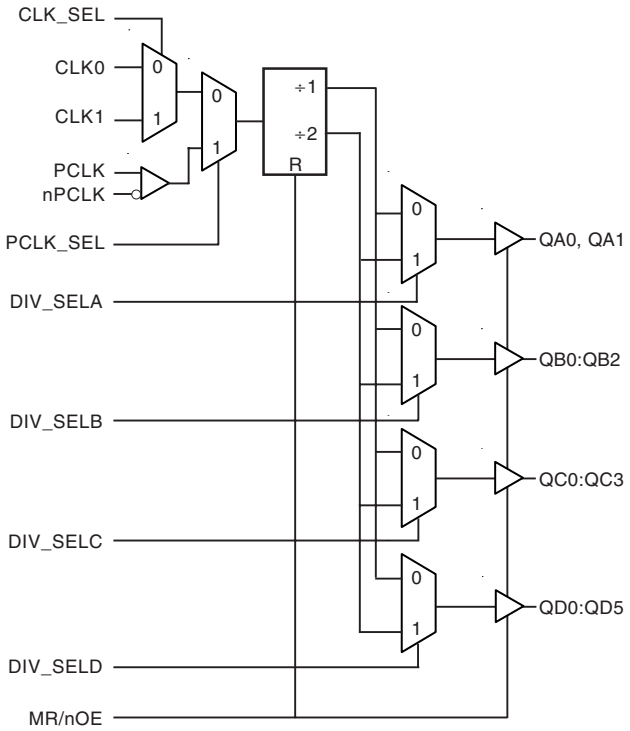
The divide select inputs, DIV_SELx, control the output frequency of each bank. The outputs can be utilized in the ÷1, ÷2 or a combination of ÷1 and ÷2 modes. The master reset input, MR/nOE, resets the internal frequency dividers and also controls the active and high impedance states of all outputs.

The ICS87949I-01 is characterized at 3.3V core/3.3V output and 3.3V core/2.5V output. Guaranteed bank, output and part-to-part skew characteristics make the ICS87949I-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

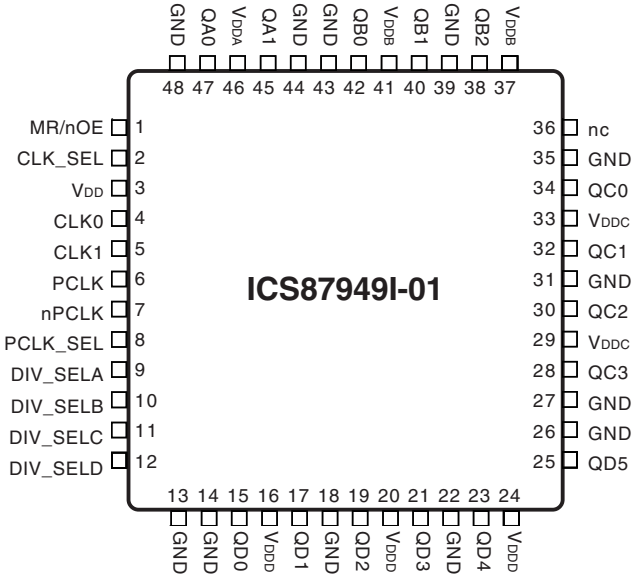
FEATURES

- 15 single ended LVCMOS/LVTTL outputs, 7Ω typical output impedance
- Selectable LVCMOS/LVTTL or LVPECL clock inputs
- CLK0 and CLK1 can accept the following input levels: LVCMOS and LVTTL
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Maximum input frequency: 250MHz
- Output skew: 250ps (maximum)
- Part-to-part skew: 1ns (maximum)
- Full 3.3V or mixed 3.3V core/2.5V output supply
- -40°C to 85°C ambient operating temperature
- Functionally compatible to the MPC949 in a smaller footprint requiring less board space

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	MR/nOE	Input	Pulldown	Active HIGH Master Reset. Active LOW output enable. When logic HIGH, the internal dividers are reset and the outputs are tri-stated (HiZ). When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
2	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1. When LOW, selects CLK0. LVCMOS / LVTTL interface levels.
3	V_{DD}	Power		Positive supply pin.
4, 5	CLK0, CLK1	Input	Pullup	LVCMOS / LVTTL clock inputs.
6	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
7	nPCLK	Input	Pullup	Inverting differential LVPECL clock input.
8	PCLK_SEL	Input	Pulldown	PCLK select input. LVCMOS / LVTTL interface levels.
9	DIV_SELA	Input	Pulldown	Controls frequency division for Bank A outputs. LVCMOS / LVTTL interface levels.
10	DIV_SELB	Input	Pulldown	Controls frequency division for Bank B outputs. LVCMOS / LVTTL interface levels.
11	DIV_SELC	Input	Pulldown	Controls frequency division for Bank C outputs. LVCMOS / LVTTL interface levels.
12	DIV_SELD	Input	Pulldown	Controls frequency division for Bank D outputs. LVCMOS / LVTTL interface levels.
13, 14, 18, 22, 26, 27, 31, 35, 39, 43, 44, 48	GND	Power		Power supply ground.
15, 17, 19 21, 23, 25	QD0, QD1, QD2, QD3, QD4, QD5	Output		Bank D outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
16, 20, 24,	V_{DDD}	Power		Positive supply pins for Bank D outputs.
28, 30, 32, 34	QC3, QC2, QC1, QC0	Output		Bank C outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
29, 33	V_{DDC}	Power		Positive supply pins for Bank C outputs.
36	nc	Unused		No connect.
37, 41	V_{DDB}	Power		Positive supply pins for Bank B outputs.
38, 40, 42	QB2, QB1, QB0	Output		Bank B outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
45, 47	QA1, QA0	Output		Bank A outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
46	V_{DDA}	Power		Positive supply pins for Bank A outputs.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
C_{PD}	Power Dissipation Capacitance (per output); NOTE 1	V_{DD}, V_{DDx} = 3.465V		23		pF
		V_{DD}, V_{DDx} = 2.625V		16		pF
R_{OUT}	Output Impedance		5	7	12	Ω

NOTE 1: V_{DDx} denotes V_{DDA}, V_{DDB}, V_{DDC}, V_{DDD}.

TABLE 3. FUNCTION TABLE

Inputs					Outputs			
MR/nOE	DIV_SELA	DIV_SELB	DIV_SELC	DIV_SELD	QA0:QA1	QB0:QB2	QC0:QC3	QD0:QD5
1	X	X	X	X	Hi Z	Hi Z	Hi Z	Hi Z
0	0	X	X	X	fIN/1	Active	Active	Active
0	1	X	X	X	fIN/2	Active	Active	Active
0	X	0	X	X	Active	fIN/1	Active	Active
0	X	1	X	X	Active	fIN/2	Active	Active
0	X	X	0	X	Active	Active	fIN/1	Active
0	X	X	1	X	Active	Active	fIN/2	Active
0	X	X	X	0	Active	Active	Active	fIN/1
0	X	X	X	1	Active	Active	Active	fIN/2

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDx}$ = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDx}	Output Supply Voltage; NOTE 1		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				60	mA
I_{DDx}	Output Supply Current; NOTE 2				20	mA

NOTE 1: V_{DDx} denotes V_{DDA}, V_{DDB}, V_{DDC}, V_{DDD}.
NOTE 2: I_{DDx} denotes I_{DDA}, I_{DDB}, I_{DDC}, I_{DDD}.

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDx}$ = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	DIV_SELA:DIV_SELD, CLK_SEL, PCLK_SEL, MR/nOE		2		V_{DD} + 0.3	V
		CLK0, CLK1		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	DIV_SELA:DIV_SELD, CLK_SEL, PCLK_SEL, MR/nOE		-0.3		0.8	V
		CLK0, CLK1		-0.3		1.3	V
I_{IH}	Input High Current	DIV_SELA:DIV_SELD, CLK_SEL, PCLK_SEL, MR/nOE	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		CLK0, CLK1	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	DIV_SELA: DIV_SELD, CLK_SEL, PCLK_SEL, MR/nOE	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		CLK0, CLK1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1			2.6			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDx}/2. See Parameter Measurement Section, 3.3V Output Load Test Circuit.

TABLE 4C. LVPECL DC CHARACTERISTICS, $V_{DD} = V_{DDx}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nPCLK	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	PCLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nPCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.3		1	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 1.5		V_{DD}	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLK and nPCLK is V_{DD} + 0.3V.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDx}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Input Frequency				250	MHz
t_{PD}	Propagation Delay, NOTE 1		2.1		5	ns
*t*sk(b)	Bank Skew; NOTE 2, 6	Measured on rising edge at V_{DDx}/2			100	ps
*t*sk(o)	Output Skew; NOTE 3, 6	Measured on rising edge at V_{DDx}/2			300	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6	Measured on rising edge at V_{DDx}/2			1	ns
t_R/ t_F	Output Rise/Fall Time; NOTE 5	20% to 80%	400		950	ps
odc	Output Duty Cycle	Measured with outputs in ÷1	40		60	%
t_{EN}	Output Enable Time;NOTE 5	f = 10MHz			5	ns
t_{DIS}	Output Disable Time;NOTE 5	f = 10MHz			5	ns

All parameters measured at ≤ 250MHz unless noted otherwise.
NOTE 1: Measured from the V_{DD}/2 of the input to V_{DDx}/2 of the output.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions. Measured at V_{DDx}/2.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDx}/2.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4D. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDx} = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDx}	Output Supply Voltage; NOTE 1		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				60	mA
I_{DDx}	Output Supply Current; NOTE 2				20	mA

NOTE 1: V_{DDx} denotes V_{DDA}, V_{DDB}, V_{DDC}, V_{DDD}.
NOTE 2: I_{DDx} denotes I_{DDA}, I_{DDB}, I_{DDC}, I_{DDD}.

TABLE 4E. LVCMOS/LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDx} = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	DIV_SELA:DIV_SELD, CLK_SEL, PCLK_SEL, MR/nOE		2		V_{DD} + 0.3	V
		CLK0, CLK1		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	DIV_SELA:DIV_SELD, CLK_SEL, PCLK_SEL, MR/nOE		-0.3		0.8	V
		CLK0, CLK1		-0.3		1.3	V
I_{IH}	Input High Current	DIV_SELA:DIV_SELD, CLK_SEL, PCLK_SEL, MR/nOE	V_{DD} = V_{IN} = 3.465V			150	µA
		CLK0, CLK1	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	DIV_SELA:DIV_SELD, CLK_SEL, PCLK_SEL, MR/nOE	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		CLK0, CLK1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1			1.8			V
V_{OL}	Output Low Voltage; NOTE 1					0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDx}/2. See Parameter Measurement Section, 3.3V/2.5V Output Load Test Circuit.

TABLE 4F. LVPECL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDx} = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK	V_{DD} = V_{IN} = 3.465V			150	µA
		nPCLK	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	PCLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nPCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.3		1	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 1.5		V_{DD}	V

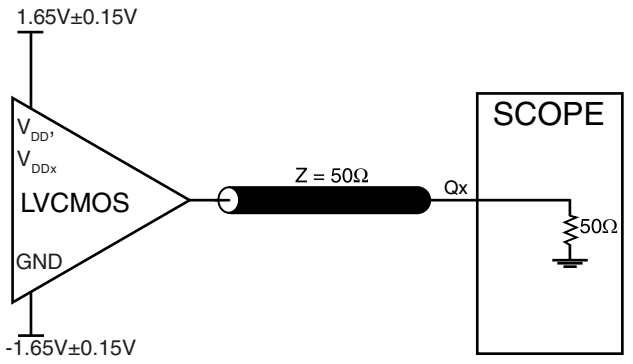
NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLK and nPCLK is V_{DD} + 0.3V.

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDx} = 2.5V±5%, T_A = -40°C TO 85°C

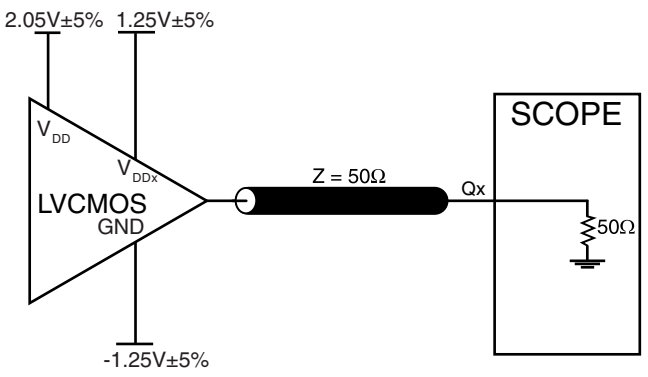
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Input Frequency				250	MHz
t_{PD}	Propagation Delay, NOTE 1		2.0		4.6	ns
*t*sk(b)	Bank Skew; NOTE 2, 6	Measured on rising edge at V_{DDx}/2			65	ps
*t*sk(o)	Output Skew; NOTE 3, 6	Measured on rising edge at V_{DDx}/2			250	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6	Measured on rising edge at V_{DDx}/2			1	ns
t_R/ t_F	Output Rise/Fall Time; NOTE 5	20% to 80%	400		950	ps
odc	Output Duty Cycle	Measured with outputs in ÷1	40		60	%
t_{EN}	Output Enable Time;NOTE 5	f = 10MHz			5	ns
t_{DIS}	Output Disable Time;NOTE 5	f = 10MHz			5	ns

All parameters measured at ≤ 250MHz unless noted otherwise.
NOTE 1: Measured from the V_{DD}/2 of the input to V_{DDx}/2 of the output.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions. Measured at V_{DDx}/2.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDx}/2.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

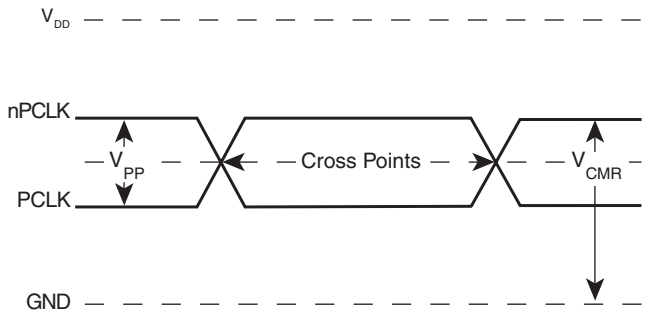
PARAMETER MEASUREMENT INFORMATION



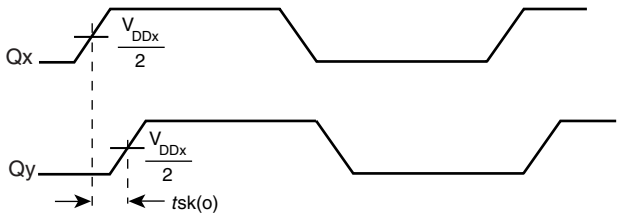
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



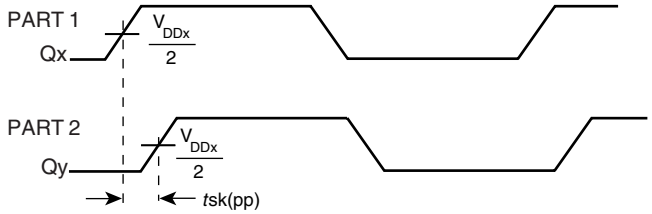
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



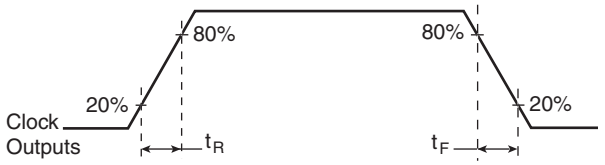
DIFFERENTIAL INPUT LEVEL



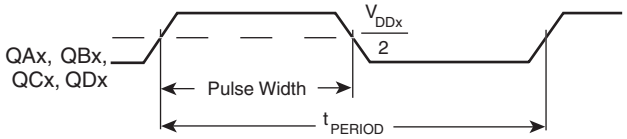
OUTPUT SKEW



PART-TO-PART SKEW

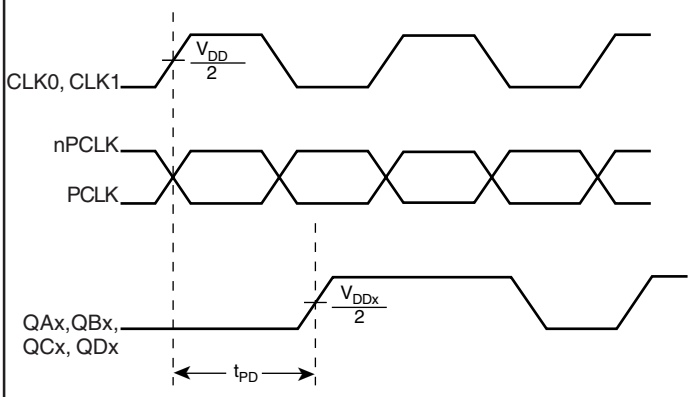


OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



PROPAGATION DELAY

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

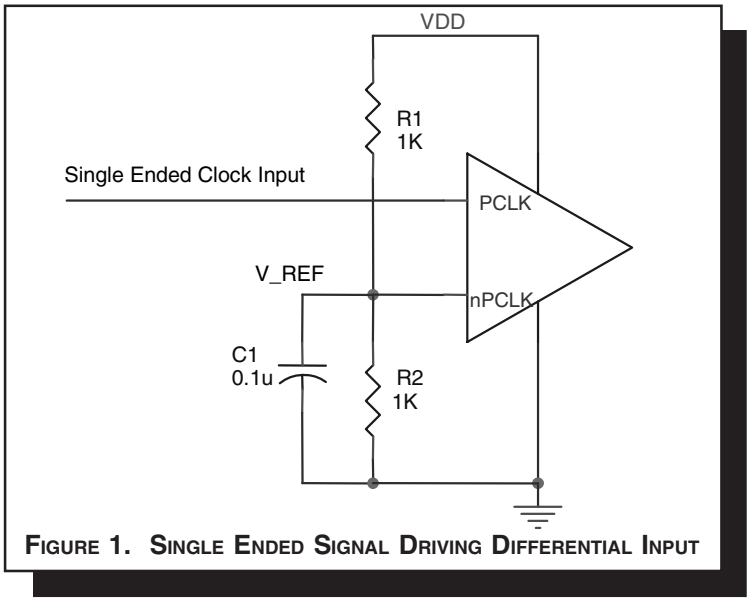


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3D* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

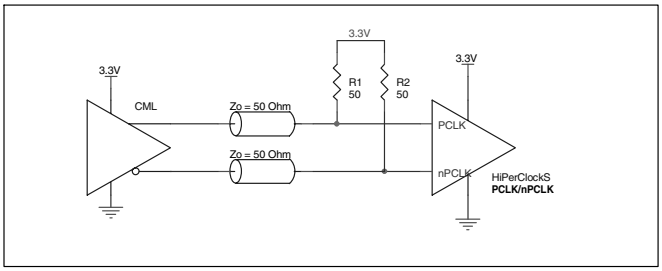


FIGURE 3A. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A CML DRIVER

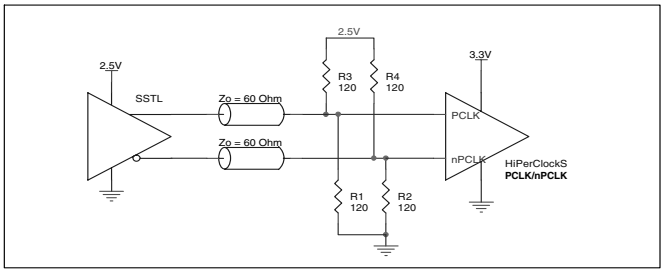


FIGURE 3B. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY AN SSTL DRIVER

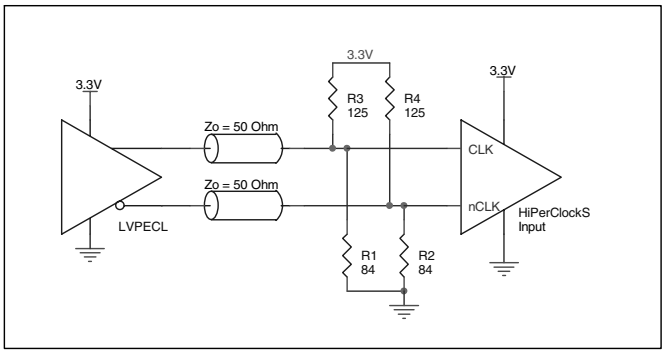


FIGURE 3C. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

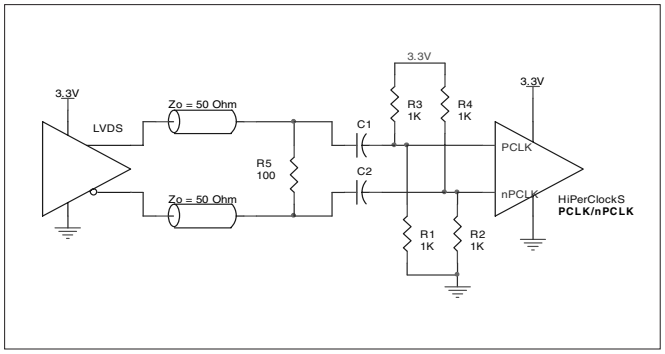


FIGURE 3D. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

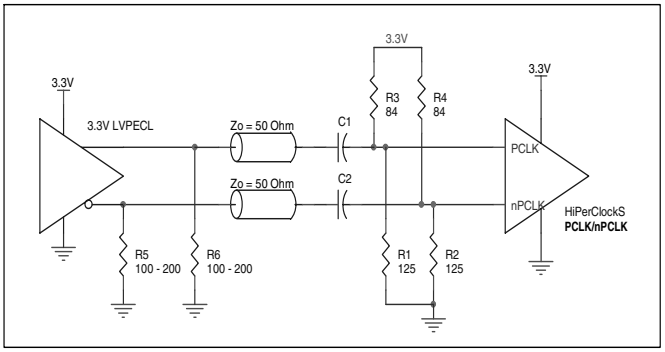


FIGURE 3E. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

SCHEMATIC EXAMPLE

This application note provides general design guide using ICS87949I-01 LVCMOS buffer. *Figure 4* shows a schematic example of the ICS87949I-01 LVCMOS clock buffer. In this example, the input is driven by an LVCMOS driver.

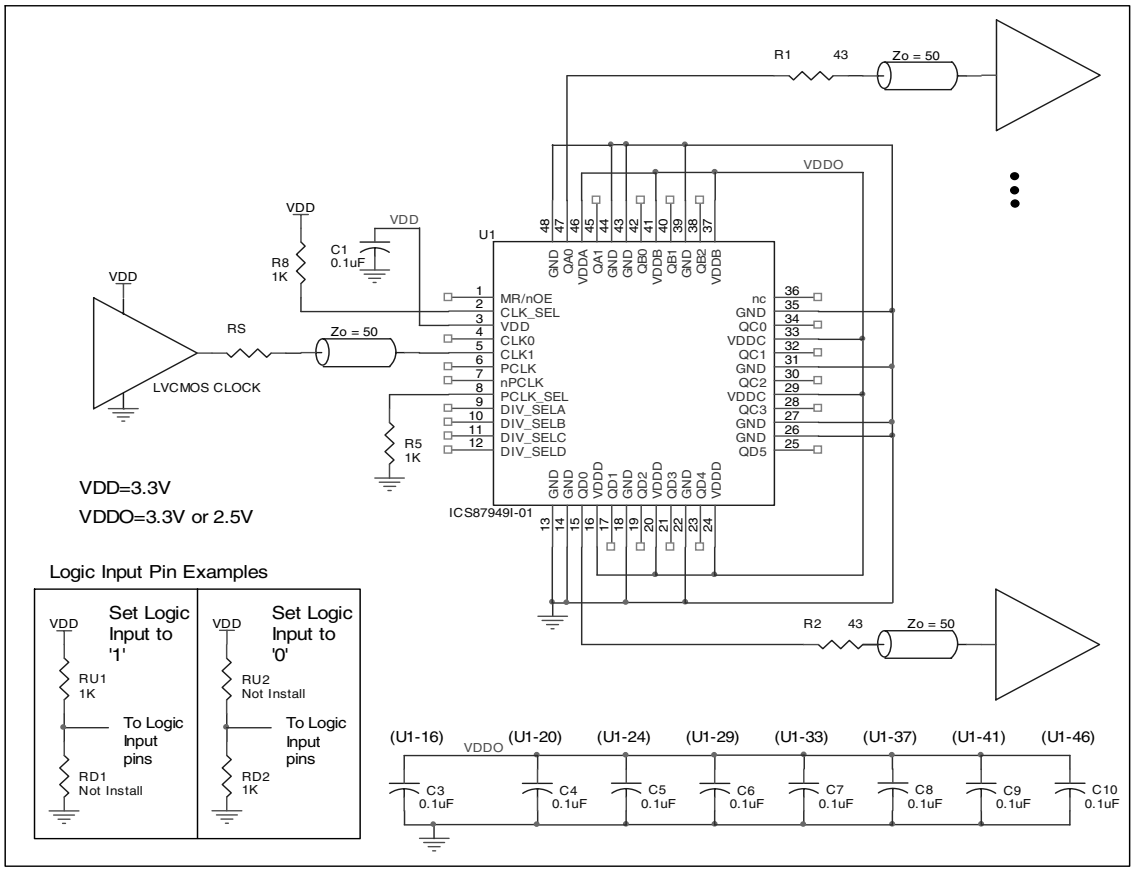


FIGURE 4. EXAMPLE ICS87949I-01 LVCMOS CLOCK OUTPUT BUFFER SCHEMATIC

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 48 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87949I-01 is: 1545

PACKAGE OUTLINE - Y SUFFIX FOR 48 LEAD LQFP

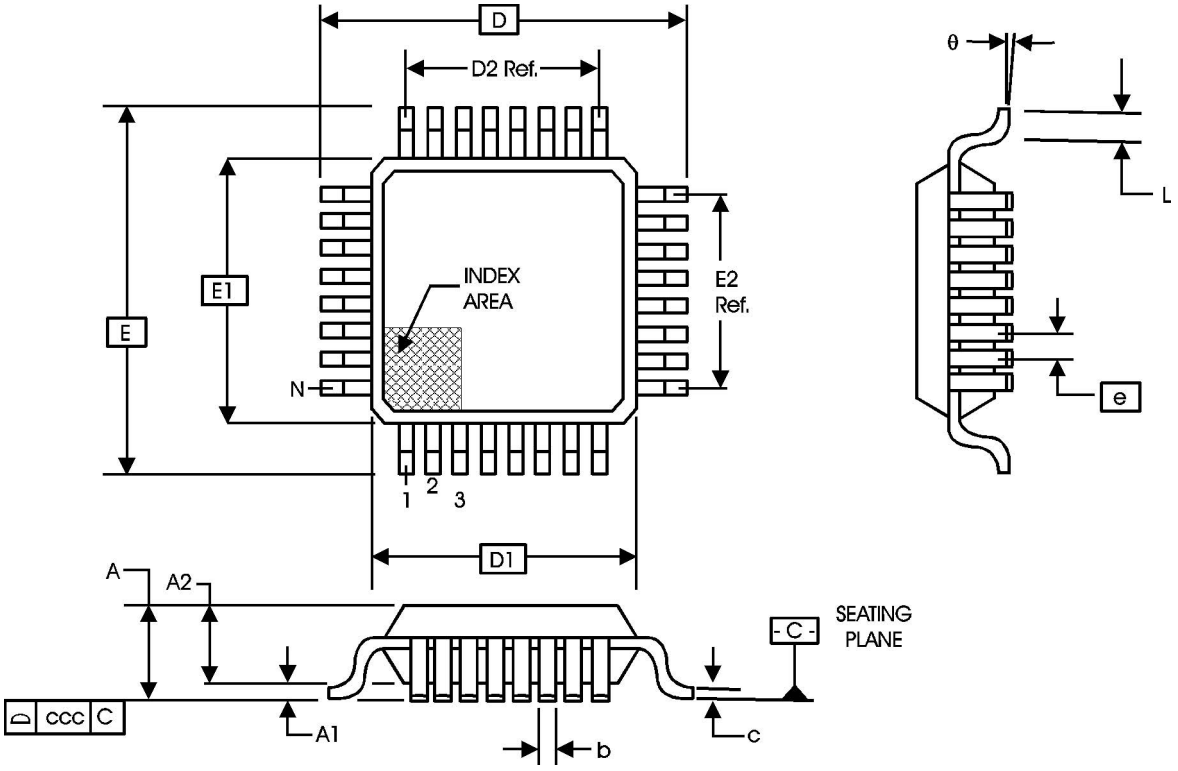


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N		48	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS87949AYI-01	ICS87949AYI01	48 Lead LQFP	250 per tray	-40°C to 85°C
ICS87949AYI-01T	ICS87949AYI01	48 Lead LQFP on Tape and Reel	1000	-40°C to 85°C