Integrated Circuit Systems, Inc.

ICS9148-25

Pentium/Pro™ System and Cyrix™ Clock Chip

General Description

The **ICS9148-25** is a Clock Synthesizer chip for Pentium and PentiumPro plus Cyrix CPU based Desktop/Notebook systems that will provide all necessary clock timing.

Features include four CPU, seven PCI and eight SDRAM clocks. Two reference outputs are available equal to the crystal frequency, plus the IOAPIC output powered by VDDL. Additionally, the device meets the Pentium power-up stabilization, which requires that CPU and PCI clocks be stable within 2ms after power-up.

High drive PCICLK and SDRAM outputs typically provide greater than 1 V/ns slew rate into 30pF loads. CPUCLK outputs typically provide better than 1V/ns slew rate into 20pF loads while maintaining 50 ±5% duty cycle. The REF clock outputs typically provide better than 0.5V/ns slew rates.

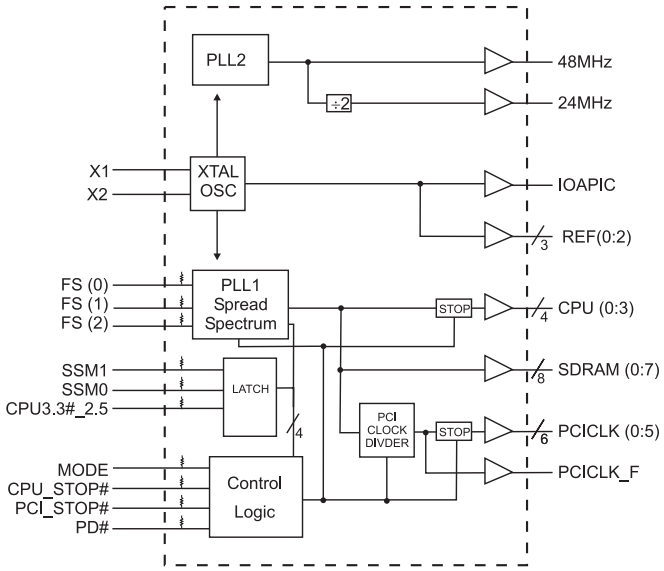
The **ICS9148-25** accepts a 14.318MHz reference crystal or clock as its input and runs on a 3.3V supply.

Sperad Spectrum is modulated in center-spread mode on CPU/SDRAM/PCI clocks. Modulation amount is selectable at power-up (latched inputs) for ±0.5, ±1.0, ±2.0 or No spreading.

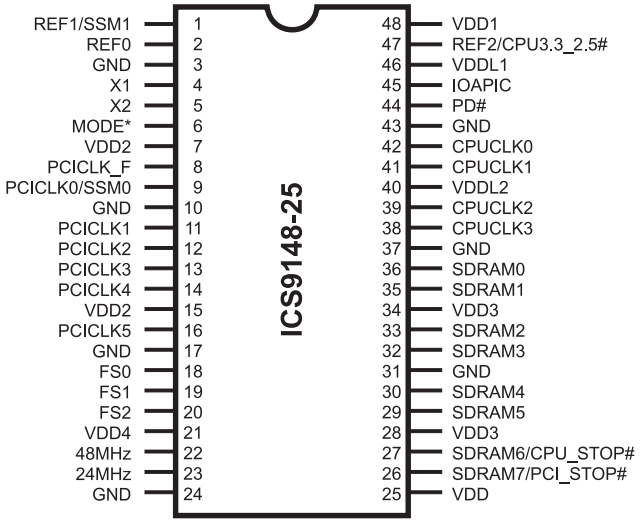
Features

- Generates system clocks for CPU, IOAPIC, SDRAM, PCI, plus 14.318 MHz), USB, Plus Super I/O
- Spread spectrum for CPU/SDRAM/PCI clocks default
- Supports single or dual processor systems
- Modulation of Spread Spectrum selectable as ±0.5, ±1.0, ±2.0 or none
- Supports Intel 60, 66.8MHz, Cyrix 55, 75MHz plus 83.3 and 68MHz (Turbo of 66.6) speeds.
- Synchronous clocks skew matched to 250ps window on CPU, SDRAM and 500ps window on PCI clocks
- CPU clocks to PCI clocks skew 1-4ns (CPU early)
- MODE input pin selects optional power management input control pins
- Two fixed outputs, 48MHz and 24 MHz
- Separate 2.5V and 3.3V supply pins
  - 2.5V or 3.3V output: CPU, IOAPIC (Strength selectable)
  - 3.3V outputs: SDRAM, PCI, REF, 48/24 MHz
- No power supply sequence requirements
- 48 pin 300 mil SSOP

Block Diagram



Pin Configuration



48-Pin SSOP

Power Groups

VDD = Supply for PLL core.
VDD1 = REF (0:2), X1, X2
VDD2 = PCICLK_F, PCICLK (0:5)
VDD3 = SDRAM (0:5), SDRAM6/CPU_STOP#, SDRAM7/PCI_STOP#
VDD4 = 48MHz, 24MHz
VDDL1 = IOAPIC
VDDL2 = CPUCLK (0:3)

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Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	SSM1	IN	Latched input for Spread Spectrum modulation amount (see table)*
	REF1	OUT	Reference clock output
2	REF0	OUT	Reference clock output
3, 10, 17, 24, 31, 37, 43	GND	PWR	Ground (common)
4	X1	IN	Crystal or reference input, nominally 14.318 MHz. Includes internal load cap to GND and feedback resistor from X2.
5	X2	OUT	Crystal output, includes internal load cap to GND.
6	MODE	IN	Input function selection for Power Management pins*
7,15	VDD2	PWR	Supply for PCICLK_F, and PCICLK (0:5)
8	PCICLK_F	OUT	Free running PCI clock, not affected by PCI_STOP#
9	PCICLK0	OUT	PCI clocks
	SSM0	IN	Latched input for Spread Spectrum modulation amount (see table)*
11, 12, 13, 14, 16	PCI_CLK (1:5)	OUT	PCI clocks
18	FS0	IN	Frequency select 0 input*
19	FS1	IN	Frequency select 1 input*
20	FS2	IN	Frequency select 2 input*
21	VDD4	PWR	Supply for 48MHz and 24MHz clocks
22	48MHz	OUT	48MHz driver output for USB clock
23	24MHz	OUT	24MHz driver output for Super I/O
25	VDD	PWR	Supply for PLL core
26	SDRAM7	OUT	SDRAM clock
	PCI_STOP#	IN	Halts PCI Bus (0:5) at next logic "0" level when low*
27	SDRAM6	OUT	SDRAM clock
	CPU_STOP#	IN	Halts CPU clocks at next logic "0" level when low*
28,34	VDD3	PWR	Supply for SDRAM (0:5), SDRAM6/CPU_STOP#, SDRAM7/PCI_STOP
29, 30, 32, 33, 35, 36	SDRAM (0:5)	OUT	SDRAMs clock at CPU speed
38, 39, 41, 42	CPUCLK (0:3)	OUT	CPUCLK clock output, powered by VDDL2
40	VDD2	PWR	Supply for CPUCLK (0:3)
44	PD#	IN	Powers down chip, active low*
45	IOAPIC	OUT	IOAPIC clock output, powered by VDDL1, at crystal frequency
46	VDDL1	PWR	Supply for IOAPIC
47	CPU3.3_2.5#	IN	Latched 3.3 or 2.5 VDD buffer strength selection* (see table)
	REF2	OUT	Reference clock output
48	VDD1	PWR	Supply for REF (0:2), X1, X2

*Internal pull-up resistor of 120 to 150K to 3.3V on indicated inputs.

Functionality

V_{DD} = 3.3V ±5% V_{DDL} = 2.5V ±5% or 3.3V ±5%, T_A = 0 to 70°C
Crystal (X1, X2) = 14.31818 MHz

FS2	FS1	FS0	CPUCLK, SDRAM (MHz)	PCICLK (MHz)
0	0	0	83.3	1/2 CPU
0	0	1	75	30 (CPU/2.5)
0	1	0	83.3	33.3 (CPU/2.5)
0	1	1	68.5	1/2 CPU
1	0	0	55	1/2 CPU
1	0	1	75	1/2 CPU
1	1	0	60	1/2 CPU
1	1	1	66.8	1/2 CPU

Mode Pin - Power Management Input Control

MODE, Pin 6	Pin 26	Pin 27
0	PCI_STOP# Input	CPU_STOP# Input
1	SDRAM7 Output	SDRAM 6 Output

Power Management Functionality

CPU_STOP#	PCI_STOP#	PD#	CPUCLK Outputs	PCICLK(0:5) Outputs	PCICLK_F, REF, 24/48MHz and SDRAM	Crystal OSC	VCO
X	X	0	Stopped Low	Stopped Low	Stopped Low	Off	Off
0	0	1	Stopped Low	Stopped Low	Running	Running	Running
0	1	1	Stopped Low	Running	Running	Running	Running
1	0	1	Running	Stopped Low	Running	Running	Running
1	1	1	Running	Running	Running	Running	Running

Spread Spectrum Functionality

Latched Pin 1 SSM1	Latched Pin 9 SSM0	CPU, SDRAM and PCICLOCKS	REF, IOAPIC	24MHz	48MHz
0	0	Normal, steady frequency mode	14.318MHz	24MHz	48MHz
0	1	Frequency modulated in center spread ±2.0%	14.318MHz	24MHz	48MHz
1	0	Frequency modulated in center spread ±1.0%	14.318MHz	24MHz	48MHz
1*	1*	Frequency modulated in center spread ±0.5%	14.318MHz	24MHz	48MHz

*default with internal pull-ups

CPU 3.3_2.5V Buffer selector for CPUCLK and IOAPIC drivers.

CPU3.3_2.5# Latched Input Level	Buffer Selected for Operation at:
0	2.5V VDD
1	3.3V VDD

Technical Pin Function Descriptions

VDD(1,2,3,4)
This is the power supply to the internal core logic of the device as well as the clock output buffers for REF(0:1), PCICLK, 48/24MHzA/B and SDRAM(0:7).

This pin operates at 3.3V volts. Clocks from the listed buffers that it supplies will have a voltage swing from Ground to this level. For the actual guaranteed high and low voltage levels for the Clocks, please consult the DC parameter table in this data sheet.

VDDL1,2
This is the power supplies for the CPUCLK and IOAPCI output buffers. The voltage level for these outputs may be 2.5 or 3.3volts. Clocks from the buffers that each supplies will have a voltage swing from Ground to this level. For the actual Guaranteed high and low voltage levels of these Clocks, please consult the DC parameter table in this Data Sheet. See control pin CPUCLK3.3_2.5# for output buffer strength matching VDDL required for skew control.

GND
This is the power supply ground (common or negative) return pin for the internal core logic and all the output buffers.

X1
This input pin serves one of two functions. When the device is used with a Crystal, X1 acts as the input pin for the reference signal that comes from the discrete crystal. When the device is driven by an external clock signal, X1 is the device input pin for that reference clock. This pin also implements an internal Crystal loading capacitor that is connected to ground. See the data tables for the value of this capacitor. Also includes feedback resistor from X2.

X2
This Output pin is used only when the device uses a Crystal as the reference frequency source. In this mode of operation, X2 is an output signal that drives (or excites) the discrete Crystal. The X2 pin will also implement an internal Crystal loading capacitor that is connected to ground. See the Data Sheet for the value of this capacitor.

CPUCLK (0:3)
These Output pins are the Clock Outputs that drive processor and other CPU related circuitry that requires clocks which are in tight skew tolerance with the CPU clock. The voltage swing of these Clocks are controlled by the Voltage level applied to the VDDL2 pin of the device. See the Functionality Table for a list of the specific frequencies that are available for these Clocks and the selection codes to produce them. See control pin CPUCLK3.3_2.5# for output buffer strength matching VDDL required for CPU to SDRAM skew control. These clocks are modulated by Sperad Spectrum.

SDRAM(0:7)
These Output Clocks are use to drive Dynamic RAM's and are low skew copies of the CPU Clocks. The voltage swing of the SDRAM's output is controlled by the supply voltage that is applied to VDD3 of the device, operates at 3.3 volts. These clocks are modulated by Sperad Spectrum.

48MHz
This is a fixed frequency Clock output at 48MHz that is typically used to drive USB devices.

24MHz
This pin is a fixed frequency clock output typically used to drive Super I/O devices.

IOAPIC
This Output is a fixed frequency Output Clock that runs at the Reference Input (typically 14.31818MHz) . Its voltage level swing is controlled by VDDL1 and may operate at 2.5 or 3.3volts.

REF(0:2)
The REF Outputs are fixed frequency Clocks that run at the same frequency as the Input Reference Clock X1 or the Crystal (typically 14.31818MHz) attached across X1 and X2.

PCICLK_F
This Output is equal to PCICLK(0:5) and is FREE RUNNING, and will not be stopped by PCI_STP#. This clock is modulated by Spread Spectrum.

PCICLK (0:5)
These Output Clocks generate all the PCI timing requirements for a Pentium/Pro based system. They conform to the current PCI specification. They run at 1/2 CPU frequency, or CPU/2.5, see frequency table. These clocks are modulated by Sperad Spectrum.

FS (0,1,2)
These Input pins control the frequency of the Clocks at the CPU, PCICLK and SDRAM output pins. See frequency table. These pins are all Full-time inputs with a pull-up to VDD.

MODE
This Input pin is used to select the Input function of the Power Management I/O pins 26 and 27. An active Low will place pins in the Input mode and enable those stop clock functions. This pin is a full-time input with a pull-up to VDD.

Technical Pin Function Descriptions

CPU3.3_2.5#
This Input pin controls the CPU and IOAPIC output buffer strength for skew matching CPU and SDRAM outputs to compensate for the external VDDL supply condition. It is important to use this function when selecting power supply requirements for VDDL1,2. A logic "0" (ground) will indicate 2.5V operation and a logic "1" will indicate 3.3V operation. This pin has an internal pull-up to VDD. This pin is a latched input.

PD#
This is an asynchronous active Low Input pin used to Power Down the device into a Low Power state by not removing the power supply. The internal Clocks are disabled and the VCO and Crystal are stopped. Powered Down will also place all the Outputs in a low state at the end of their current cycle. The latency of Power Down will not be greater than 3ms. This pin is a Full-time input with a pull-up to VDD.

CPU_STOP#
This is a active Low Input pin used to stop the CPUCLK clocks in an active low state. All other clocks will continue to run while this function is enabled. The CPUCLK's will have a turn OFF latency and a turn ON latency of 2 or 3 CPU clocks. This pin is a Full-time input with a pull-up to VDD.

PCI_STOP#
This is a synchronous active Low Input pin used to stop the PCICLK (0:5) clocks in a low state. It will not effect PCICLK_F or any other outputs. There is only one full PCI clock output for Turn OFF or Turn ON latency. This pin is a Full-time input with a pull-up to VDD.

SSM (0:1)
These pins define the input condition for the Spread Spectrum amount of modulation. See Spread Spectrum functionality table. Note that spreading is only done on the CPU/SDRAM/ PCI clocks no modulation is done on the REF, IOAPIC or PLL2 (24, 48MHz) outputs.

These latched input pins are defined at power-on for logic Hi or logic Low condition by external pull-up or pull-down resistors, or the internal pull-up resistor to VDD. See shared pin operation of Input/output pins on next page.

Shared Pin Operation - Input/Output Pins

Pins 1, 9 & 47 on the **ICS9148-25** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 4-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm(10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period. There is no degradation to the output clocks from resistors as low as 2K ohm. The internal pull-up resistors can be used as the logic high program input.

Figs. 1 and 2 show the recommended means of implementing this function. In Fig. 1 either one of the resistors is loaded onto the board (selective stuffing) to configure the device's internal logic. Figs. 2a and b provide a single resistor loading option where either solder spot tabs or a physical jumper header may be used.

These figures illustrate the optimal PCB physical layout options. These configuration resistors are of such a large ohmic value that they do not effect the low impedance clock signals. The layouts have been optimized to provide as little impedance transition to the clock signal as possible, as it passes through the programming resistor pad(s).

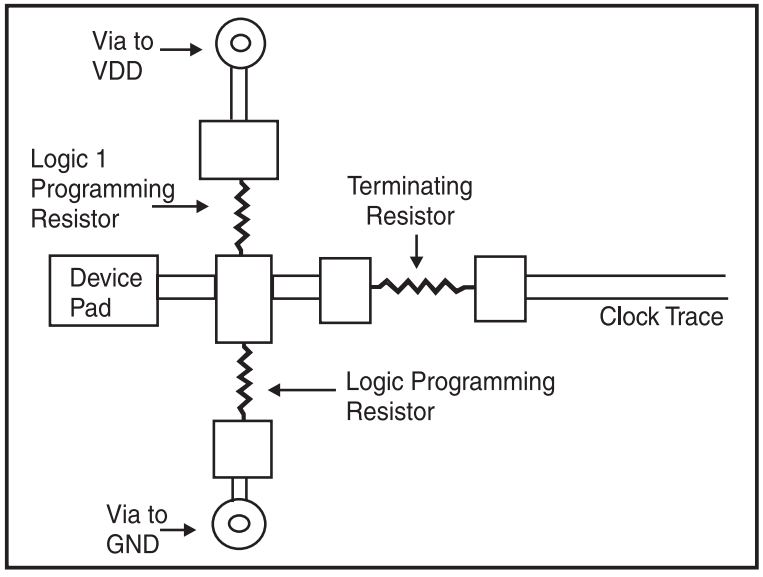


Fig. 1

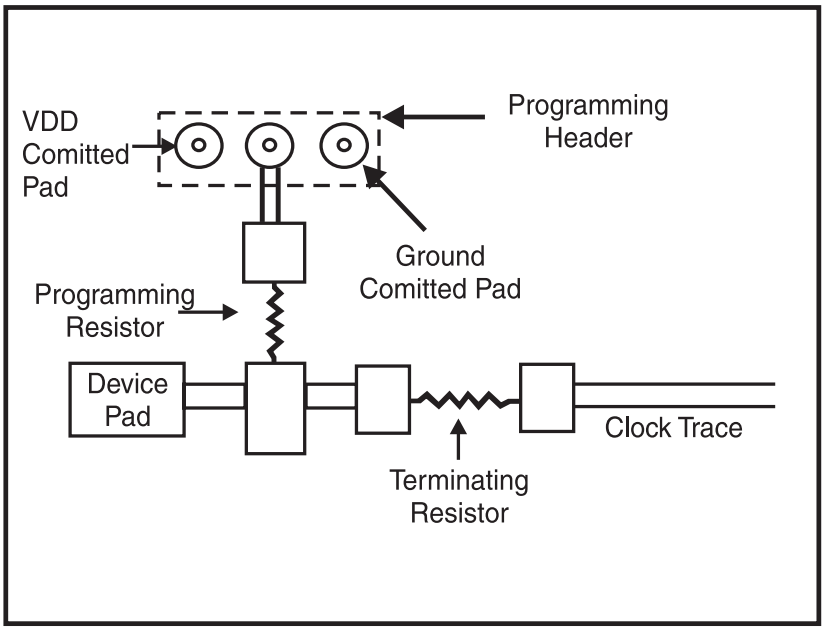

VDD
Comitted
Pad
Programming
Header
Ground
Comitted Pad
Programming
Resistor
Device
Pad
Clock Trace
Terminating
Resistor

Fig. 2a

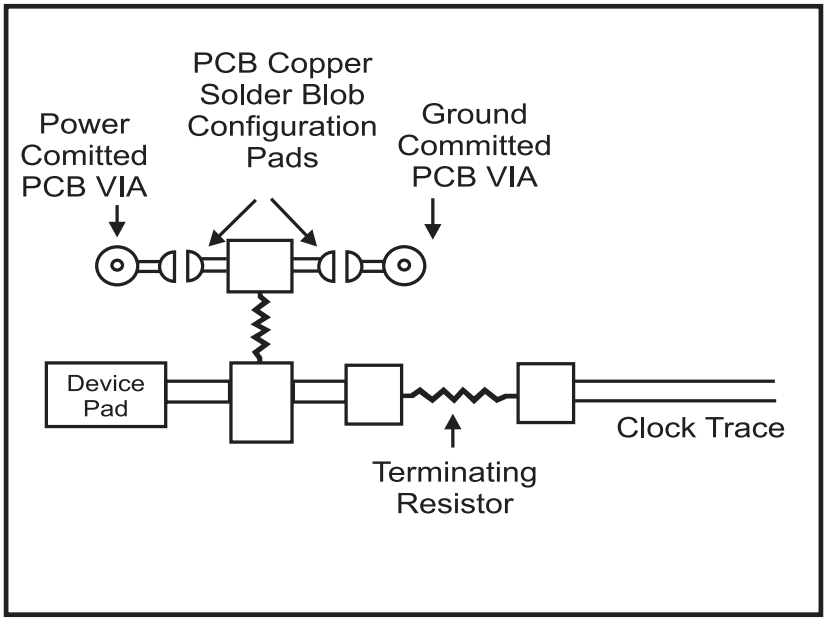

PCB Copper
Solder Blob
Configuration
Pads
Power
Comitted
PCB VIA
Ground
Committed
PCB VIA
Device
Pad
Clock Trace
Terminating
Resistor

Fig. 2b

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}		0.1	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; Select @ 66M		75	95	mA
Power Down Supply Current	$I_{DD3.3PD}$	C_L = 0 pF; With input address to Vdd or GND		8	600	µA
Input frequency	F_i	V_{DD} = 3.3 V;		14.318		MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	ms
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.		5		ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$T_{CPU-SDRAM1}$	V_T = 1.5 V		200	500	ps
	$T_{CPU-PCI1}$	V_T = 1.5 V;	1	2	4.5	ns
	$T_{REF-IOAPIC}$	V_T = 1.5 V;		900		ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5OP}$	C_L = 0 pF; Select @ 66M		8	9.5	mA
Skew[1]	$T_{CPU-SDRAM2}$	V_T = 1.5 V; V_{TL} = 1.25 V; SDRAM Leads		250	500	ps
	$T_{REF-IOAPIC}$	V_T = 1.5 V; V_{TL} = 1.25 V; SDRAM Leads		260		ps
	$T_{CPU-PCI2}$	V_T = 1.5 V; V_{TL} = 1.25 V; CPU Leads	1	2	4	ns

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O = V_{DD}*(0.5)$	10		25	Ω
Output Impedance	R_{DSN2B}[1]	$V_O = V_{DD}*(0.5)$	10		25	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -13.0 mA	2	2.2		V
Output Low Voltage	V_{OL2B}	I_{OL} = 14 mA		0.3	0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V		-25	-16	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	22	26		mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.35	1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.2	1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	50	55	ns
Skew	t_{sk2B}[1]	V_T = 1.25 V		60	250	ps
Jitter	$t_{jcyc-cyc2B}$[1]	V_T = 1.25 V		150	250	ps
	t_{j1s2B}[1]	V_T = 1.25 V		30	150	ps
	t_{jabs2B}[1]	V_T = 1.25 V	-250	80	+250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.6	3.1		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.15	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-62	-40	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	40	55		mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.5	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.4	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	50	60	%
Skew	t_{sk1}[1]	V_T = 1.5 V		200	500	ps
Jitter	t_{j1s1}[1]	V_T = 1.5 V		10	150	ps
	t_{jabs1}[1]	V_T = 1.5 V	-250	65	250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 - 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP3}[1]	V_O = V_{DD}*(0.5)	10		24	Ω
Output Impedance	R_{DSN3}[1]	V_O = V_{DD}*(0.5)	10		24	Ω
Output High Voltage	V_{OH3}	I_{OH} = -30 mA	2.6	2.8		V
Output Low Voltage	V_{OL3}	I_{OL} = 23 mA		0.3	0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V		-62	-40	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8 V	40	55		mA
Rise Time	T_{r3}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.5	2	ns
Fall Time	T_{f3}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.4	2	ns
Duty Cycle	D_{t3}[1]	V_T = 1.5 V	45	50	60	%
Skew	T_{sk3}[1]	V_T = 1.5 V		200	500	ps
Jitter	T_{j1s3}[1]	V_T = 1.5 V		50	150	ps
	T_{jabs3}[1]	V_T = 1.5 V	-250	100	250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP4B}[1]	V_O = V_{DD}*(0.5)	10		30	Ω
Output Impedance	R_{DSN4B}[1]	V_O = V_{DD}*(0.5)	10		30	Ω
Output High Voltage	$V_{OH4\B}$	I_{OH} = -8 mA	2	2.5		V
Output Low Voltage	V_{OL4B}	I_{OL} = 12 mA		0.3	0.5	V
Output High Current	I_{OH4B}	V_{OH} = 1.7 V		-25	-16	mA
Output Low Current	I_{OL4B}	V_{OL} = 0.7 V	19	23		mA
Rise Time	t_{r4B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.4	1.6	ns
Fall Time	t_{f4B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.2	1.6	ns
Duty Cycle	d_{t4B}[1]	V_T = 1.25 V	40	53	60	%
Jitter	$t_{jcyc-cyc4B}$[1]	V_T = 1.25 V		1400		ps
	t_{j1s4B}[1]	V_T = 1.25 V		300	400	ps
	t_{jabs4B}[1]	V_T = 1.25 V	-1000	800	1000	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics-REF1, 48MHz, & 24MHz

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 - 45 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP7}	V_O = V_{DD}*(0.5)	10		24	Ω
Output Impedance	R_{DSN7}	V_O = V_{DD}*(0.5)	10		24	Ω
Output High Voltage	V_{OH7}	I_{OH} = -30 mA	2.6	2.75		V
Output Low Voltage	V_{OL7}	I_{OL} = 23 mA		0.3	0.4	V
Output High Current	I_{OH7}	V_{OH} = 2.0 V		-62	-40	mA
Output Low Current	I_{OL7}	V_{OL} = 0.8 V	40	50		mA
Rise Time	T_{r7}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.4	2	ns
Fall Time	T_{f7}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.4	2	ns
Duty Cycle	D_{t7}[1]	V_T = 1.5 V	45	54	55	%
Jitter	$t_{jcyc-cyc7}$[1]	V_T = 1.5 V		1400		ps
	T_{j1s7}[1]	V_T = 1.5 V		210	400	ps
	T_{jabs7}[1]	V_T = 1.5 V	-1000	450	1000	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - REF0

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 - 45 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP7}	V_O = V_{DD}*(0.5)	10		24	Ω
Output Impedance	R_{DSN7}	V_O = V_{DD}*(0.5)	10		24	Ω
Output High Voltage	V_{OH7}	I_{OH} = -30 mA	2.6	2.75		V
Output Low Voltage	V_{OL7}	I_{OL} = 23 mA		0.3	0.4	V
Output High Current	I_{OH7}	V_{OH} = 2.0 V		-62	-54	mA
Output Low Current	I_{OL7}	V_{OL} = 0.8 V	41	50		mA
Rise Time	T_{r7}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.8	2.2	ns
Fall Time	T_{f7}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.8	2.2	ns
Duty Cycle	D_{t7}[1]	V_T = 1.5 V	40	54	60	%
Jitter	$t_{jcyc-cyc7}$[1]	V_T = 1.5 V		1400		ps
	T_{j1s7}[1]	V_T = 1.5 V		350	400	ps
	T_{jabs7}[1]	V_T = 1.5 V	-1000	900	1000	ps

[1]Guarenteed by design, not 100% tested in production.

General Layout Precautions:

1) Use a ground plane on the top layer of the PCB in all areas not used by traces.

2) Make all power traces and vias as wide as possible to lower inductance.

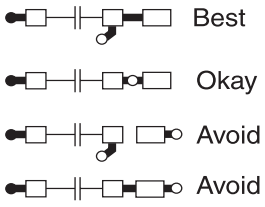
Notes:

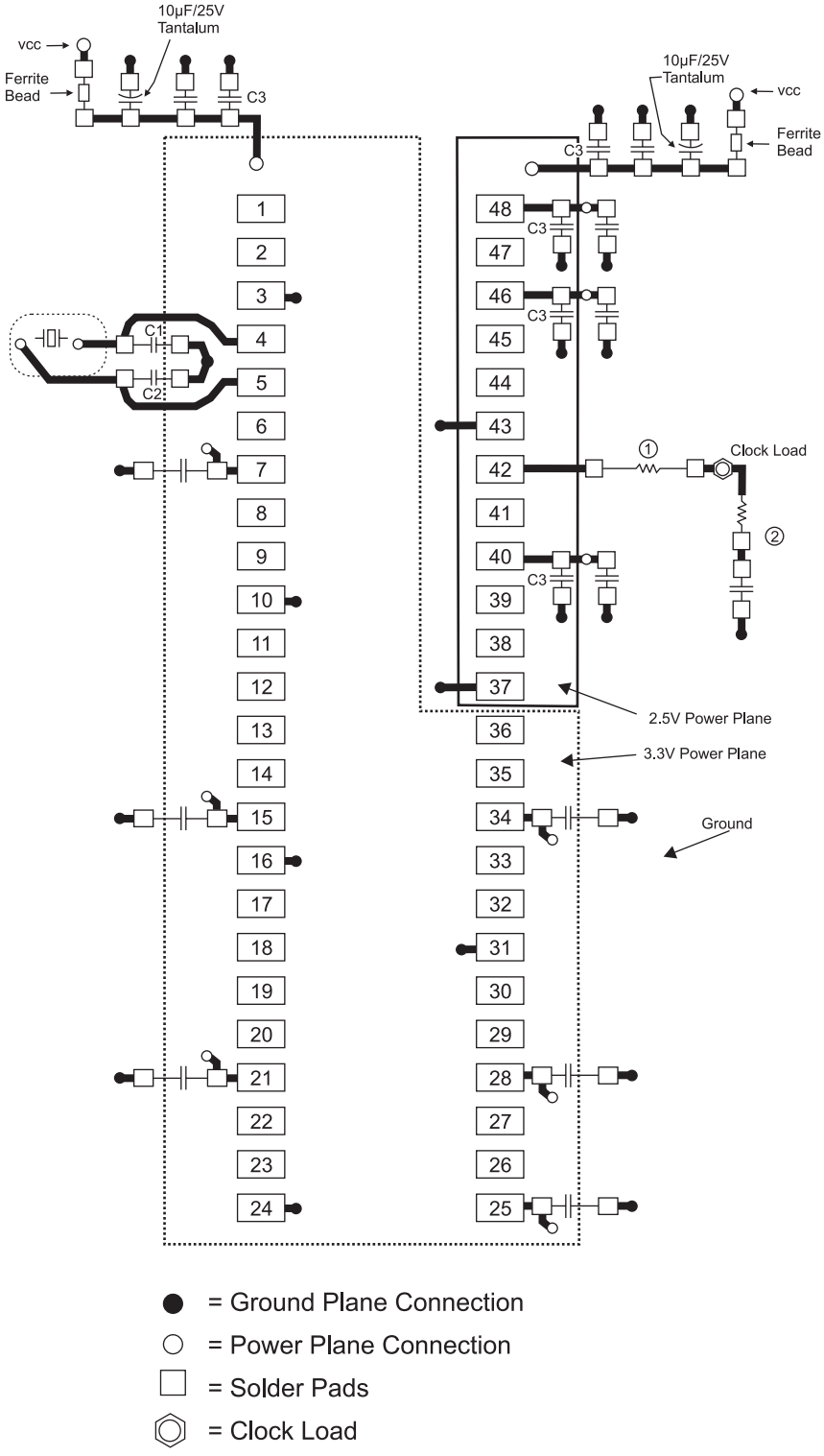
1) All clock outputs should have series terminating resistor. Not shown in all places to improve readibility of diagram.

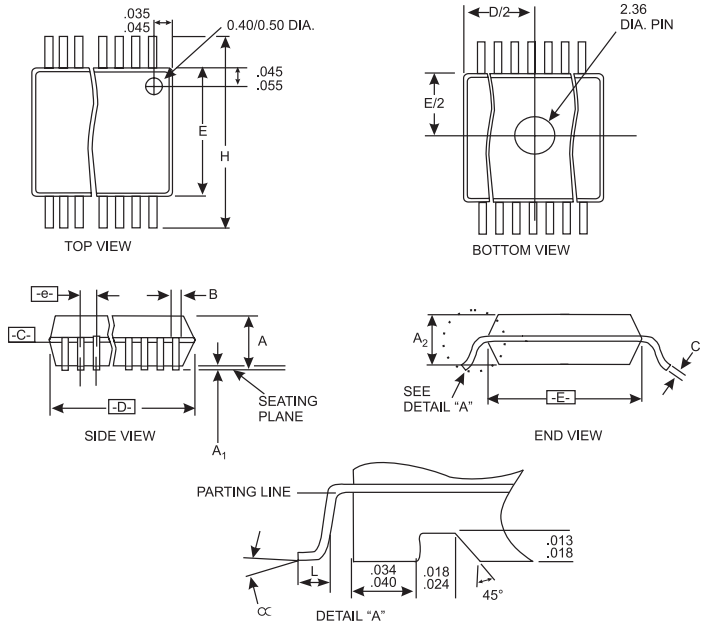
2) 47 ohm / 56pf RC termination should be used on all over 50MHz outputs.

3) Optional crystal load capacitors are recommended.

Connections to VDD:







SSOP Package

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016	AD	.720	.725	.730	56
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	.006	.0085					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∝	0°	5°	8°					
X	.085	.093	.100					

This table in inches

Ordering Information

ICS9148F-25

Example:

ICS XXXX F - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
F=SSOP

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device