

# LH51256

T-46-23-1

## CMOS 256K (32K × 8) Static RAM

### FEATURES

- 32,768 × 8 bit organization
- Access times:  
100/120 ns (MAX.)
- Power consumption:  
Operating: 248 mW (MAX.)  
( $T_A = -40$  to  $85^\circ\text{C}$ , minimum cycle)  
Standby: 16.5  $\mu\text{W}$  (MAX.)  
( $T_A = 0$  to  $60^\circ\text{C}$ )
- Fully static operation
- TTL compatible I/O
- Three state outputs
- Single +5 V power supply
- Packages:  
28-pin, 600-mil DIP  
28-pin, 450-mil SOP

### DESCRIPTION

The LH51256 is a 256K bit static RAM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

### PIN CONNECTIONS

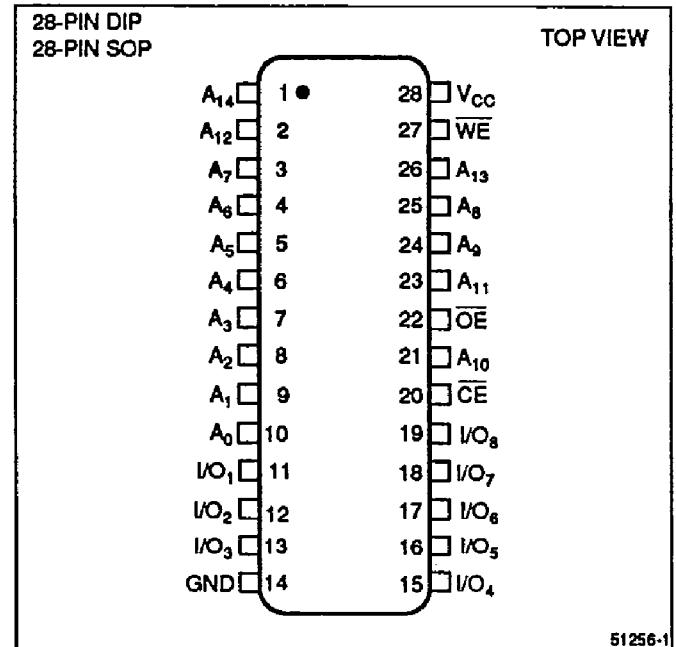
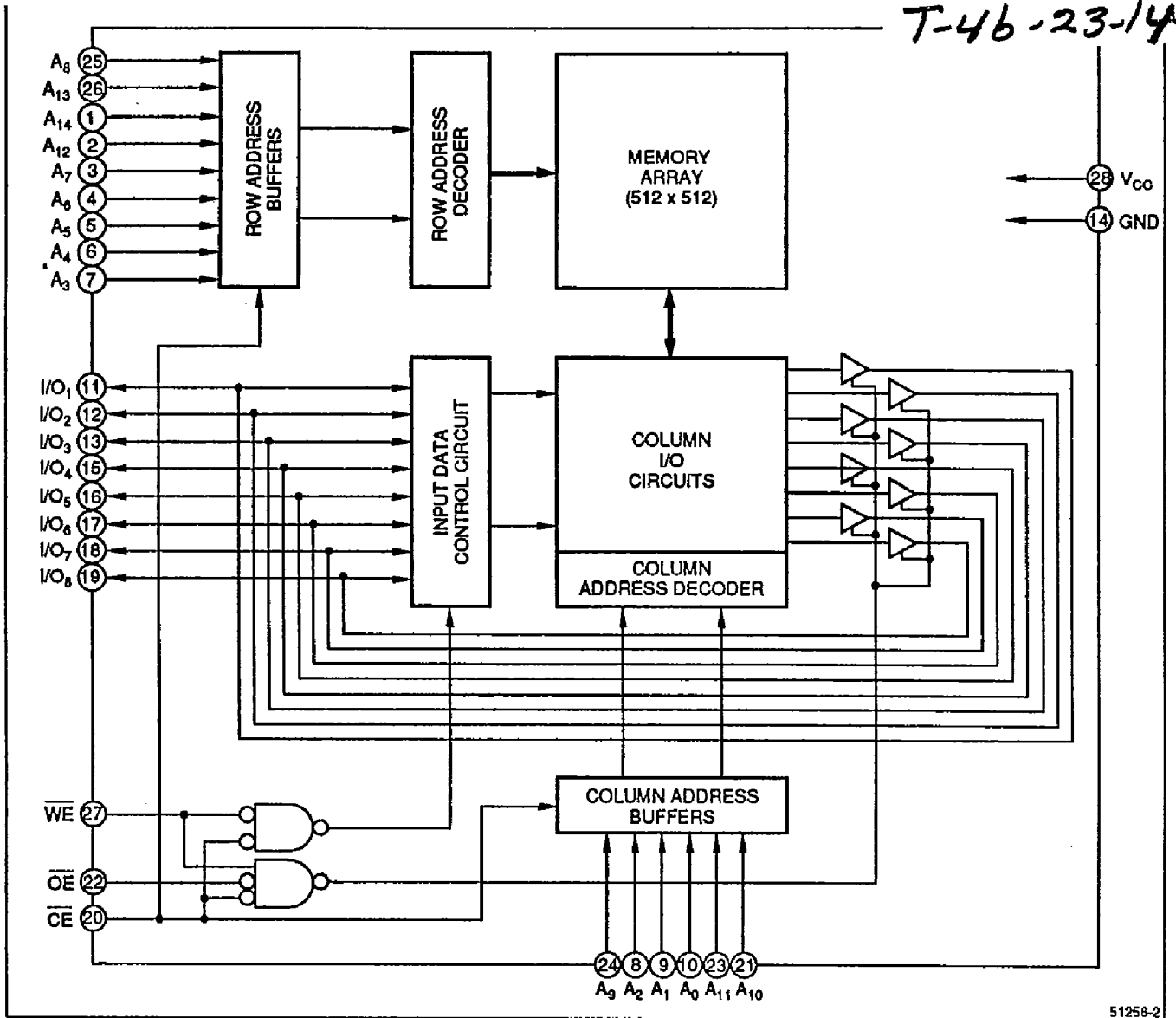


Figure 1. Pin Connections for DIP and SOP Packages

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Figure 2. LH51256 Block Diagram

**PIN DESCRIPTION**

| SIGNAL                           | PIN NAME            |
|----------------------------------|---------------------|
| A <sub>0</sub> - A <sub>14</sub> | Address input       |
| $\overline{CE}$                  | Chip Enable input   |
| $\overline{WE}$                  | Write Enable input  |
| $\overline{OE}$                  | Output Enable input |

| SIGNAL                              | PIN NAME     |
|-------------------------------------|--------------|
| I/O <sub>1</sub> - I/O <sub>8</sub> | Data I/O     |
| V <sub>cc</sub>                     | Power supply |
| GND                                 | Ground       |

**TRUTH TABLE**

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | MODE           | I/O <sub>1</sub> - I/O <sub>8</sub> | I <sub>cc</sub>              | NOTE |
|-----------------|-----------------|-----------------|----------------|-------------------------------------|------------------------------|------|
| H               | X               | X               | Non selected   | High-Z                              | Standby (I <sub>SB</sub> )   | 1    |
| L               | L               | X               | Write          | Data in                             | Operating (I <sub>cc</sub> ) | 1    |
| L               | H               | L               | Read           | Data out                            | Operating (I <sub>cc</sub> ) |      |
| L               | H               | H               | Output disable | High-Z                              | Operating (I <sub>cc</sub> ) |      |

**NOTE:**

1. X = H or L

## ABSOLUTE MAXIMUM RATINGS

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| PARAMETER             | SYMBOL           | RATING       | UNIT | NOTE |
|-----------------------|------------------|--------------|------|------|
| Supply voltage        | V <sub>CC</sub>  | -0.3 to +7.0 | V    | 1    |
| Input voltage         | V <sub>IN</sub>  | -0.3 to +7.0 | V    | 1    |
| Operating temperature | T <sub>opr</sub> | -40 to +85   | °C   |      |
| Storage temperature   | T <sub>stg</sub> | -55 to +150  | °C   |      |

### NOTES:

- The maximum applicable voltage on any pin with respect to GND.

## RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = -40 to +85°C)

| PARAMETER      | SYMBOL          | MIN. | TYP. | MAX.                  | UNIT |
|----------------|-----------------|------|------|-----------------------|------|
| Supply voltage | V <sub>CC</sub> | 4.5  | 5.0  | 5.5                   | V    |
| Input voltage  | V <sub>IH</sub> | 2.2  |      | V <sub>CC</sub> + 0.3 | V    |
|                | V <sub>IL</sub> | -0.3 |      | 0.8                   | V    |

## DC CHARACTERISTICS (V<sub>CC</sub> = 5 V ± 10%, T<sub>A</sub> = -40 to +85°C unless otherwise noted)

| PARAMETER              | SYMBOL           | CONDITIONS   | MIN. | TYP. | MAX. | UNIT |
|------------------------|------------------|--|------|------|------|------|
| Input leakage current  | I <sub>LI</sub>  | V <sub>CC</sub> = 5.5V,<br>V <sub>IN</sub> = 0 to V <sub>CC</sub>                                |      |      | 1    | μA   |
| Output leakage current | I <sub>LO</sub>  | $\overline{CE}$ or $\overline{OE}$ = V <sub>IH</sub> ,<br>V <sub>IO</sub> = 0 to V <sub>CC</sub> |      |      | 1    | μA   |
| Operating current      | I <sub>CC</sub>  | $\overline{CE}$ = V <sub>IL</sub> ,<br>Outputs open  |      |      | 45   | mA   |
| Standby current        | I <sub>SB1</sub> | $\overline{CE}$ = V <sub>IH</sub>  |      |      | 10   | mA   |
|                        | I <sub>SB</sub>  | $\overline{CE} \geq V_{CC} - 0.2 V$ ,<br>T <sub>A</sub> = 0 to +60°C                             |      |      | 3    | μA   |
|                        |                  | $\overline{CE} \geq V_{CC} - 0.2 V$ ,<br>T <sub>A</sub> = -40 to +85°C                           |      |      | 10   | μA   |
| Output voltage         | V <sub>OL</sub>  | I <sub>OL</sub> = 2.1 mA   |      |      | 0.4  | V    |
|                        | V <sub>OH</sub>  | I <sub>OH</sub> = -1.0 mA  | 2.4  |      |      | V    |

## AC CHARACTERISTICS

### (1) READ CYCLE (V<sub>CC</sub> = 5 V ± 10%, T<sub>A</sub> = -40 to +85°C)

| PARAMETER                                | SYMBOL           | LH51256/N-10 |      | LH51256/N-12 |      | UNIT | NOTE |
|--|------------------|--------------|------|--------------|------|------|------|
|  |                  | MIN.         | MAX. | MIN.         | MAX. |      |      |
| Read cycle time                          | t <sub>RC</sub>  | 100          |      | 120          |      | ns   |      |
| Address access time                      | t <sub>AA</sub>  |              | 100  |              | 120  | ns   |      |
| $\overline{CE}$ access time              | t <sub>ACE</sub> |              | 100  |              | 120  | ns   |      |
| Output enable time                       | t <sub>OE</sub>  |              | 50   |              | 60   | ns   |      |
| Output hold time                         | t <sub>OH</sub>  | 5            |      | 5            |      | ns   |      |
| $\overline{CE}$ Low to output in Low-Z   | t <sub>LZ</sub>  | 5            |      | 5            |      | ns   | 1    |
| $\overline{OE}$ Low to output in Low-Z   | t <sub>OLZ</sub> | 5            |      | 5            |      | ns   | 1    |
| $\overline{CE}$ High to output in High-Z | t <sub>HZ</sub>  | 0            | 30   | 0            | 30   | ns   | 1    |
| $\overline{OE}$ High to output in High-Z | t <sub>OHZ</sub> | 0            | 30   | 0            | 30   | ns   | 1    |

### NOTE:

- Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C<sub>LOAD</sub> = 5 pF.

## 2) WRITE CYCLE ( $V_{CC} = 5 V \pm 10\%$ , $T_A = -40$ to $+85^\circ C$ )

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| PARAMETER                                | SYMBOL           | LH51256/N-10 |      | LH51256/N-12 |      | UNIT | NOTE |
|--|------------------|--------------|------|--------------|------|------|------|
|  |                  | MIN.         | MAX. | MIN.         | MAX. |      |      |
| Write cycle time                         | t <sub>WC</sub>  | 100          |      | 120          |      | ns   |      |
| $\overline{CE}$ Low to end of write      | t <sub>CW</sub>  | 90           |      | 100          |      | ns   |      |
| Address valid to end of write            | t <sub>AW</sub>  | 90           |      | 100          |      | ns   |      |
| Address setup time                       | t <sub>AS</sub>  | 5            |      | 5            |      | ns   |      |
| Write recovery time                      | t <sub>WR</sub>  | 15           |      | 15           |      | ns   |      |
| Write pulse width                        | t <sub>WP</sub>  | 50           |      | 50           |      | ns   |      |
| Input data setup time                    | t <sub>DW</sub>  | 30           |      | 30           |      | ns   |      |
| Input data hold time                     | t <sub>DH</sub>  | 10           |      | 10           |      | ns   |      |
| $\overline{WE}$ High to output active    | t <sub>OW</sub>  | 0            |      | 0            |      | ns   | 1    |
| $\overline{WE}$ Low to output in High-Z  | t <sub>WZ</sub>  | 0            | 30   | 0            | 30   | ns   | 1    |
| $\overline{OE}$ High to output in High-Z | t <sub>OHZ</sub> | 0            | 30   | 0            | 30   | ns   | 1    |

### NOTE:

- Active output to high-impedance and high-impedance to output active tests specified for a  $\pm 500$  mV transition from steady state levels into the test load.  $C_{LOAD} = 5$  pF.

## AC TEST CONDITIONS

| PARAMETER               | MODE  |
|-------------------------|---|
| Input voltage amplitude | 0.6V to 2.4 V   |
| Input rise/fall time    | 10 ns   |
| Timing reference level  | 1.5 V   |
| Output load conditions  | 1TTL + $C_L = 100$ pF<br>(Includes scope and jig capacitance) |

## CAPACITANCE <sup>1</sup> ( $T_A = 25^\circ C$ , $f = 1$ MHz)

| PARAMETER                | SYMBOL   | CONDITIONS     | MIN. | TYP. | MAX. | UNIT |
|--------------------------|----------|----------------|------|------|------|------|
| Input capacitance        | $C_{IN}$ | $V_{IN} = 0$ V |      |      | 7    | pF   |
| Input/output capacitance | $C_{IO}$ | $V_{IO} = 0$ V |      |      | 10   | pF   |

### NOTE:

- This parameter is sampled and not production tested.

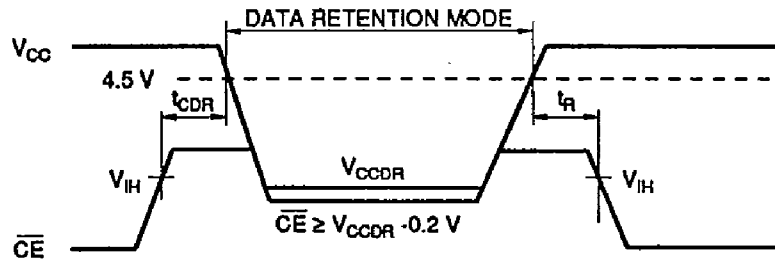
## DATA RETENTION CHARACTERISTICS ( $T_A = -40$ to $+85^\circ C$ except as noted)

| PARAMETER                  | SYMBOL           | CONDITIONS   | MIN.            | TYP. | MAX. | UNIT    | NOTE |
|----------------------------|------------------|--|-----------------|------|------|---------|------|
| Data retention voltage     | $V_{CCDR}$       | $\overline{CE} \geq V_{CCDR} - 0.2V$   | 2.0             |      |      | V       |      |
| Data retention current     | $I_{CCDR}$       | $V_{CCDR} = 3$ V<br>$\overline{CE} \geq V_{CCDR} - 0.2V$ ,<br>$T_A = 0$ to $+60^\circ C$ ,<br>$V_{IN} = 0$ to $V_{CCDR}$   |                 |      | 1    | $\mu A$ |      |
|                            |                  | $V_{CCDR} = 3$ V<br>$\overline{CE} \geq V_{CCDR} - 0.2V$ ,<br>$T_A = -40$ to $+85^\circ C$ ,<br>$V_{IN} = 0$ to $V_{CCDR}$ |                 |      | 6    | $\mu A$ |      |
| $\overline{CE}$ setup time | t <sub>CDR</sub> |  | 0               |      |      | ns      |      |
| $\overline{CE}$ hold time  | t <sub>R</sub>   |  | t <sub>RC</sub> |      |      | ns      | 1    |

### NOTE:

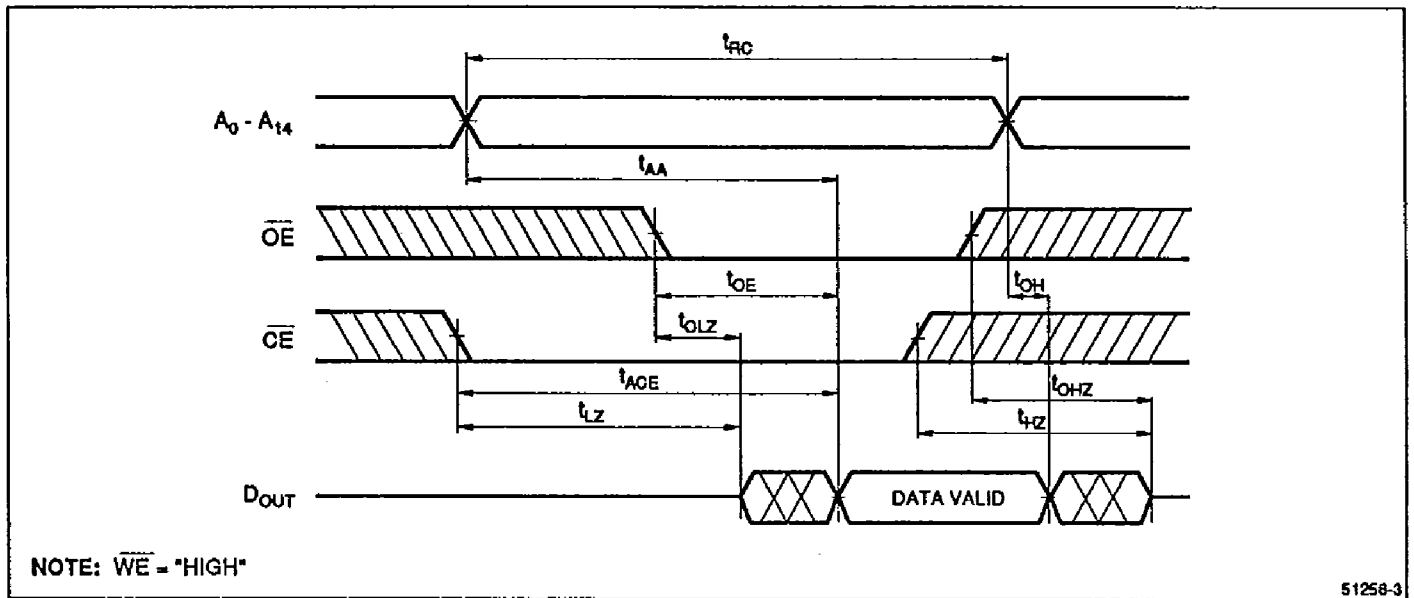
- t<sub>RC</sub> = Read cycle time

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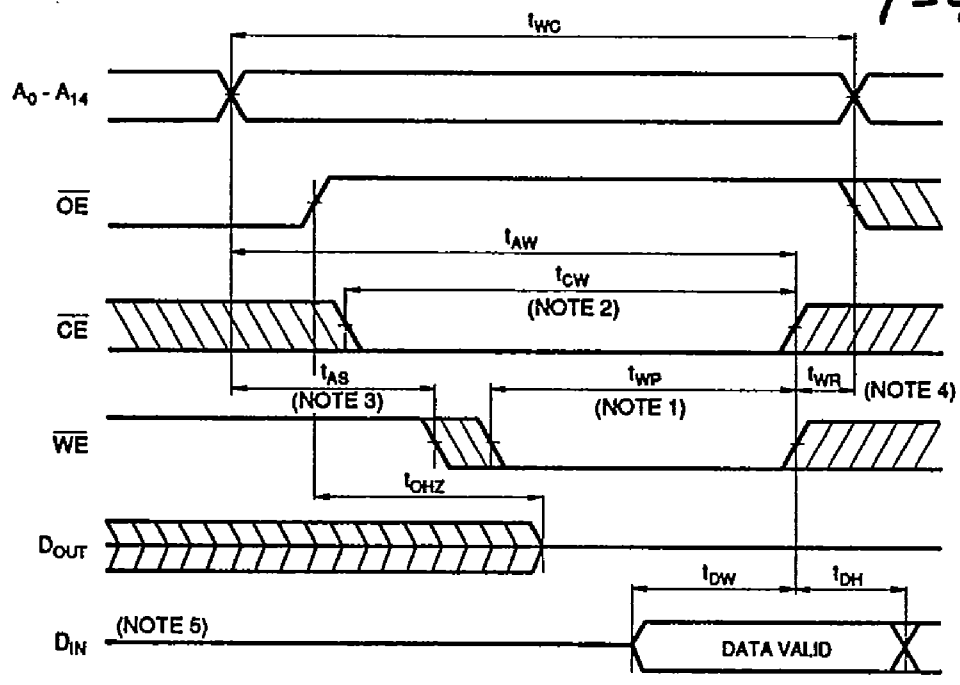
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Figure 3. Low Voltage Data Retention



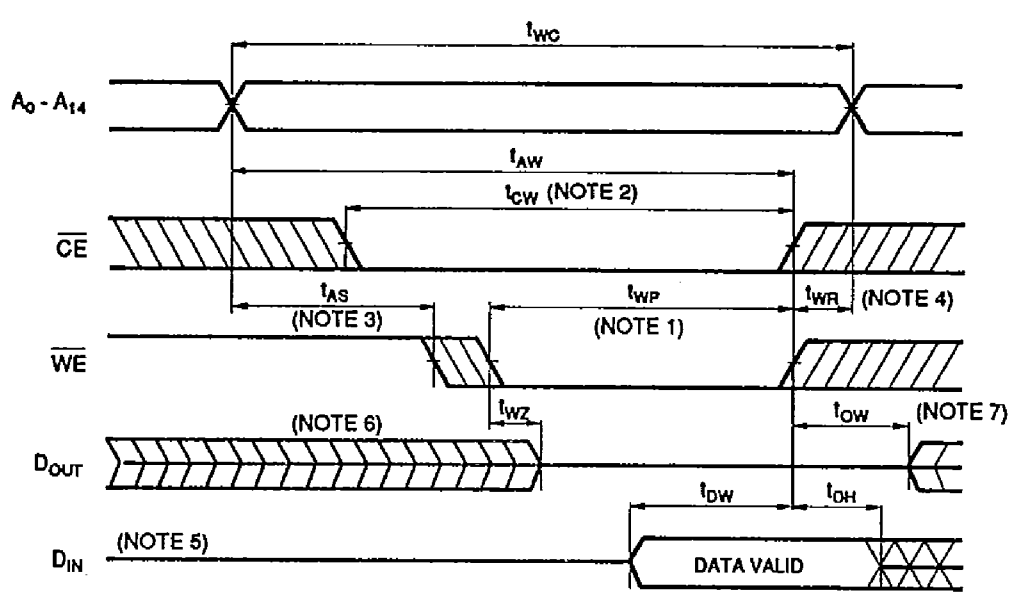
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Figure 4. Read Cycle



- NOTES:**
1. The write pulse occurs during the overlap ( $t_{WP}$ ) of  $\overline{CE} = \text{LOW}$  and  $\overline{WE} = \text{LOW}$ .
  2.  $t_{CW}$  is defined as the time from the  $\overline{CE}$  low transition to the end of write.
  3.  $t_{AS}$  is defined as the time from address change to the start of writing.
  4.  $t_{WR}$  is defined as the time from the end of writing to the address change.
  5. When the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

Figure 5. Write Cycle 1 ( $\overline{OE}$  Clock)



- NOTES:**
1. The write pulse occurs during the overlap ( $t_{WP}$ ) of  $\overline{CE} = \text{LOW}$  and  $\overline{WE} = \text{LOW}$ .
  2.  $t_{CW}$  is defined as the time from the  $\overline{CE}$  low transition to the end of write.
  3.  $t_{AS}$  is defined as the time from address change to the start of writing.
  4.  $t_{WR}$  is defined as the time from the end of writing to the address change.
  5. When the I/O pins are in the output state, input signals with the opposite logic level must not be applied.
  6. If  $\overline{CE}$  LOW transition occurs at the same time or after  $\overline{WE}$  LOW transition, the output will remain high-impedance.
  7. If  $\overline{CE}$  HIGH transition occurs at the same time or prior to the  $\overline{WE}$  HIGH transition, the output will remain high-impedance.

Figure 6. Write Cycle 2 ( $\overline{OE}$  Low)

# ORDERING INFORMATION

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