STRUCTURE Silicon monolithic integrated circuits

PRODUCT SERIES 3-phase motor pre-driver for LBP

TYPE **BD6762FV**

FUNCTION
- Pre-driver for driving Nch MOS FET
- Direct PWM driver possible to select 120 degree or 120 degree slope

○Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limit	Unit
Supply voltage	VCC	36	V
	VG	36	V
Power dissipation	Pd	1100※1	mW
Input voltage	VIN	0～VREG	V
Operating temperature range	Topr	-25～+75	℃
Storage temperature range	Tstg	-40～+150	℃
Junction temperature	Tjmax	150	℃

※1 70mm×70mm×1.6mm glass epoxy board. Derating in done at 8.8mW/℃ for operating above Ta=25℃.

○Recommended operating conditions (Ta=-25～+75℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VCC	16	24	28	V

This product described in this specification isn't judged whether it applies to COCOM regulations.
Please confirm in case of export.
This product isn't designed for protection against radioactive rays.

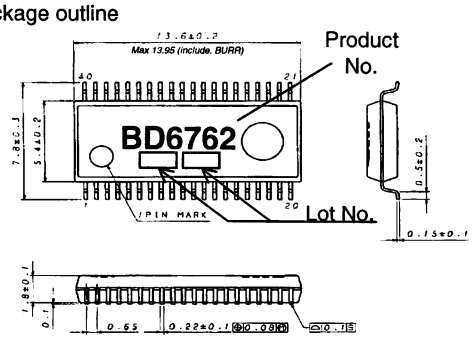
○Electrical characteristics (Unless otherwise specified, Ta=25℃, VCC=24V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Overall						
Circuit current1	ICCS	5.1	7.6	10.2	mA	ST/SP=OPEN
Circuit current2	ICC	10	17	25	mA	ST/SP=GND
VREG voltage	VREG	4.5	5	5.5	V	IVREG=-1mA
Low voltage protection level	VUVON	9.5	11.5	13.5	V	
Low voltage protection hysteresis level	VUVHYS	0.4	0.5	0.6	V	
Hall amp						
Input bias current	IBH	–	1	3	μA	
In-phase input voltage range	VHAR	0	–	3	V	
Input level	VINH	50	–	–	mVp-p	
PWM						
High CFE voltage	VCFEH	2.6	2.9	3.2	V	
Low CFE voltage	VCFEL	1.2	1.4	1.6	V	
CFE oscillating frequency	FCFE	13	16	19	kHz	RFE=20k、CFE=1000pF
RFE voltage	VRFE	0.75	0.95	1.15	V	
FG Amp						
Input bias current	IFGM	-1	–	1	μA	
Input offset voltage	VFGOF	-10	–	10	mV	
High output voltage	VFGOH	3.5	4.0	–	V	I=-0.5mA
Low output voltage	VFGOL	–	1.0	1.5	V	I=0.5mA
Low FGS output voltage	VFGSL	–	0.1	0.3	V	I=2mA
Open loop gain	GFG	45	54	–	dB	f=3kHz
Bias voltage	VBFG	2.25	2.50	2.75	V	
Hysteresis width	VFGHYS	100	180	250	mV	
Integration amp						
Di clamp voltage 1	VDI1	1.5	2.1	2.7	V	INTIN=0.1mA
Di clamp voltage 2	VDI2	0.5	0.7	0.9	V	INTOUT=0.1mA
Bias voltage	VBERR	2.25	2.50	2.75	V	INTIN=INTOUT
Speed discriminator						
High output voltage	VDOH	VREG-0.3	VREG-0.1	–	V	I=-0.1mA
Low output voltage	VDOL	–	0.1	0.3	V	I=0.1mA
PLL						
High output voltage	VPOH	VREG-0.45	VREG-0.15	–	V	I=-0.1mA
Low output voltage	VPOL	–	0.15	0.45	V	I=0.1mA
Lock detection						
Low output voltage	VLDL	–	0.15	0.3	V	I=2mA
Lock protection						
CLK cycle for protection circuit	TLP	13	20	27	msec	LP=0.1μF
VCO						
CLK input frequency range	FCLK	0.2	–	2.5	kHz	Design value (only VCO)
High-level CLK input voltage	VCKH	2.2	–	VREG	V	
Low-level CLK input voltage	VCKL	0	–	0.8	V	
High-level CLK input current	ICKH	-10	–	10	μA	
Low-level CLK input current	ICKL	-140	-100	-60	μA	

○Electrical characteristics (Unless otherwise specified, Ta=25℃, VCC=24V)

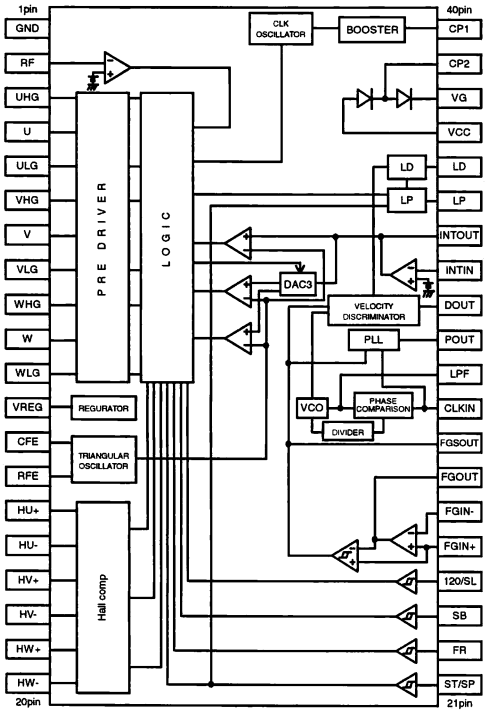
Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Start・stop						
High-level ST/SP input voltage	VSTH	2.2	–	VREG	V	STOP
Low-level ST/SP input voltage	VSTL	0	–	0.8	V	START
High-level ST/SP input current	ISTH	-10	0	10	μA	
Low-level ST/SP input current	ISTL	-70	-50	-30	μA	
Forward rotation / reverse rotation						
High-level FR input voltage	VFRH	2.2	–	VREG	V	reverse
Low-level FR input voltage	VFRL	0	–	0.8	V	forward
High-level FR input current	IFRH	-10	0	10	μA	
Low-level FR input current	IFRL	-70	-50	-30	μA	
120°/slope switching						
High-level 120/slope input voltage	VANH	2.2	–	VREG	V	120°
Low-level 120/slope input voltage	VANL	0	–	0.8	V	120° slope
High-level 120/slope input current	IANH	-10	0	10	μA	
Low-level 120/slope input current	IANL	-70	-50	-30	μA	
Short brake						
High-level SB input voltage	VSBH	2.2	–	VREG	V	short brake condition
Low-level SB input voltage	VSBL	0	–	0.8	V	short brake cancellation
High-level SB input current	ISBH	-10	0	10	μA	
Low-level SB input current	ISBL	-70	-50	-30	μA	
Current limit						
Current detection voltage	VCL	0.23	0.26	0.29	V	
Booster						
CP1 oscillating frequency	FCP1	75	125	175	kHz	
VG step-up voltage	VG	VCC+5.7	VCC+6.7	VCC+7.7	V	
High-side output						
High output voltage 1	VHHG1	VCC+5.8	VCC+6.8	VCC+7.8	V	VG=31V
High output voltage 2	VHHG2	VCC+3.8	VCC+4.8	VCC+5.8	V	Io=-1mA
Low output voltage 1	VHLG1	–	0.1	0.3	V	
Low output voltage 2	VHLG2	–	0.5	1.0	V	Io=5mA
Clamp voltage	VHCL	10	11	12	V	
Low-side output						
High output voltage 1	VLHG1	9.8	10.8	11.8	V	
High output voltage 2	VLHG2	9.0	10.0	11.0	V	Io=-5mA
Low output voltage 1	VLLG1	–	0.1	0.3	V	
Low output voltage 2	VLLG2	–	0.3	0.5	V	Io=5mA

○Package outline



SSOP-B40 (Unit: mm)

○Block diagram



○Pin No. / Pin name

Pin No.	Pin name	Pin No.	Pin name
1	GND	21	ST/SP
2	RF	22	FR
3	UHG	23	SB
4	U	24	120/SL
5	ULG	25	FGIN+
6	VHG	26	FGIN-
7	V	27	FGOUT
8	VLG	28	FGSOUT
9	WHG	29	CLKIN
10	W	30	LPF
11	WLG	31	POUT
12	VREG	32	DOUT
13	CFE	33	INTIN
14	RFE	34	INTOUT
15	HU+	35	LP
16	HU-	36	LD
17	HV+	37	VCC
18	HV-	38	VG
19	HW+	39	CP2
20	HW-	40	CP1

○Operation Notes

(1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range (Topr) may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. The implementation of a physical safety measure such as a fuse should be considered when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

(2) Power supply lines

Regenerated current may flow as a result of the motor's back electromotive force. Insert capacitors between the power supply and ground pins to serve as a route for regenerated current. Determine the capacitance in full consideration of all the characteristics of the electrolytic capacitor, because the electrolytic capacitor may loose some capacitance at low temperatures. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.

(3) Ground potential

Ensure a minimum GND pin potential in all operating conditions.

(4) Setting of heat

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(5) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

(6) ASO

When using the IC, set the output transistor for the motor so that it does not exceed absolute maximum ratings or ASO.

(7) Thermal shutdown circuit

This IC incorporates a TSD (thermal shutdown) circuit (TSD circuit). If the temperature of the chip reaches the following temperature, the motor coil output will be opened. The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

TSD on temperature [°C] (typ.)	Hysteresis temperature [°C] (typ.)
175	23

(8) Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

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