

# DATA SHEET

## **BS108**

**N-channel enhancement mode  
vertical D-MOS transistor**

Product specification  
File under Discrete Semiconductors, SC13b

April 1995

# N-channel enhancement mode vertical D-MOS transistor

**BS108**

**FEATURES**

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

**DESCRIPTION**

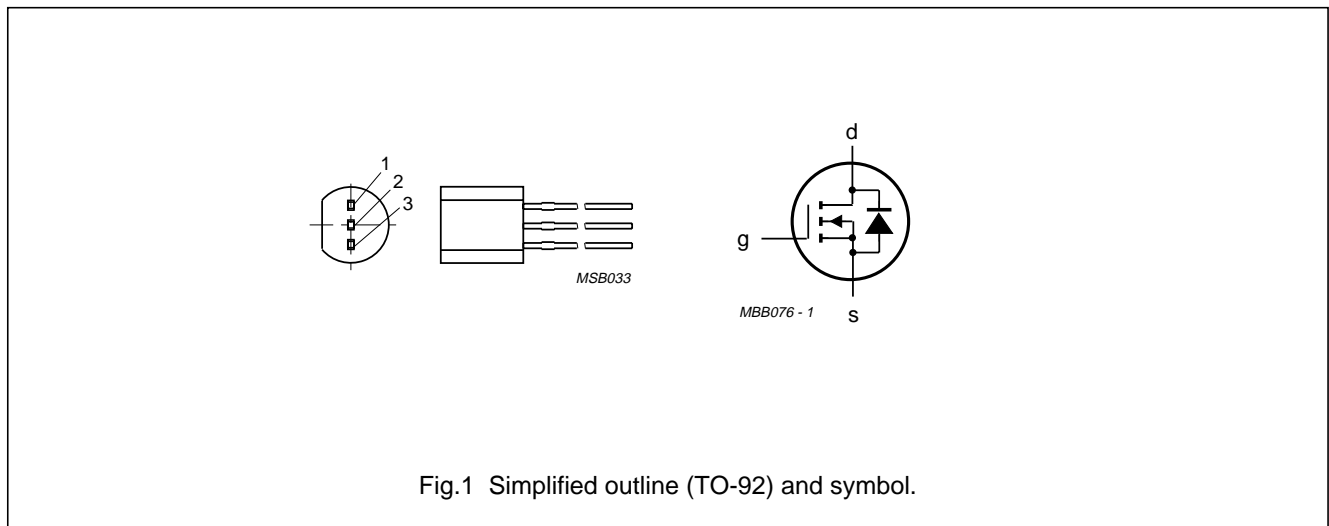
N-channel enhancement mode vertical D-MOS transistor in a TO-92 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

**QUICK REFERENCE DATA**

| SYMBOL       | PARAMETER                     | MAX. | UNIT     |
|--------------|-------------------------------|------|----------|
| $V_{DS}$     | drain-source voltage          | 200  | V        |
| $I_D$        | DC drain current              | 250  | mA       |
| $R_{DS(on)}$ | drain-source on-resistance    | 8    | $\Omega$ |
| $V_{GS(th)}$ | gate-source threshold voltage | 1.8  | V        |

**PINNING**

| PIN | DESCRIPTION |
|-----|-------------|
| 1   | source      |
| 2   | gate        |
| 3   | drain       |



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## LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

| SYMBOL        | PARAMETER                 | CONDITIONS                              | MIN. | MAX. | UNIT |
|---------------|---------------------------|---|------|------|------|
| $V_{DS}$      | drain-source voltage      |   | –    | 200  | V    |
| $\pm V_{GSO}$ | gate-source voltage       | open drain                              | –    | 20   | V    |
| $I_D$         | DC drain current          |   | –    | 250  | mA   |
| $I_{DM}$      | peak drain current        |   | –    | 1    | A    |
| $P_{tot}$     | total power dissipation   | up to $T_{amb} = 25\text{ °C}$ (note 1) | –    | 1    | W    |
| $T_{stg}$     | storage temperature range |   | –65  | 150  | °C   |
| $T_j$         | junction temperature      |   | –    | 150  | °C   |

## THERMAL RESISTANCE

| SYMBOL        | PARAMETER                         | THERMAL RESISTANCE |
|---------------|-----------------------------------|--------------------|
| $R_{th\ j-a}$ | from junction to ambient (note 1) | 125 K/W            |

### Note

- Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum  $10 \times 10$  mm

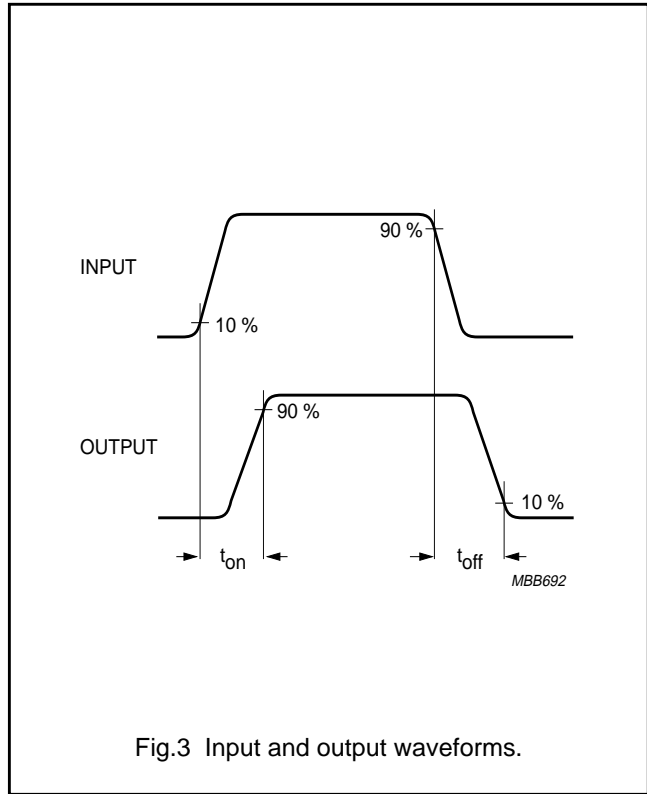
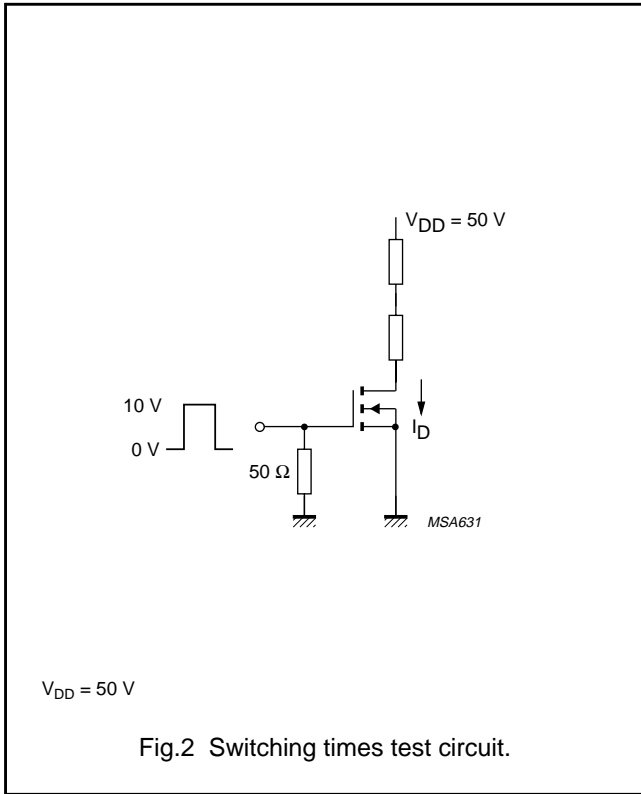
## CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified.

| SYMBOL                                    | PARAMETER                      | CONDITIONS  | MIN. | TYP. | MAX. | UNIT          |
|---|--------------------------------|---|------|------|------|---------------|
| $V_{(BR)DSS}$                             | drain-source breakdown voltage | $I_D = 10\ \mu\text{A}$ ; $V_{GS} = 0$  | 200  | –    | –    | V             |
| $I_{DSS}$                                 | drain-source leakage current   | $V_{DS} = 160\text{ V}$ ; $V_{GS} = 0$  | –    | –    | 1    | $\mu\text{A}$ |
| $I_{GSS}$                                 | gate-source leakage current    | $\pm V_{GS} = 20\text{ V}$ ; $V_{DS} = 0$   | –    | –    | 100  | nA            |
| $V_{GS(th)}$                              | gate-source threshold voltage  | $I_D = 1\text{ mA}$ ; $V_{GS} = V_{DS}$   | 0.4  | –    | 1.8  | V             |
| $R_{DS(on)}$                              | drain-source on-resistance     | $I_D = 100\text{ mA}$ ; $V_{GS} = 2.8\text{ V}$                                   | –    | 5    | 8    | $\Omega$      |
| $ Y_{fs} $                                | transfer admittance            | $I_D = 300\text{ mA}$ ; $V_{DS} = 25\text{ V}$                                    | 200  | 400  | –    | mS            |
| $C_{iss}$                                 | input capacitance              | $V_{DS} = 25\text{ V}$ ; $V_{GS} = 0$ ;<br>$f = 1\text{ MHz}$                     | –    | 50   | 80   | pF            |
| $C_{oss}$                                 | output capacitance             | $V_{DS} = 25\text{ V}$ ; $V_{GS} = 0$ ;<br>$f = 1\text{ MHz}$                     | –    | 20   | 30   | pF            |
| $C_{rss}$                                 | feedback capacitance           | $V_{DS} = 25\text{ V}$ ; $V_{GS} = 0$ ;<br>$f = 1\text{ MHz}$                     | –    | 5    | 10   | pF            |
| <b>Switching times (see Figs 2 and 2)</b> |                                |   |      |      |      |               |
| $t_{on}$                                  | turn-on time                   | $I_D = 250\text{ mA}$ ; $V_{DD} = 50\text{ V}$ ;<br>$V_{GS} = 0$ to $10\text{ V}$ | –    | 5    | 10   | ns            |
| $t_{off}$                                 | turn-off time                  | $I_D = 250\text{ mA}$ ; $V_{DD} = 50\text{ V}$ ;<br>$V_{GS} = 0$ to $10\text{ V}$ | –    | 20   | 30   | ns            |

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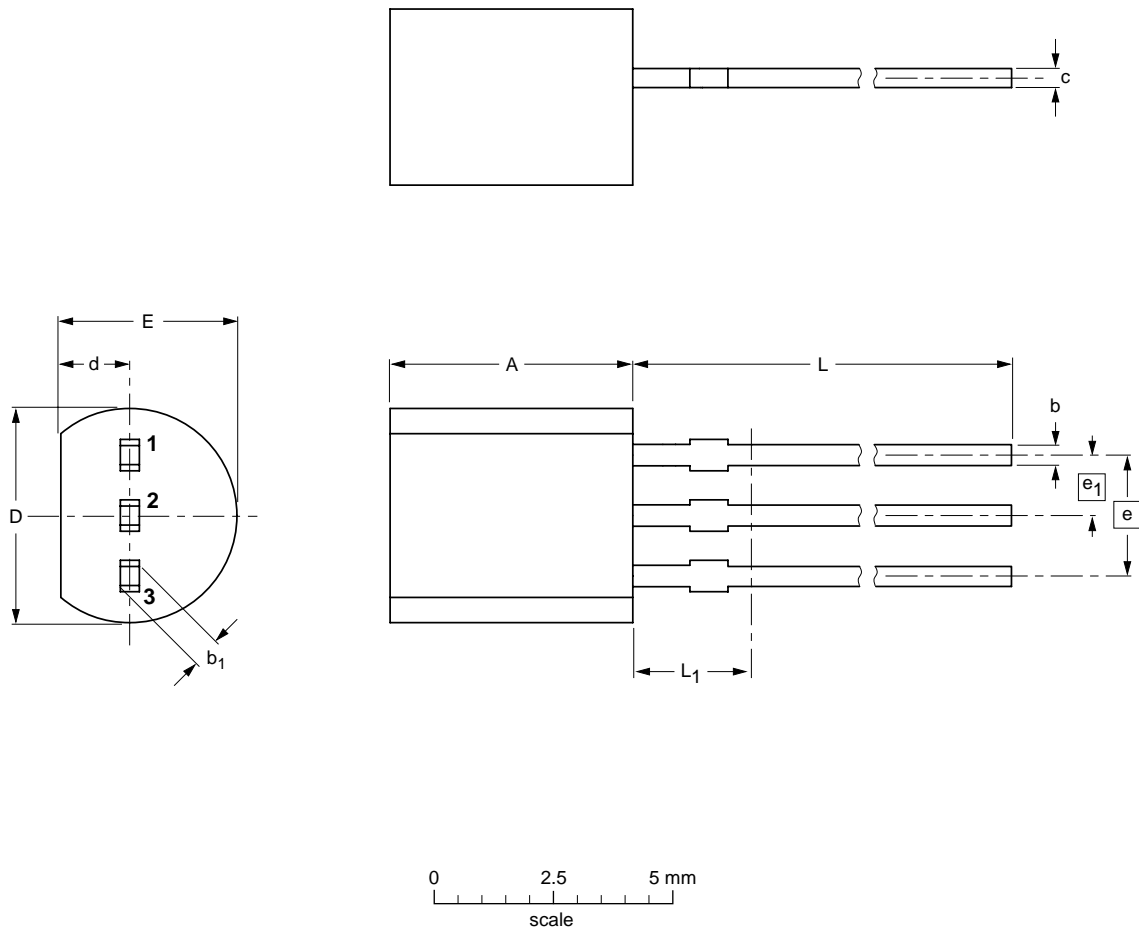
# N-channel enhancement mode vertical D-MOS transistor

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## PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A          | b            | b <sub>1</sub> | c            | D          | d          | E          | e    | e <sub>1</sub> | L            | L <sub>1</sub> <sup>(1)</sup> |
|------|------------|--------------|----------------|--------------|------------|------------|------------|------|----------------|--------------|-------------------------------|
| mm   | 5.2<br>5.0 | 0.48<br>0.40 | 0.66<br>0.56   | 0.45<br>0.40 | 4.8<br>4.4 | 1.7<br>1.4 | 4.2<br>3.6 | 2.54 | 1.27           | 14.5<br>12.7 | 2.5                           |

**Note**

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

| OUTLINE VERSION | REFERENCES |       |       | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|-------|---------------------|------------|
|                 | IEC        | JEDEC | EIAJ  |                     |            |
| SOT54           |            | TO-92 | SC-43 |                     | 97-02-28   |

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## DEFINITIONS

|   |   |
|---|---|
| <b>Data sheet status</b>  |   |
| Objective specification   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification   | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification   | This data sheet contains final product specifications.                                |
| <b>Limiting values</b>  |   |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
| <b>Application information</b>  |   |
| Where application information is given, it is advisory and does not form part of the specification.   |   |

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N-channel enhancement mode vertical  
D-MOS transistor

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