P0120003P

800mW GaAs Power FET (Pb-Free Type)

Technical Note

SUMITOMO ELECTRIC

♦Features

- Up to 2.7 GHz frequency band
- Beyond +27 dBm output power
- Up to +43dBm Output IP3
- High Drain Efficiency
- 12dB Gain at 2.1GHz
- SOT-89 SMT Package
- Low Noise Figure

♦Applications

- Wireless communication system
- Cellular, PCS, PHS, W-CDMA, WLAN

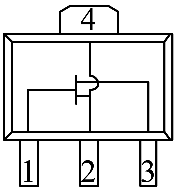
♦Description

P0120003P is a high performance GaAs MESFET housed in a low-cost SOT-89 package. Our originally developed "pulse-doped" channel structure has realized low distortion, which leads to high IP3. The channel structure also achieved an extremely low noise figure. The details about pulse-doped FET channel are described in our products catalog. Utilization of AuSn die attach has realized a low and stable thermal resistance. ***The lead frame is plated with Sn-Bi to make the device Pb-free.***

SEI's long history of manufacturing has cultivated high device reliability. The estimated MTTF of the FET is longer than 15years at Tj of 150°C. You can see the details in ***Reliability and Quality Assurance.***

♦Functional Diagram

Pin No.	Function
1	Input/Gate
2, 4	Ground
3	Output/Drain



♦Ordering Information

Part No	Description	Number of devices	Container
P0120003P	GaAs Power FET	1000	7" Reel
KP023J	2.11-2.17GHz Application Circuit	1	Anti-static Bag

♦Absolute Maximum Ratings (@Tc=25°C)

Parameter	Symbol	Value	Units
Drain-Source Voltage	Vds	8	V
Gate-Source Voltage	Vgs	- 4	V
Drain Current	Ids	Idss	---
RF Input Power (continuous)	Pin	20 (*)	dBm
Power Dissipation	Pt	2.2	W
Junction Temperature	Tj	125	°C
Storage Temperature	Tstg	- 40 to +125	°C

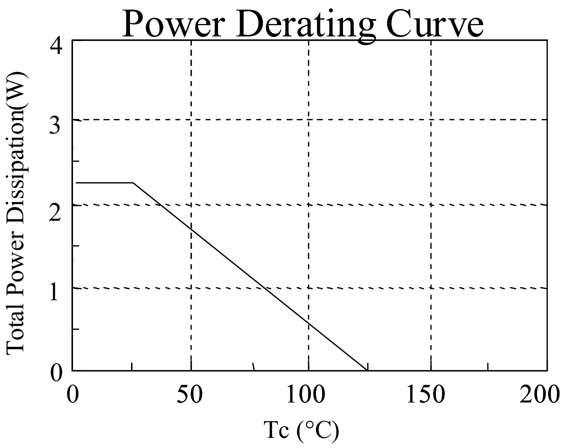
Tc: Case Temperature. Operating the device beyond any of these values may cause permanent damage.

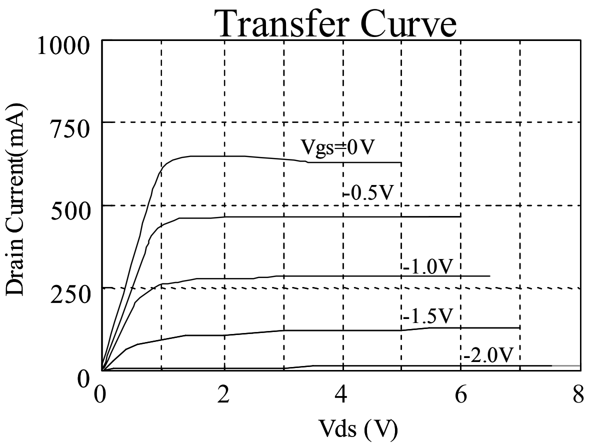
(*) Measured at 2.1GHz with our test fixture matched to OIP3.

♦Electrical Specifications (@Tc=25°C)

Parameter		Symbol	Test Conditions	Values			Units
				Min.	Typ.	Max.	
DC	Saturated Drain Current	Idss	Vds=3V, Vg=0V	---	---	850	mA
	Transconductance	gm	Vds=6V, Ids=300mA	250	---	---	mS
	Pinchoff Voltage	Vp	Vds=6V, Ids=30mA	- 3.0	---	- 1.7	V
	Gate-Source Breakdown Voltage	|Vgs0|	Igso= - 30μA	3.0	---	---	V
	Thermal Resistance	Rth	Channel-Case	---	---	45	°C/W
RF	Frequency	f				2.7	GHz
	Output Power @ 1dB Gain Compression	P1dB	Vds=6V Ids=220mA f=2.1GHz		29	---	dBm
	Small Signal Gain	G			12	---	dB
	Output IP3	OIP3		---	43	---	dBm
	Power Added Efficiency	η_{add}		---	56	---	%

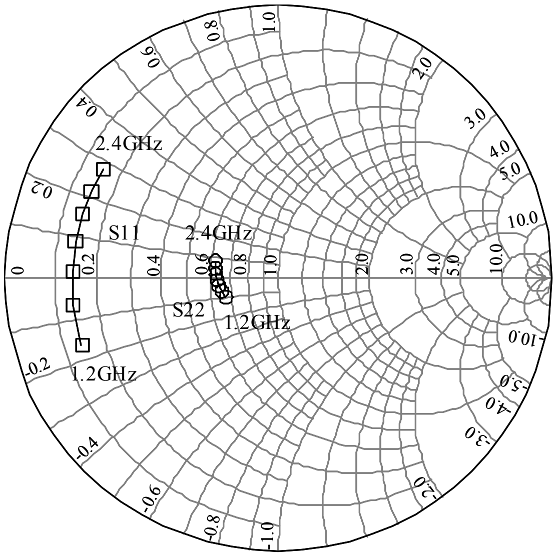
♦Typical Characteristics

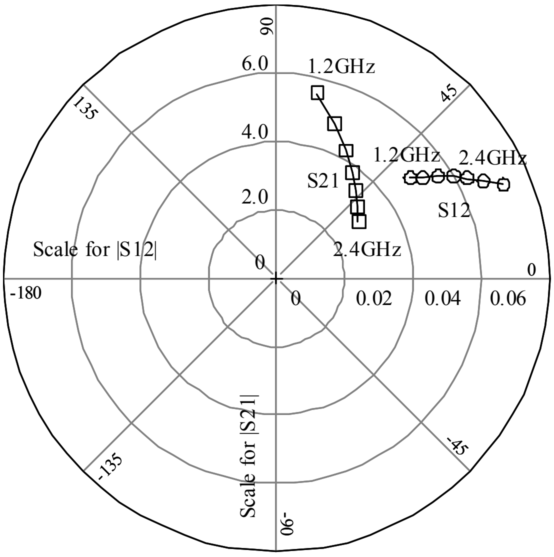




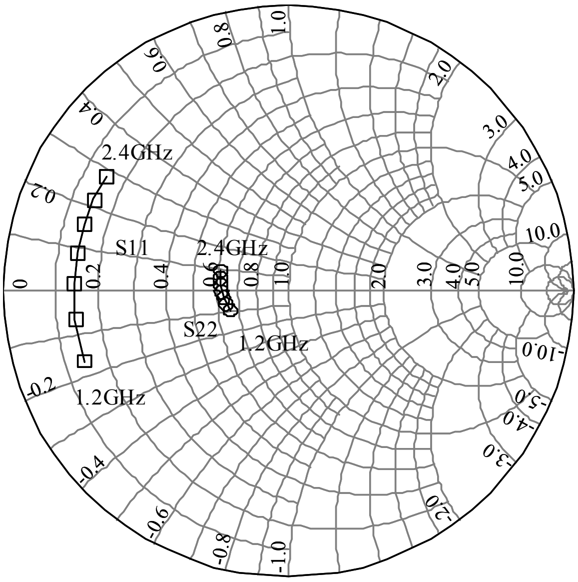
♦Load-pull Characteristics (Typical Data)

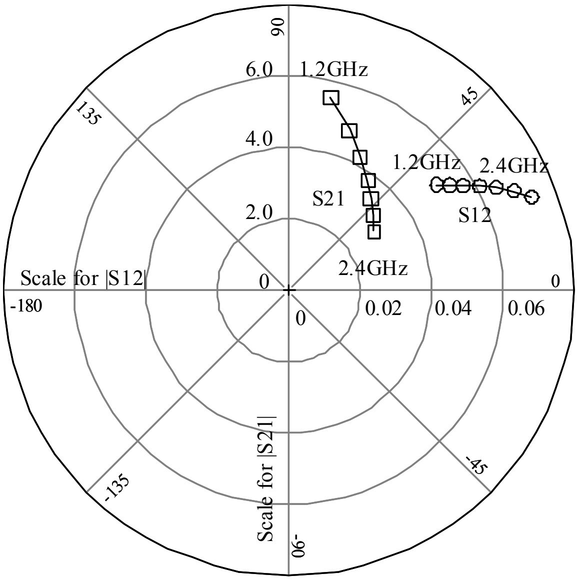
Tc=25°C, Vds=6V, **Ids=220mA,** Common Source, Zo=50Ω (Calibrated to device leads)





Tc=25°C, Vds=6V, **Ids=180mA,** Common Source, Zo=50Ω (Calibrated to device leads)





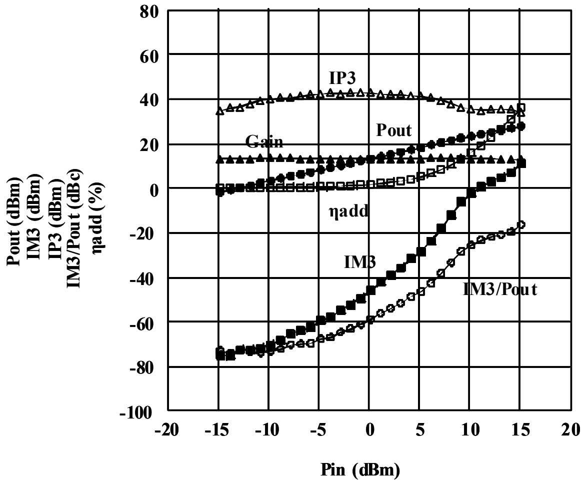
=220mA

Freq (GHz)	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
1.2	0.760	-161.1	5.548	77.6	0.049	36.8	0.204	-160.1
1.4	0.756	-172.5	4.827	69.3	0.052	34.4	0.212	-166.9
1.6	0.754	178.0	4.263	61.7	0.056	32.3	0.219	-172.7
1.8	0.754	169.6	3.812	54.6	0.060	30.0	0.225	-178.1
2.0	0.755	162.0	3.454	47.9	0.063	27.7	0.229	176.5
2.2	0.755	154.9	3.163	41.3	0.067	25.2	0.233	171.2
2.4	0.754	148.0	2.925	34.8	0.072	22.4	0.238	164.9

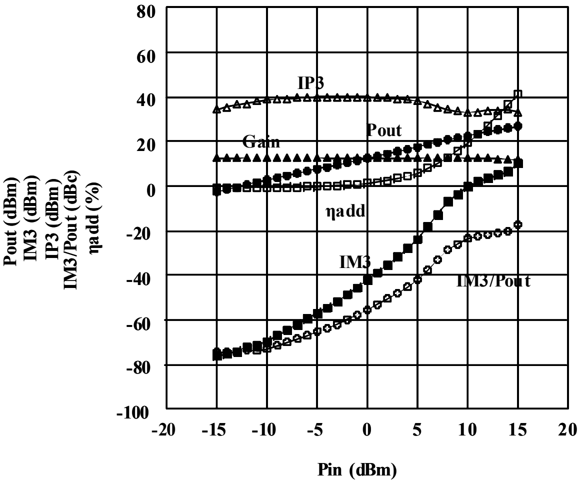
=180mA

Freq (GHz)	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
1.2	0.758	-161.1	5.539	77.7	0.051	35.5	0.215	-161.3
1.4	0.754	-172.5	4.820	69.3	0.054	33.1	0.223	-168.2
1.6	0.753	178.0	4.256	61.8	0.057	30.9	0.229	-174.0
1.8	0.753	169.6	3.805	54.7	0.061	28.6	0.235	-179.5
2.0	0.753	162.0	3.449	48.0	0.065	26.3	0.239	175.0
2.2	0.753	154.9	3.158	41.4	0.069	23.8	0.243	169.6
2.4	0.752	148.0	2.920	34.9	0.073	21.0	0.248	163.4

[Note] You can download the S-parameter list from our web site: www.sei.co.jp/GaAsIC/



Ids=220mA



Ids=180mA

Device: P0120003P
Frequency: f1=2.1GHz, f2=2.101GHz
Bias: Vds=6V, Ids=220mA
Source Matching: Mag 0.61 Ang -159.3°
Load Matching: Mag 0.48 Ang -155.4°

Device:P0120003P
Frequency: f1=2.1GHz, f2=2.101GHz
Bias:Vds=6V,Ids=180mA
Source Matching:Mag 0.61 Ang -159.3°
Load Matching: Mag 0.437 Ang -160.7°

[Note] P_{out} and η_{add} are measured by one signal.

The data for the figures above were measured with the load impedance matched to IP3.

Id=220mA

Pin (dBm)	Pout (dBm)	Gain (dB)	IM3 (dBm)	IM3/Pout (dBc)	IP3 (dBm)	Id (mA)	ηadd (%)
-15.0	-2.0	13.0	-75.0	-73.0	34.5	220.5	0.0
-10.0	3.2	13.2	-70.2	-73.3	39.9	219.1	0.2
-5.0	8.1	13.1	-59.5	-67.7	42.1	216.4	0.5
0.0	13.1	13.1	-46.0	-59.0	42.6	212.0	1.5
5.0	18.0	13.0	-28.5	-46.5	41.0	205.3	4.9
10.0	23.1	13.1	-2.5	-25.7	35.2	207.5	15.7
15.0	27.6	12.6	11.1	-16.5	33.8	252.6	35.8

Id=180mA

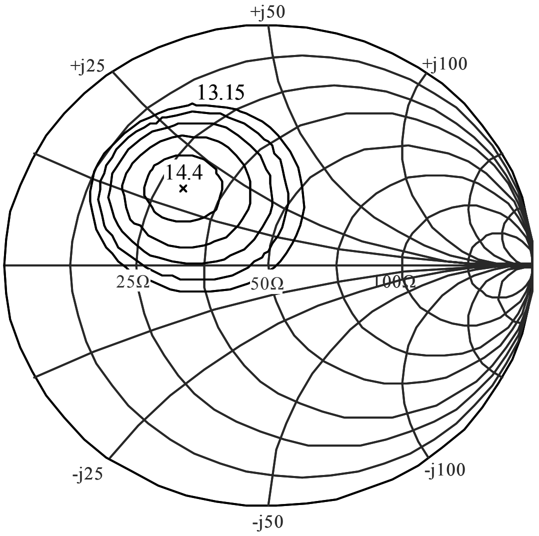
Pin (dBm)	Pout (dBm)	Gain (dB)	IM3 (dBm)	IM3/Pout (dBc)	IP3 (dBm)	Id (mA)	ηadd (%)
-15.0	-1.7	13.3	-75.4	-73.7	35.1	178.2	0.1
-10.0	3.5	13.5	-68.7	-72.2	39.6	177.1	0.2
-5.0	8.4	13.4	-56.1	-64.5	40.7	174.8	0.6
0.0	13.4	13.4	-41.3	-54.7	40.7	171.2	2.0
5.0	18.4	13.4	-23.0	-41.3	39.0	165.1	6.6
10.0	23.4	13.4	0.6	-22.8	33.9	173.1	20.1
15.0	27.6	12.6	11.1	-16.5	34.0	216.4	41.9

Tc=25°C, Vds=6V, Ids=220mA, Pin=0dBm

[Pout-Lstate]

f = 2.1GHz

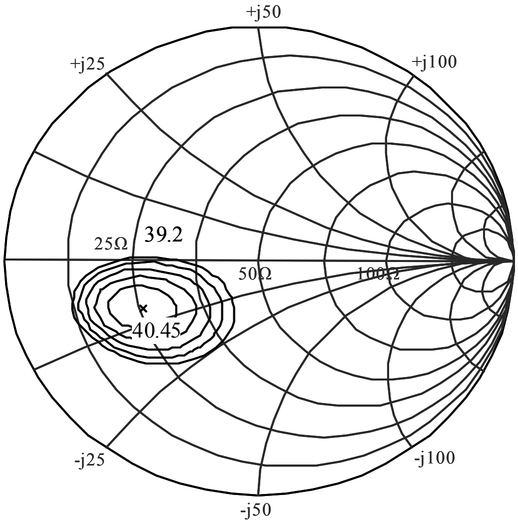
Γ_{pout} : 0.46∠ 135.5
Source : 0.76∠ -166.1
Pout max : 14.4dBm



[IP3-Lstate]

f1 = 2.1GHz
f2 = 2.101GHz

Γ_{IP3} : 0.52∠ -155.9
Source : 0.73∠ -170.1
IP3 max : 40.45dBm

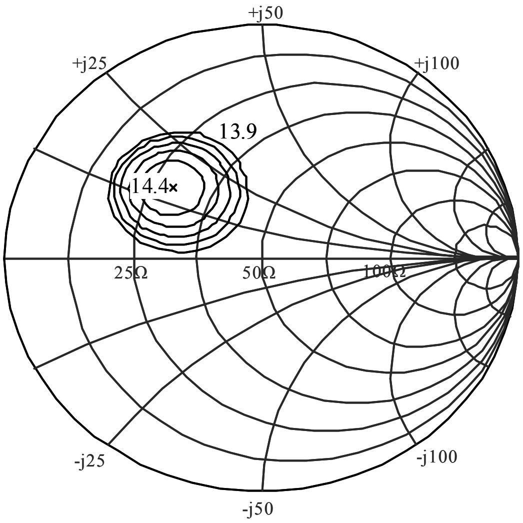


Tc=25°C, Vds=6V, Ids=180mA, Pin=0dBm

[Pout-Lstate]

f = 2.1GHz

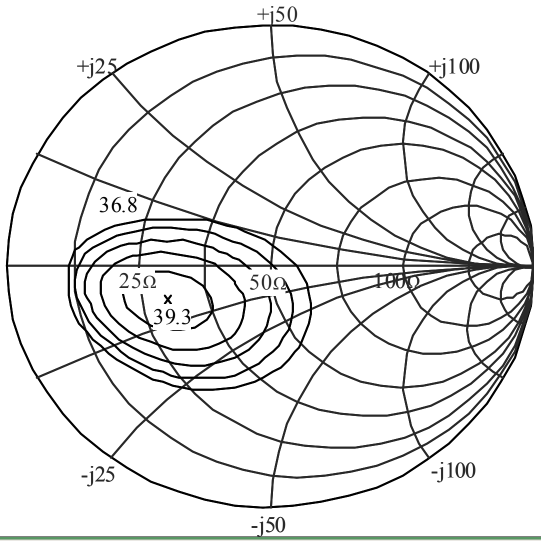
Γ_{pout} : 0.46∠ 138.7
Source : 0.76∠ -166.1
Pout max : 14.4dBm



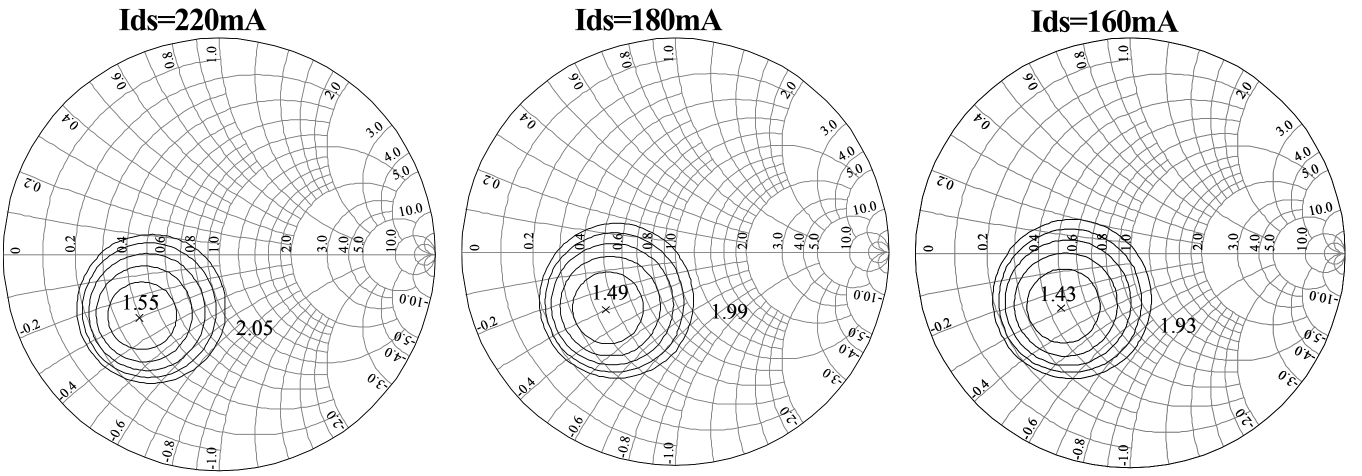
[IP3-Lstate]

f1 = 2.1GHz
f2 = 2.101GHz

Γ_{IP3} : 0.42∠ -160.2
Source : 0.73∠ -170.1
IP3 max : 39.3dBm



♦NF Characteristics



[Note] The data for Smith charts were measured at frequency of 2GHz and Tc of 25°C.

Vds=6V Ids=220mA

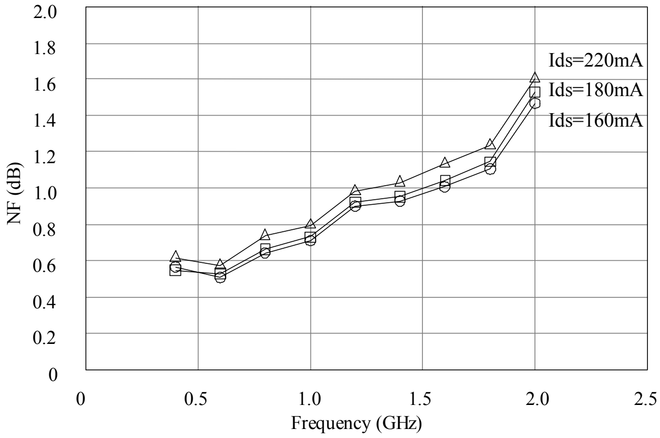
Freq. (GHz)	NFmin (dB)	Γopt Mag	Γopt Ang(deg)	Rn/50	Associated Gain(dB)
0.4	0.58	0.43	-90.8	0.09	21.8
0.6	0.55	0.35	-35.4	0.13	20.3
0.8	0.72	0.28	13.4	0.16	18.6
1.0	0.77	0.36	61.4	0.16	17.6
1.2	0.95	0.40	99.2	0.13	16.5
1.4	0.98	0.47	129.9	0.09	15.7
1.6	1.07	0.51	159.5	0.05	15.0
1.8	1.16	0.55	-173.9	0.04	14.3
2.0	1.55	0.47	-141.6	0.12	13.4

Vds=6V Ids=160mA

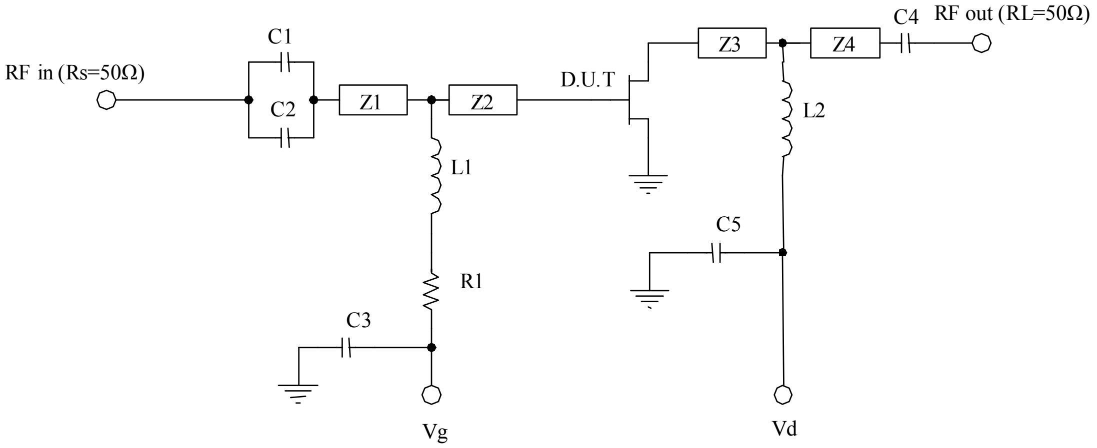
Freq. (GHz)	NFmin (dB)	Γopt Mag	Γopt Ang(deg)	Rn/50	Associated Gain(dB)
0.4	0.53	0.43	-93.5	0.08	21.6
0.6	0.49	0.33	-45.3	0.11	19.8
0.8	0.63	0.26	3.9	0.14	18.2
1.0	0.69	0.32	54.5	0.14	17.2
1.2	0.88	0.34	94.5	0.12	16.1
1.4	0.89	0.43	125.8	0.09	15.4
1.6	0.96	0.46	156.0	0.05	14.7
1.8	1.04	0.52	-177.3	0.04	14.1
2.0	1.43	0.41	-141.5	0.12	13.1

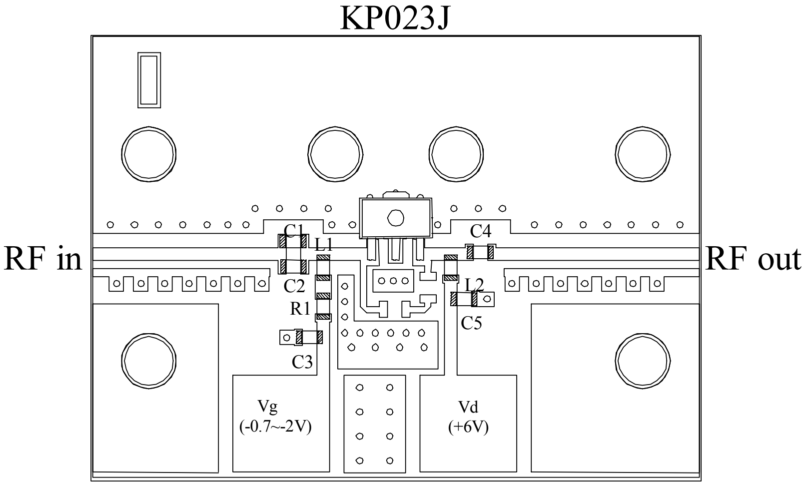
Vds=6V Ids=180mA

Freq. (GHz)	NFmin (dB)	Γopt Mag	Γopt Ang(deg)	Rn/50	Associated Gain(dB)
0.4	0.51	0.44	-89.2	0.08	21.9
0.6	0.51	0.33	-42.7	0.11	19.9
0.8	0.65	0.27	6.7	0.14	18.3
1.0	0.71	0.33	56.8	0.13	17.3
1.2	0.90	0.34	96.5	0.13	16.2
1.4	0.91	0.45	127.5	0.08	15.5
1.6	0.99	0.48	157.2	0.05	14.8
1.8	1.08	0.53	-176.2	0.04	14.1
2.0	1.49	0.42	-140.2	0.12	13.2

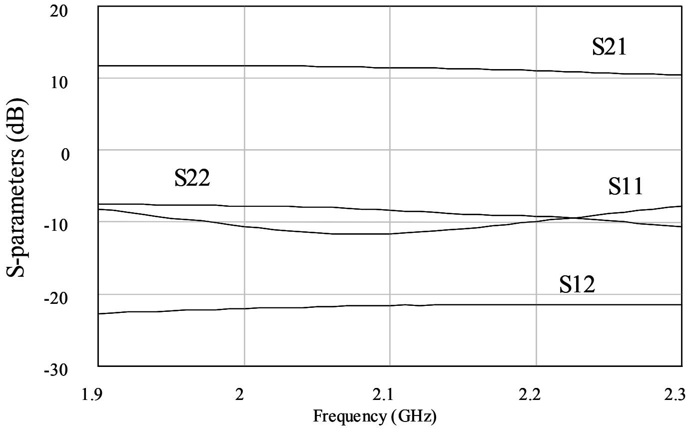


♦Application Circuit : 2110-2170MHz





Ref. Des.	Value	Part Number
R1	82Ω	SUSUMU RR0816 series
C1	1pF	MURATA GRM18 series
C2	1pF	
C3	0.1µF	
C4	4pF	
C5	0.1µF	
L1	27nH	TOKO LL1608 series
L2	27nH	

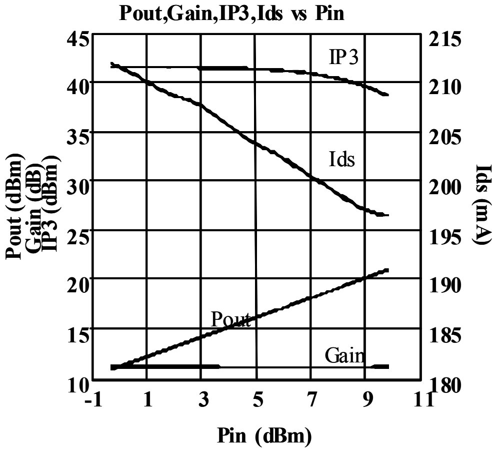


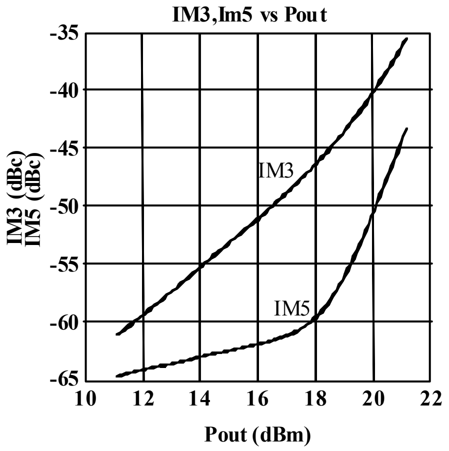
Ref. Designator	Electrical length @ 2.1GHz (deg)
Z1	4.08
Z2	13.61
Z3	8.62
Z4	6.38

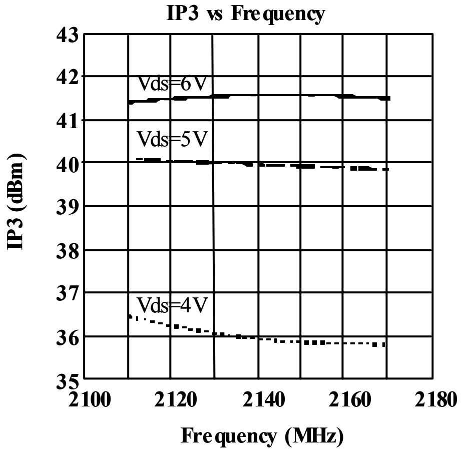
All microstrip lines have a line impedance of 50Ω.

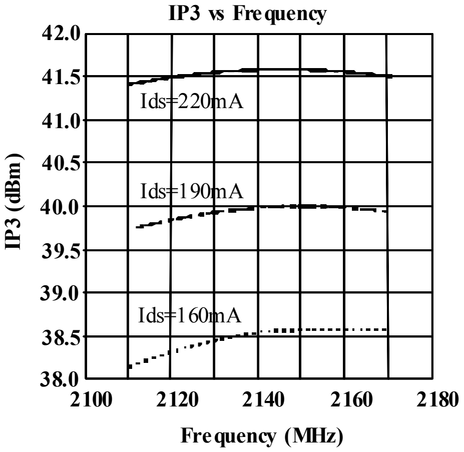
[Typical Performance]

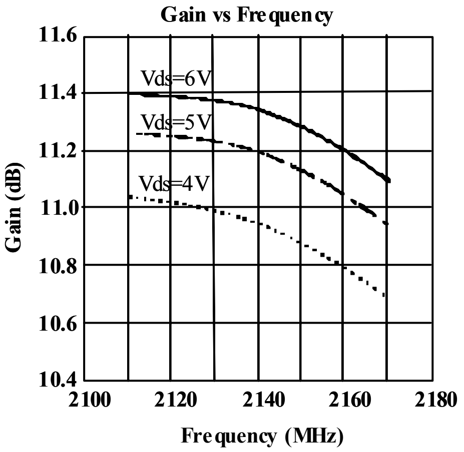
KP023J Application Circuit
Vds=6V, Ids=220mA, Tc=25°C
Frequency characteristics were measured with Pout at 17dBm.

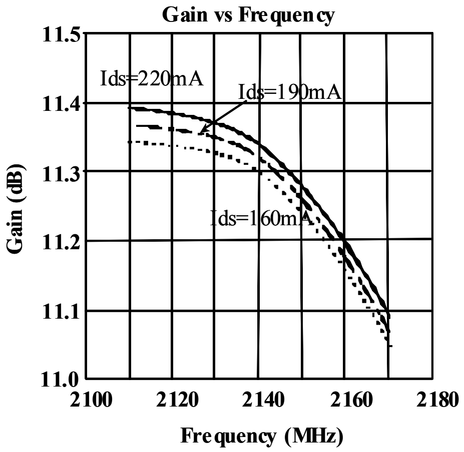






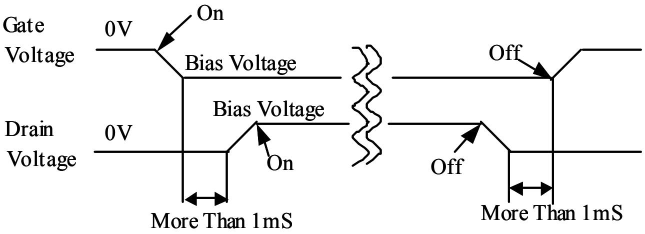






♦Caution: Power Supply Sequence

For safe operation, electric power should be supplied in following sequence. First, the negative voltage should be applied on the gate, and the voltage should be more negative than the pinch-off voltage when you turn on the power supply. Then, drain bias can be applied. Finally, you can turn on the RF signal.
When turning off the power supply, the sequence should be (1)RF signal (2)Drain (3)Gate.

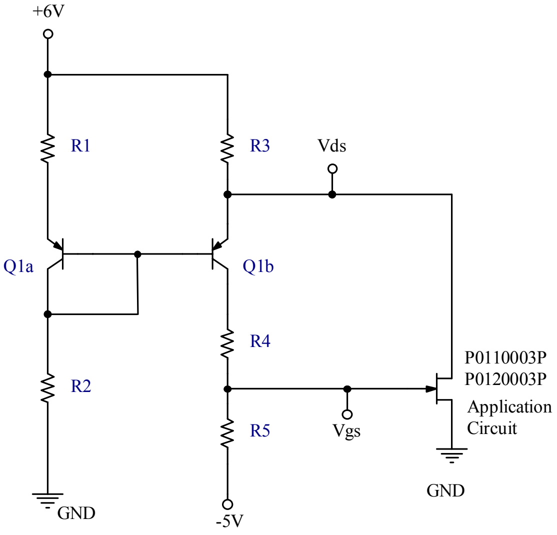


♦Bias Circuit

[Passive Biasing]
If you use a fixed bias circuit, you sometimes need to control the gate bias to get the same Ids, since the devices have some margin of pinch-off voltage (Vp) variation depending on the wafer lots. If you employ a fixed Vgs biasing for your system, you should closely monitor the drain current, particularly when new wafer lots are introduced.

[Active Biasing]
We recommend using an active bias circuit, which can eliminate the influence of Vp variation. An example of an active bias circuit called "current mirror " is shown below. Here, two PNP transistors having the minimum variation of Ibe characteristics are used. These transistors adjust Vgs by changing Vds automatically. It will realize the constant current characteristics, regardless of the temperature.
The circuit should be connected directly in line with where the voltage supplies would be normally connected with the application circuit. Of course a matching circuit is required, but it is not shown in this figure.

[Note]
In the measurements of RF performance (Pout vs Pin, etc) using the application circuit described before, the active bias circuit herein was not utilized. The application circuits were biased directly from two power supplies.



Vds	+5.9V
Ids	220mA
Q1	UMT1N (Rohm)
R1	16Ω 1/10W
R2	1.8kΩ 1/10W
R3	0.22Ω RL series (SUSUMU)
R4	1kΩ 1/10W
R5	1.3kΩ 1/10W

If you used Ids other than 220mA, you can calculate the resistance values as follows:

R4 set to be 1kΩ
I_1: Ic of Q1a I_2:Ic of Q1b
V_{be1}: Vbe of Q1a V_{be2}: Vbe of Q1b

$R1=(+6V-Vds+V_{be2}-V_{be1})/I_1=(+6V-Vds)/I_1$
$R2=(Vds-V_{be2})/I_1$
$R3=(+6V-Vds)/(Ids+I_2)$
$R5=|-5V-Vgs|/I_2$

♦Attention to Heat Radiation

In the layout design of the printed circuit board (PCB) on which the power FETs are attached, the heat radiation to minimize the device junction temperature should be taken into account, since it significantly affects the MTTF and RF performance. In any environment, the junction temperature should be lower than the absolute maximum rating during the device operation and it is recommended that the thermal design has enough margin.

The junction temperature can be calculated by the following formula.

$$T_{jmax}=(Vds*Ids-P_{out})(R_{th}+R_{board}+R_{hs})+T_a$$

P_{out}: Output power
R_{th}: Thermal resistance between channel and case
R_{board}: Thermal resistance of PCB
R_{hs}: Thermal resistance of heat sink
T_a: Ambient temperature
T_{jmax}: Maximum junction temperature

Generally, there are two ways of heat radiation. One is the plated thru hole and the other is the heat sink. Key points will be illustrated in each case below. Note that no measure against oscillation is adopted in the figures. In the design of circuit and layout, you should take stabilizing into account if necessary.

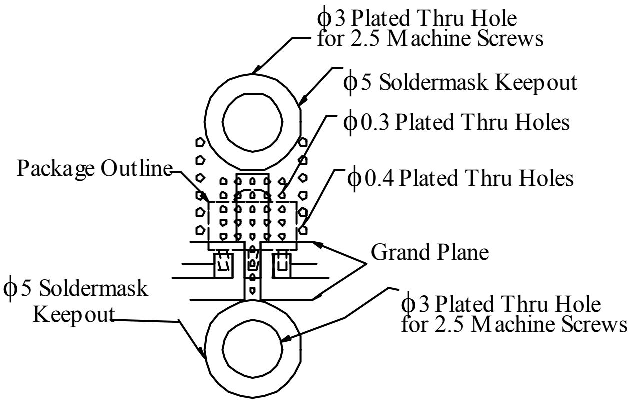
[Using Thru Hole]

☐Multiple plated thru holes are required directly below the device.

☐Place more than 2 machine screws as close to the ground pin (pin 4) as possible. The PCB is screwed on the mounting plate or the heat sink to lower the thermal resistance of the PCB.

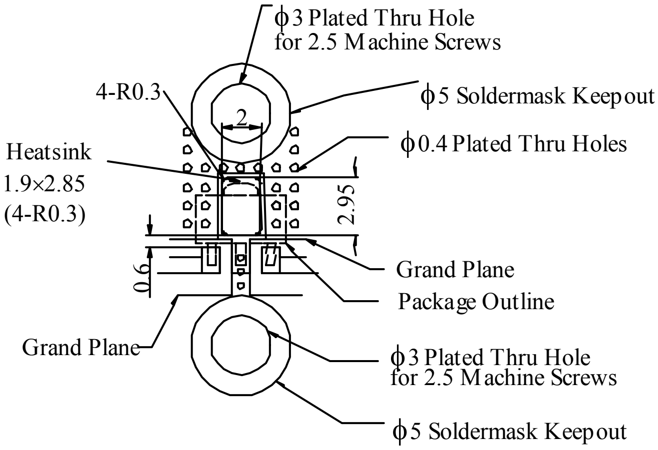
☐Lay out a large ground pad area with multiple plated thru holes around pin 4 of the device.

☐The required matching and feedback circuit described in the application circuit examples should be connected to the device, although it is not shown in the figure below.



[Using Heat Sink]

If you cannot get the junction temperature lower than the absolute maximum rating only with the plated thru holes, then you need to employ the heat sink. Attaching the heat sink directly under pin 4 of the device improves the thermal resistance between junction and ambient.



[Note]

☐Ground/thermal vias are critical for the proper device performance. Drills of the recommended diameters should be used in the fabrication of vias.

☐Add as much copper a s possible to inner and outer layers near the part to ensure optimal thermal performance.

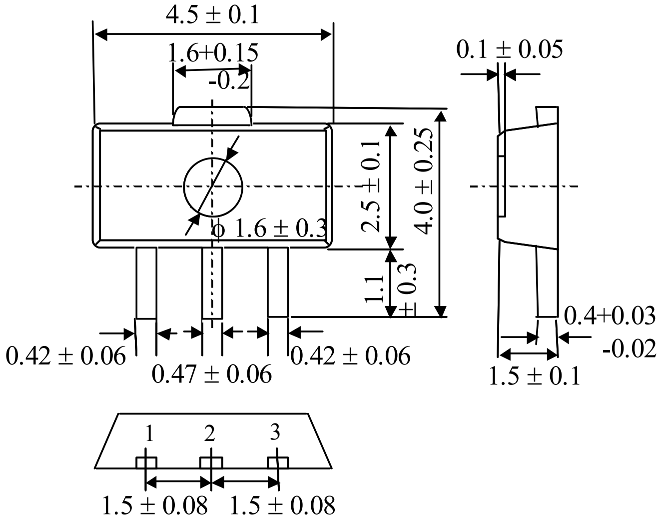
☐Mounting screws can be added near the part to fasten the board to heat sink. Ensure that the ground/thermal via region contacts the heat sink.

☐Do not put solder mask on the backside of the PCB in the region where the board contacts the heat sink.

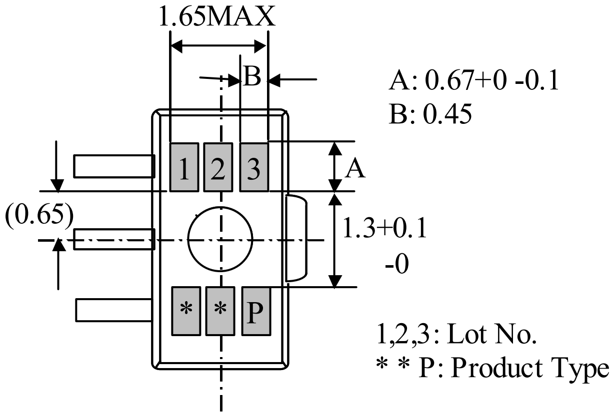
☐RF trace width depends upon the PCB material and construction.

☐Use 1 oz. Copper minimum.

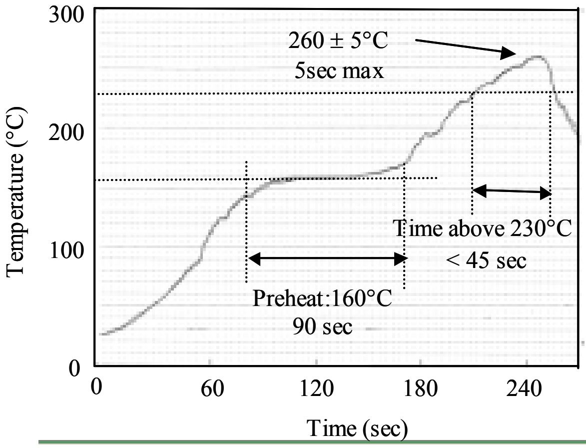
♦Package Drawing



♦Laser Marking



♦Convection Reflow Profile (Recommended)



[Note]

The reflow profile is different from the one for Sn-Pb plating.

If you use a soldering iron to attach the devices, please beware of the followings.

(1) The tip of the iron should be grounded. Or you should use an iron that is electrostatic discharge proof.

(2) The temperature of the iron tip should be lower than 240 °C and the soldering should be completed within 10 seconds.

♦Attention to ESD

Generally, GaAs devices are very sensitive to electrostatic discharge (ESD). To reduce the ESD damage, please pay attention to the followings. The devices should be stored with the electrodes short-circuited by conductive materials. The workstation and tools should be grounded for safe dissipation of the static charges in the environment. The workpeople are to wear anti-static clothing and wrist straps. For safety reasons, resistance of 10MΩ or so should exist between workpeople and ground.

♦Attention to Moisture

The moisture sensitivity level (MSL) of P0120003P is 3, which means that the "floor life" is 168 hours below 30°C with relative humidity (Rh) of 60%.

The devices are usually shipped in moisture-resistant alumina-laminated packages. After breaking the packages, they are to be stored under normal temperature and humidity (5-35°C, 45-75%), with no corrosive gases or dust in the environment. Assemble the devices within 168 hours after breaking the package, or you have to bake them at 85°C for 24 hours before assembling.

♦Reliability and Environmental Issues

The detailed reliability information can be seen in ***Reliability and Quality Assurance***, which you can download from our web site.

SEI's Yokohama Works, where the devices are manufactured, has been accredited ISO-14001 since 1999. We control the toxic materials in our products in accordance with PRTR regulation.

♦ Lead and Fluoride

To realize Pb-free products, Sn-Bi is used for the lead frame plating. Any fluoride that has been determined by the Montreal agreement is not used in the products.

♦Caution

GaAs FET chips are used in P0120003P. For safety reasons, you should attend to the following matters:
(1) Do not put the products in your mouse.
(2) Do not make the products into gases or powders, by burning, breaking or chemical treatments.
(3) In case you abandon the products, you should obey the related laws and regulations.

♦Technical Inquiries are Welcome

SEI welcomes technical questions from any customers. The e-mail is GaAsIC-ml@ml.sei.co.jp. You can also contact our regional offices as below.

♦Worldwide Contacts

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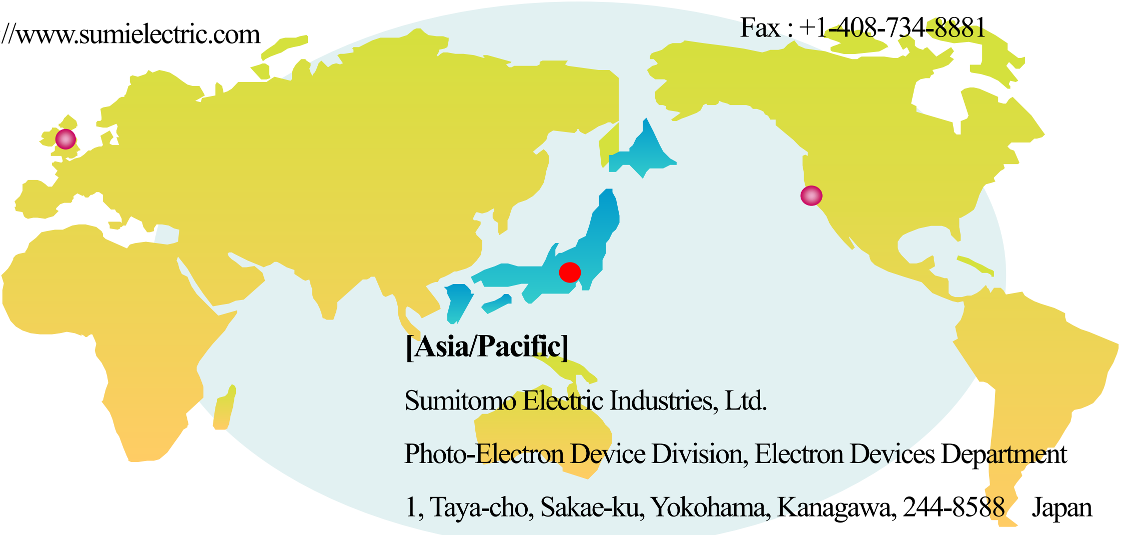

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◆SEI's semi-conductor device products are designed and manufactured for use in the standard communication equipment. Customers that wish to use these products in applications not intended by SEI must contact SEI' sales representatives in advance.

◆Generally, it is impossible to eliminate completely the defects in semi-conductor products, while SEI has been continually improving the quality and reliability of the products. SEI does not assume any responsibility for any losses incurred by customers or third parties by or arising from the use of SEI's semi-conductor products. Customers are to incorporate sufficient safety measures in the design such as redundancy, fire-containment and anti-failure features.