

## Features

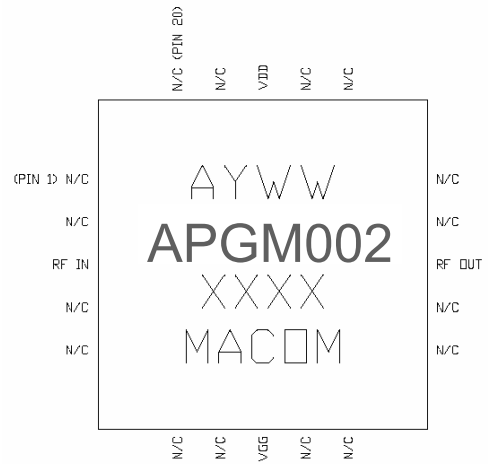
- ◆ 1.0W Operation
- ◆ Variable Drain Voltage (4-10V) Operation
- ◆ MSAG™ Process
- ◆ 5x5 mm 20 Lead MLP Package

## Description

The MAAPGM0027 is a packaged, 2-stage, 1.0 W power amplifier with on-chip bias networks in a 20 lead MLP package, allowing easy assembly. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate MESFET Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.



## Primary Applications

- ◆ Wireless Local Loop 3.4-3.6 GHz
- ◆ MMDS 2.5-2.7 GHz
- ◆ Radar

## Maximum Operating Conditions <sup>1</sup>

Parameter	Symbol	Absolute Maximum	Units
Input Power	P <sub>IN</sub>	15.0	dBm
Drain Supply Voltage	V <sub>DD</sub>	+12.0	V
Gate Supply Voltage	V <sub>GG</sub>	-3.5	V
Quiescent Drain Current (No RF, 40% IDSS)	I <sub>DQ</sub>	360	mA
Quiescent DC Power Dissipated (No RF)	P <sub>DISS</sub>	3.3	W
Junction Temperature	T <sub>J</sub>	180	°C
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C

1. Operation outside of these ranges may reduce product reliability.

**1.0W Power Amplifier 2.0-4.0 GHZ**

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**Recommended Operating Conditions**

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	V <sub>DD</sub>	4.0	8.0	10.0	V
Gate Supply Voltage	V <sub>GG</sub>	-2.4	-2.0	-1.3	V
Input Power	P <sub>IN</sub>		10.0	13.0	dBm
Junction Temperature	T <sub>J</sub>			150	°C
Thermal Resistance	Θ <sub>JC</sub>		26.1		°C/W
Package Base Temperature	T <sub>B</sub>			Note 2	°C

**2. Maximum Package Base Temperature = 150°C — Θ<sub>JC</sub>\* V<sub>DD</sub> \* I<sub>DQ</sub>**

**Electrical Characteristics: T<sub>B</sub> = 40°C<sup>3</sup>, Z<sub>0</sub> = 50 W, V<sub>DD</sub> = 8V, I<sub>DQ</sub> ≈ 230 mA<sup>4</sup>, P<sub>in</sub> = 10 dBm, R<sub>G</sub> ≈ 300 Ω**

Parameter	Symbol	Typical*	Units
Bandwidth	f	2.0-4.0	GHz
Output Power	POUT	30	dBm
Power Added Efficiency	PAE	35	%
1-dB Compression Point	P1dB	29	dBm
Small Signal Gain	G	22	dB
Input VSWR	VSWR	2:1	
Output VSWR	VSWR	1.8:1	—
Gate Supply Current	I <sub>GG</sub>	<4	mA
Drain Supply Current	I <sub>DD</sub>	<400	mA
Noise Figure	NF	6	dB
2 <sup>nd</sup> Harmonic	2f	-15	dBc
3 <sup>rd</sup> Harmonic	3f	-25	dBc
Output Third Order Intercept	OTOI	37	dBm
3 <sup>rd</sup> Order Intermodulation Distortion, Single Carrier Level = 21 dBm	IM3	-12	dBm
5 <sup>th</sup> Order Intermodulation Distortion, Single Carrier Level = 21 dBm	IM5	-36	dBm

**3. T<sub>B</sub> = MMIC base temperature.**

**4. Adjust V<sub>GG</sub> between -2.4 to -1.3V to achieve indicated I<sub>DQ</sub>.**



**Operating Instructions**

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V<sub>GG</sub> ≈ -1.7V, V<sub>DD</sub> = 0 V.
2. Ramp V<sub>DD</sub> to desired voltage, typically 8 V.
3. Adjust V<sub>GG</sub> to set I<sub>DQ</sub>, (See Note 3 above).
4. Set RF input.
5. Power down sequence in reverse. Turn V<sub>GG</sub> off last.

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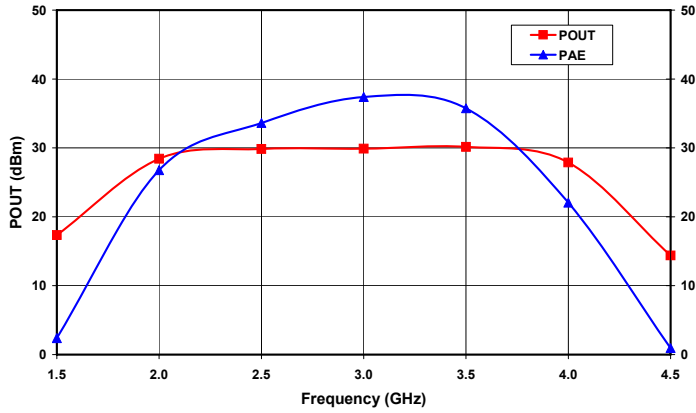


Figure 1. Output Power and Power Added Efficiency vs. Frequency at  $V_{DD} = 8V$  and  $P_{in} = 8$  dBm

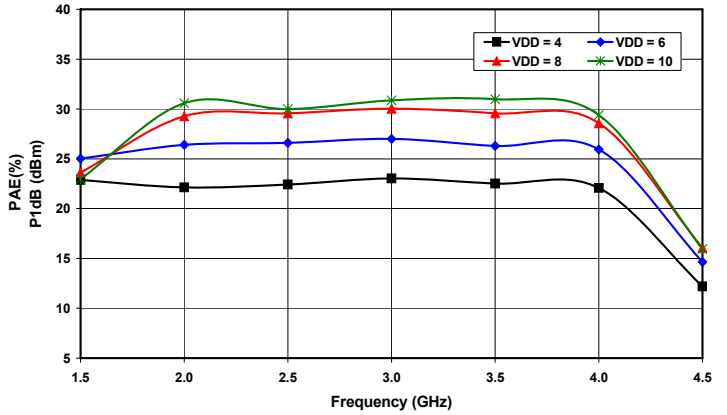


Figure 2. 1dB Compression Point vs. Drain Voltage

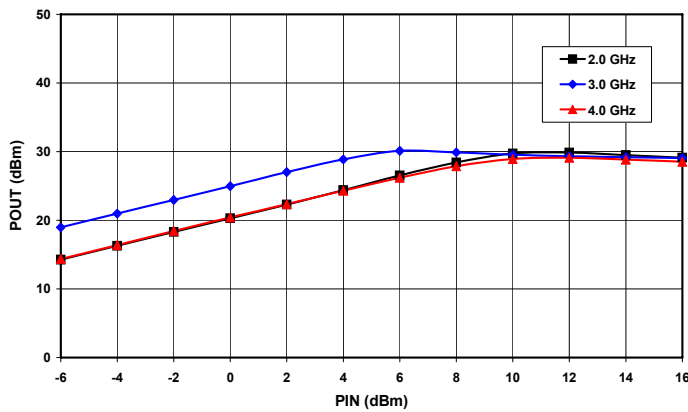


Figure 3. Output Power vs. Input Power at  $V_{DD} = 8V$

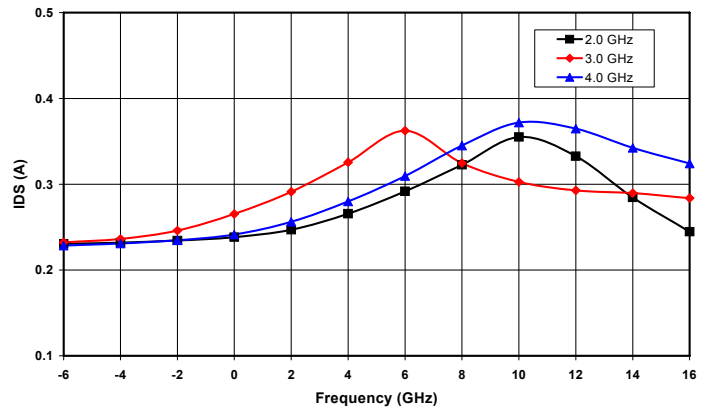


Figure 4. Drain Current vs. Input Power at  $V_{DD} = 8V$

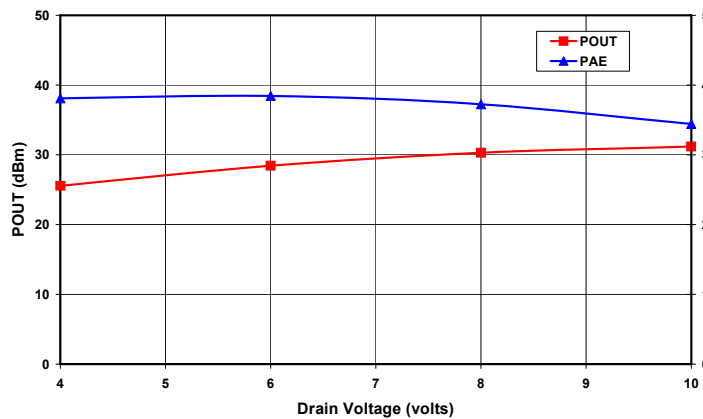


Figure 5. Saturated Output Power and Power Added Efficiency vs. Drain Voltage at  $f_0 = 3.5$  GHz

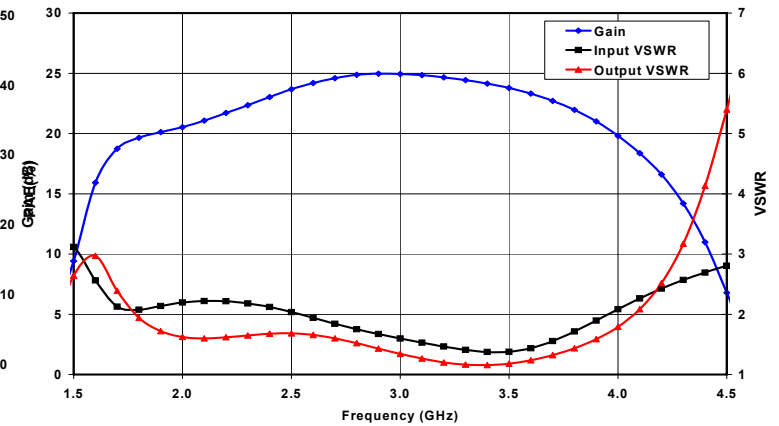
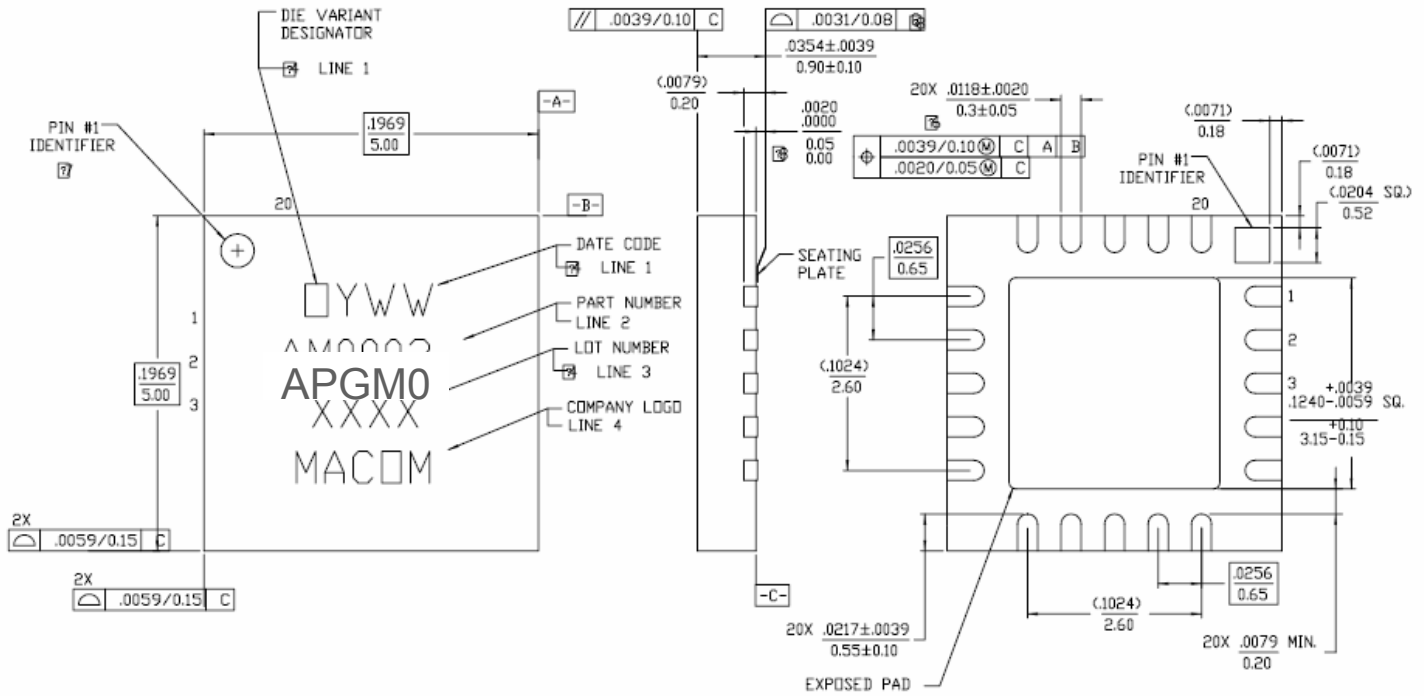


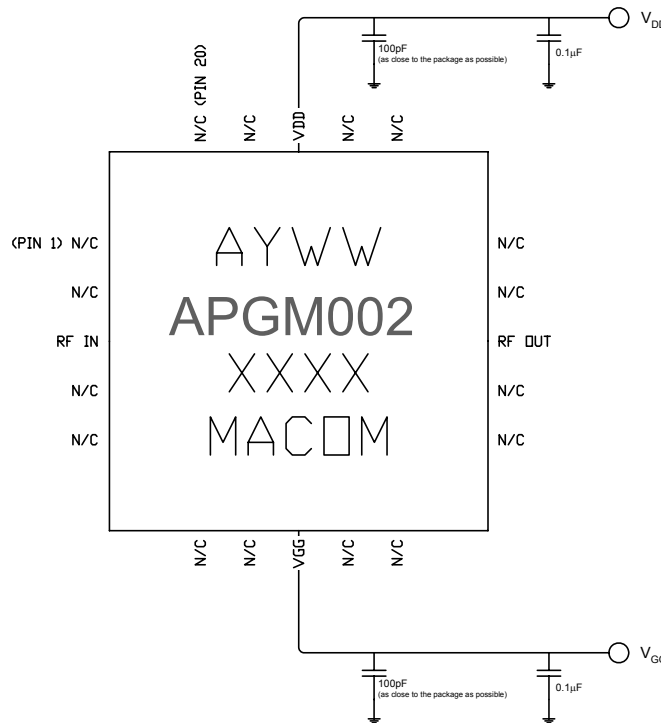
Figure 6. Small Signal Gain and VSWR vs. Frequency at  $V_{DD} = 8V$ .

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**Figure 7. 5x5 mm 20-Lead MLP.**



**Figure 8. Recommended Bias Configuration.**

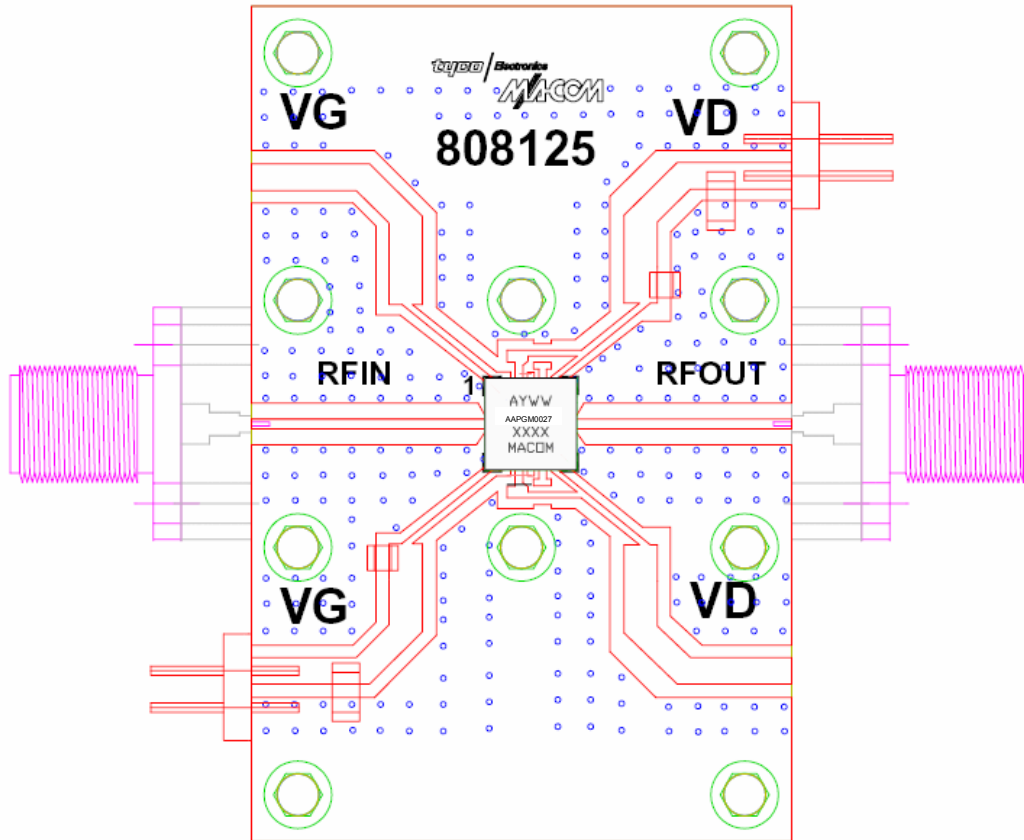


Figure 9. Demonstration Board PN MAAPGM0027-SMB (available upon request).

Refer to M/A-COM Application Note **Surface Mounting Instructions for FQFP-N Packages #S2083\*** for assembly guidelines.

Application Notes can be found by going to the Site Search Page on M/A-COM's web page (<http://www.macom.com/search/search.jsp>) and searching for the required Application Note.