

**1.2W Power Amplifier 9.0-12.0 GHZ**

**MAAPGM0038**

RO-P-DS-3060 E

**Features**

- ◆ Variable Drain Voltage (4-10V) Operation
- ◆ MSAG™ Process
- ◆ High Performance Ceramic Bolt Down Package

**Primary Applications**

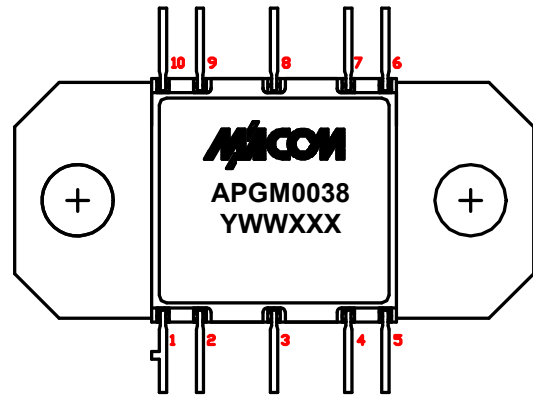
- ◆ Point-to-Point Radio
- ◆ Weather Radar
- ◆ Airborne Radar

**Description**

The MAAPGM0038 is a packaged, 3-stage, 1.2 W power amplifier with on-chip bias networks in a bolt down ceramic package, allowing easy assembly. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate MESFET Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.



Pin Number	RF Designator
1	No Connection
2	V <sub>GG</sub>
3	RF IN
4	V <sub>GG</sub>
5	No Connection
6	No Connection
7	V <sub>DD</sub>
8	RF OUT
9	V <sub>DD</sub>
10	No Connection

**Maximum Operating Conditions <sup>1</sup>**

Parameter	Symbol	Absolute Maximum	Units
Input Power	P <sub>IN</sub>	21.0	dBm
Drain Supply Voltage	V <sub>DD</sub>	+12.0	V
Gate Supply Voltage	V <sub>GG</sub>	-3.0	V
Quiescent Drain Current (No RF, 40% IDSS)	I <sub>DQ</sub>	1.15	A
Quiescent DC Power Dissipated (No RF)	P <sub>DISS</sub>	7.5	W
Junction Temperature	T <sub>J</sub>	180	°C
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C
Processing Temperature		230	°C

1. Operation outside of these ranges may reduce product reliability.

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**Recommended Operating Conditions**

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	$V_{DD}$	4.0	8.0	10.0	V
Gate Supply Voltage	$V_{GG}$	-2.4	-2.0	-1.3	V
Input Power	$P_{IN}$		16.0	19.0	dBm
Junction Temperature	$T_J$			150	°C
Thermal Resistance	$\Theta_{JC}$		12.3		°C/W
Package Base Temperature	$T_B$			Note 2	°C

**2. Maximum Package Base Temperature = 150°C —  $\Theta_{JC} * V_{DD} * I_{DQ}$**

**Electrical Characteristics:  $T_B = 40^\circ\text{C}^2$ ,  $Z_0 = 50 \text{ W}$ ,  $V_{DD} = 8\text{V}$ ,  $I_{DQ} \approx 710 \text{ mA}^3$ ,  $P_{in} = 16 \text{ dBm}$ ,  $R_G \approx 100 \Omega$**

Parameter	Symbol	Minimum	Typical*	Maximum	Units
Bandwidth	f	—	9-12	—	GHz
Output Power	POUT	30.5	31.5	—	dBm
Output Power @ 10.5 GHz	POUT	30.5	31.5	32.5*	dBm
Power Added Efficiency	PAE	—	17	—	%
1-dB Compression Point	P1dB	—	30	—	dBm
Small Signal Gain	G	19	21	—	dB
Small Signal Gain @ 10.5GHz	G	19	21	23*	dB
Input VSWR	VSWR	—	3	5.8	—
Input VSWR @ 10.5 GHz	VSWR	2.3*	3	5.8	—
Output VSWR	VSWR	—	2.5:1	—	—
Gate Supply Current	$I_{GG}$	-10	0	10	mA
Gate Supply Current @ 10.5 GHz	$I_{GG}$	-10	0	10	mA
Drain Supply Current	$I_{DD}$	—	0.9	1.1	A
Drain Supply Current @ 10.5 GHz	$I_{DD}$	0.7*	0.9	1.1	A
Noise Figure	NF	—	9	—	dB
2 <sup>nd</sup> Harmonic	2f	—	-20	—	dBc
3 <sup>rd</sup> Harmonic	3f	—	-36	—	dBc
Output Third Order Intercept	OTOI	—	40	—	dBm
3 <sup>rd</sup> Order Intermodulation Distortion, Single Carrier Level = 21 dBm	IM3	—	-13	—	dBm
5 <sup>th</sup> Order Intermodulation Distortion, Single Carrier Level = 21 dBm	IM5	—	-30	—	dBm

**3. Adjust  $V_{GG}$  between -2.4 to -1.3V to achieve indicated  $I_{DQ}$ . 4. \*Not screened-shown to indicate range of expected values.**



**Operating Instructions**

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply  $V_{GG} \approx -1.7\text{V}$ ,  $V_{DD} = 0 \text{ V}$ .
2. Ramp  $V_{DD}$  to desired voltage, typically 8 V.
3. Adjust  $V_{GG}$  to set  $I_{DQ}$ , (See Note 3 above).
4. Set RF input.
5. Power down sequence in reverse. Turn  $V_{GG}$  off last.

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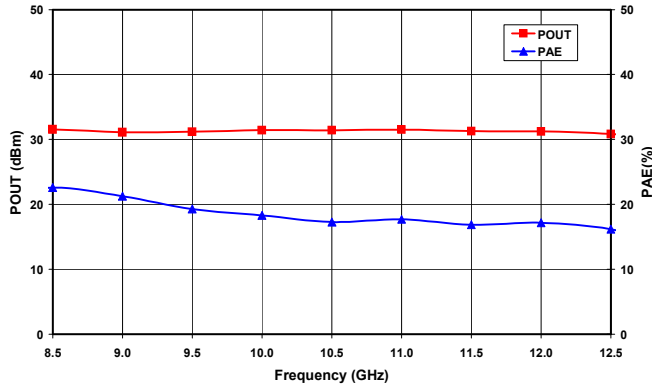


Figure 1. Output Power and Power Added Efficiency vs. Frequency at  $V_{DD} = 8V$  and  $P_{in} = 16$  dBm

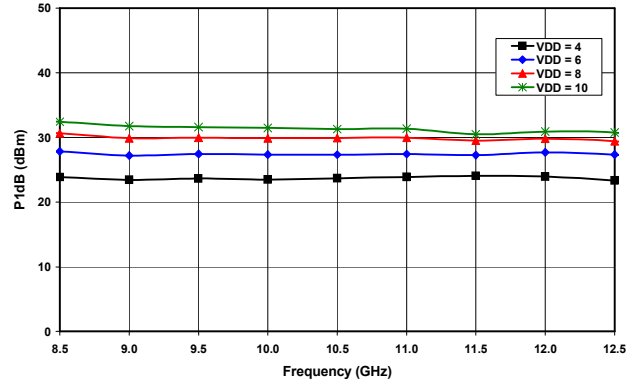


Figure 2. 1dB Compression Point vs. Drain Voltage

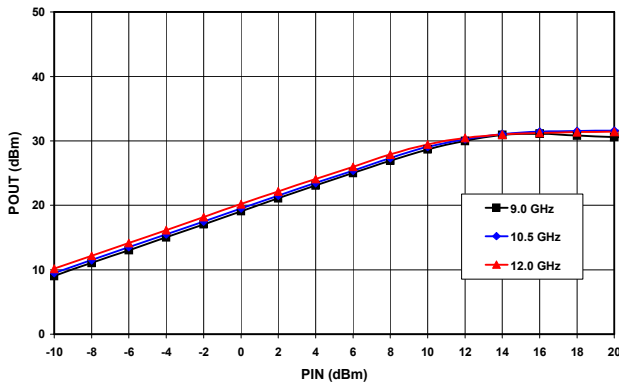


Figure 3. Output Power vs. Input Power at  $V_{DD} = 8V$

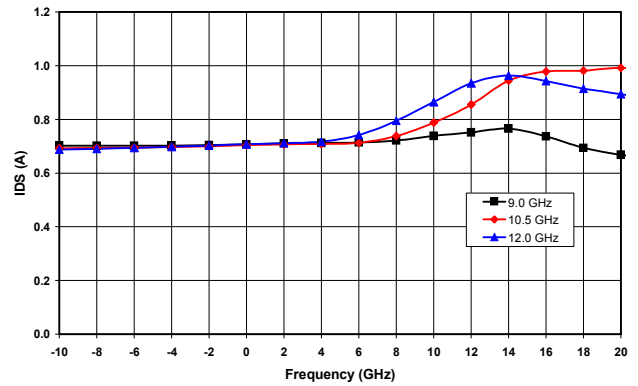


Figure 4. Drain Current vs. Input Power at  $V_{DD} = 8V$

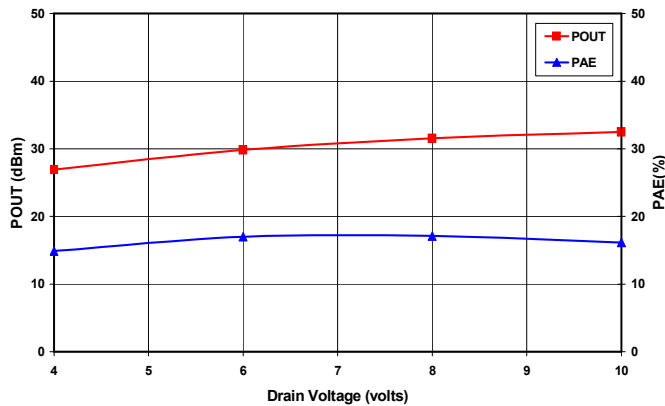


Figure 5. Saturated Output Power and Power Added Efficiency vs. Drain Voltage at  $f_0 = 10.5$  GHz

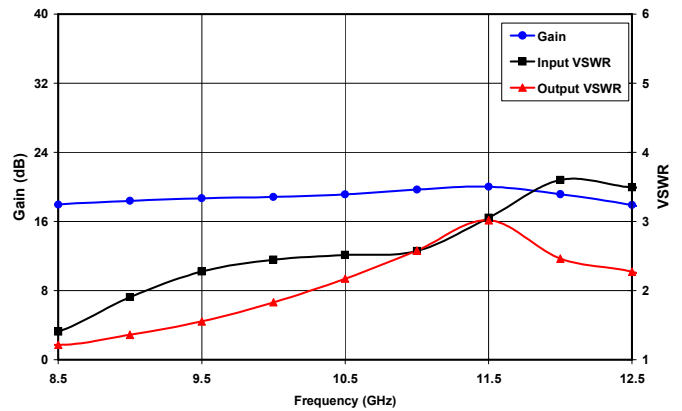
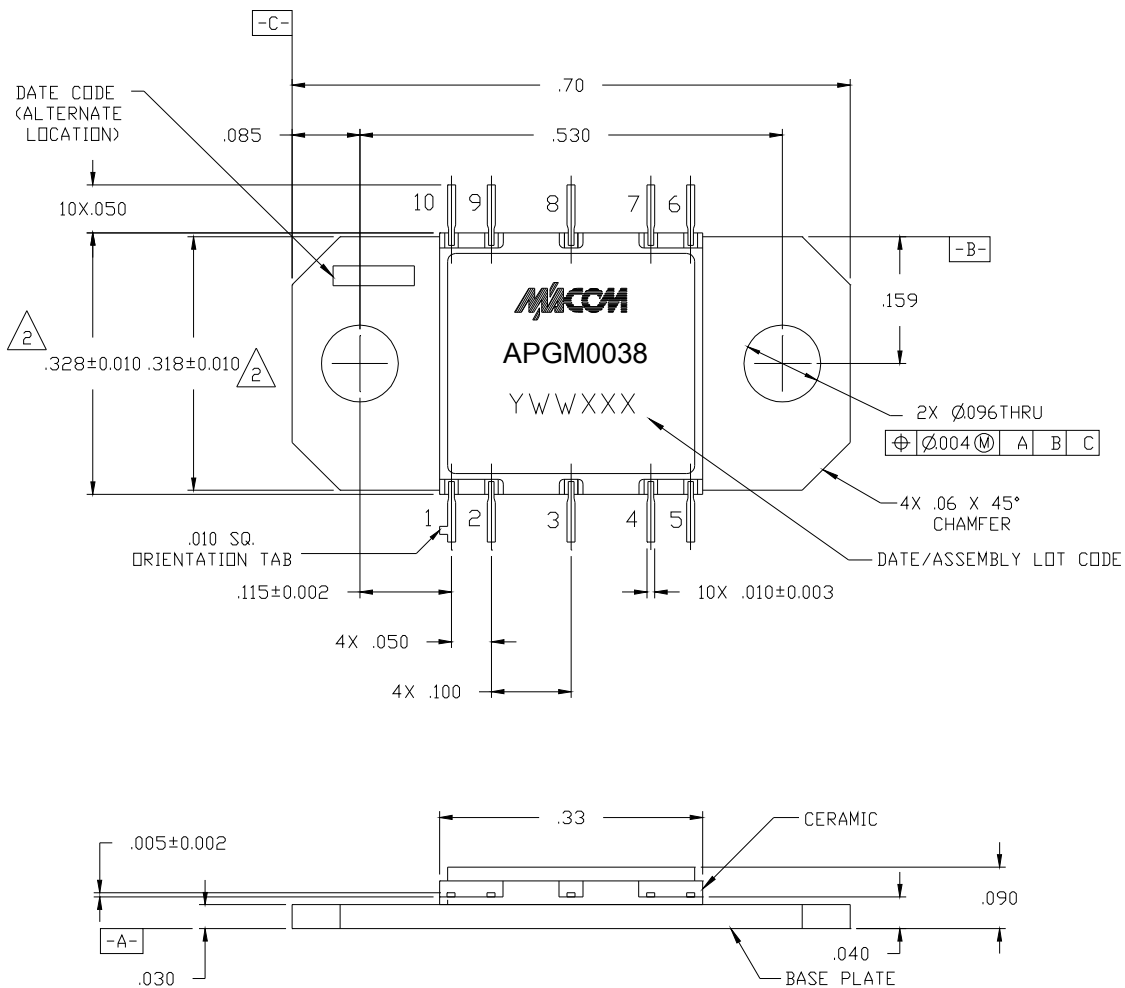


Figure 6. Small Signal Gain and VSWR vs. Frequency at  $V_{DD} = 8V$ .

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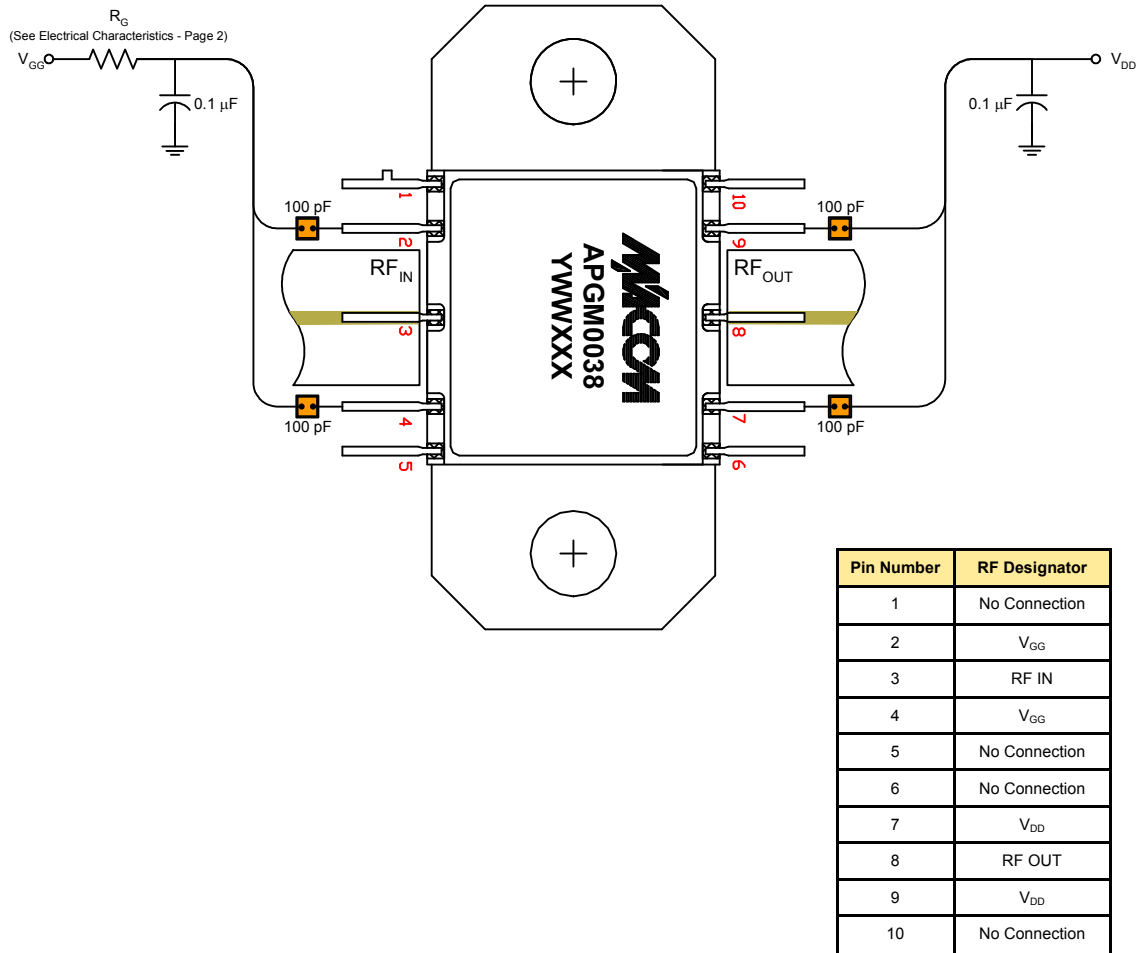
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**Figure 5. CR-15 Package Dimensions**

The CR-15 is a high frequency, low thermal resistance package. The package consists of a cofired ceramic construction with a copper-tungsten base and iron-nickel-cobalt leads. The finish consists of electrolytic gold over nickel plate.

**Figure 6. Recommended Bias Configuration**



**Assembly Instructions:**

This flange mount style package provides a robust interface between a highly integrated GaAs MMIC device and a circuit board which may be assembled using conventional surface mount techniques. A thin shim made of a thermally and electrically conductive, ductile material should be used prior to installation of the CR-15 to improve the thermal and electrical performance of the package to housing interface. Refer to **M/A-COM Application Note #M567\*** for more information .

For applications where surface mount components are to be installed after the CR-15 installation, this package will not be damaged when subjected to typical convection or IR oven reflow profiles. Refer to **M/A-COM Application Note #M538\*** for maximum allowable reflow time and temperature. Alternatively, the package leads may be individually soldered. Whether an iron or hot gas soldering equipment is used, care should be taken to insure that the temperature is well controlled and electric static discharge (ESD) safe.

\* Application Notes can be found by going to the Site Search Page on M/A-COM's web page (<http://www.macom.com/search/search.jsp>) and searching for the required Application Note.

**Biasing Notes:**

- ◆ The 100pF bypass capacitors must be placed as close to the  $V_{GG}$  and  $V_{DD}$  pins as possible (recommended < 100 mils).
- ◆ A negative bias must be applied to  $V_{GG}$  before applying a positive bias to  $V_{DD}$  to prevent damage to the amplifier.