NCP1521

1.5 MHz, 600 mA, High-Efficiency, Low Quiescent Current, Adjustable Output Voltage Step-Down Converter

The NCP1521 step−down PWM DC−DC converter is optimized for portable applications powered from one cell Li−ion or three cell Alkaline/NiCd/NiMH batteries. The device is available in an adjustable output voltage from 0.9 V to 3.3 V. It uses synchronous rectification to increase efficiency and reduce external part count. The device also has a built−in 1.5 MHz (nominal) oscillator which reduces component size by allowing a small inductor and capacitors. Automatic switching PWM/PFM mode offers improved system efficiency.

Finally, it includes an integrated soft−start, cycle−by−cycle current limiting, and thermal shutdown protection. The NCP1521 is available in space saving, low profile TSOP5 and UDFN6 packages.

Features

- 95.3% of Efficiency for 3.3 V Output and 4.2 V Input and 80 mA Load−Current
- Sources up to 600 mA
- 1.5 MHz Switching Frequency
- Adjustable Output Voltage from 0.9 V to 3.3 V
- 30 μA Quiescent Current
- Synchronous Rectification for Higher Efficiency
- 2.7 V to 5.5 V Input Voltage Range
- Thermal Limit Protection
- Shutdown Current Consumption of 0.3 μA
- Short Circuit Protection
- This is a Pb−Free Device

Typical Applications

- Cellular Phones, Smart Phones and PDAs
- Digital Still/Video Cameras
- MP3 Players and Portable Audio Systems
- Wireless and DSL Modems
- Portable Equipment
- USB Powered Devices

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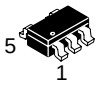
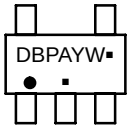
MARKING DIAGRAM



TSOP−5
SN SUFFIX
CASE 483



DBP = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

UDFN6
MU SUFFIX
CASE 517AB

ZC = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping
NCP1521ASNT1G	TSOP−5 (Pb−Free)	3000/Tape & Reel
NCP1521AMUTBG	UDFN6 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

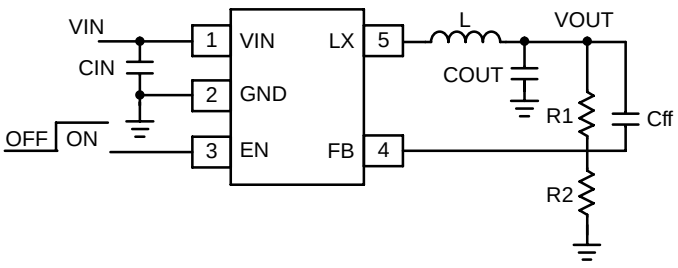


Figure 1. Typical Application − TSOP−5

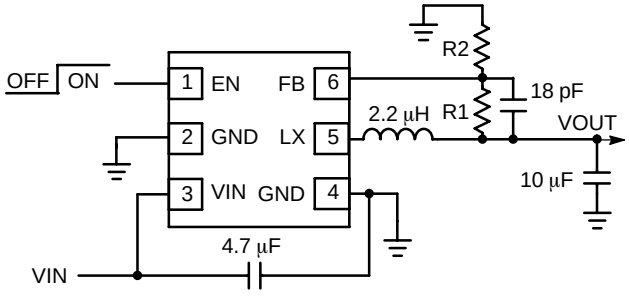


Figure 2. Typical Application − UDFN6

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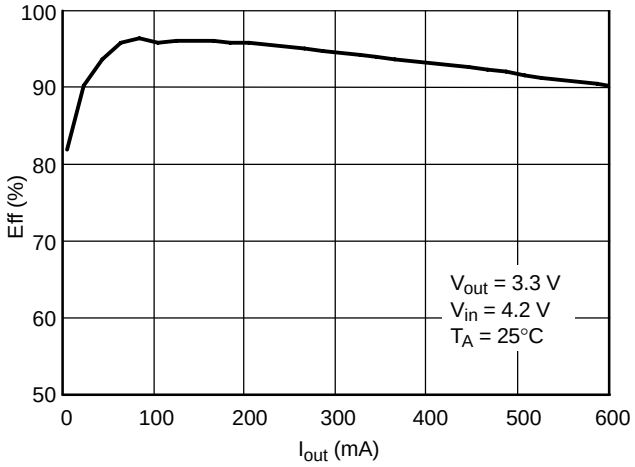


Figure 3. Efficiency vs. Output Current

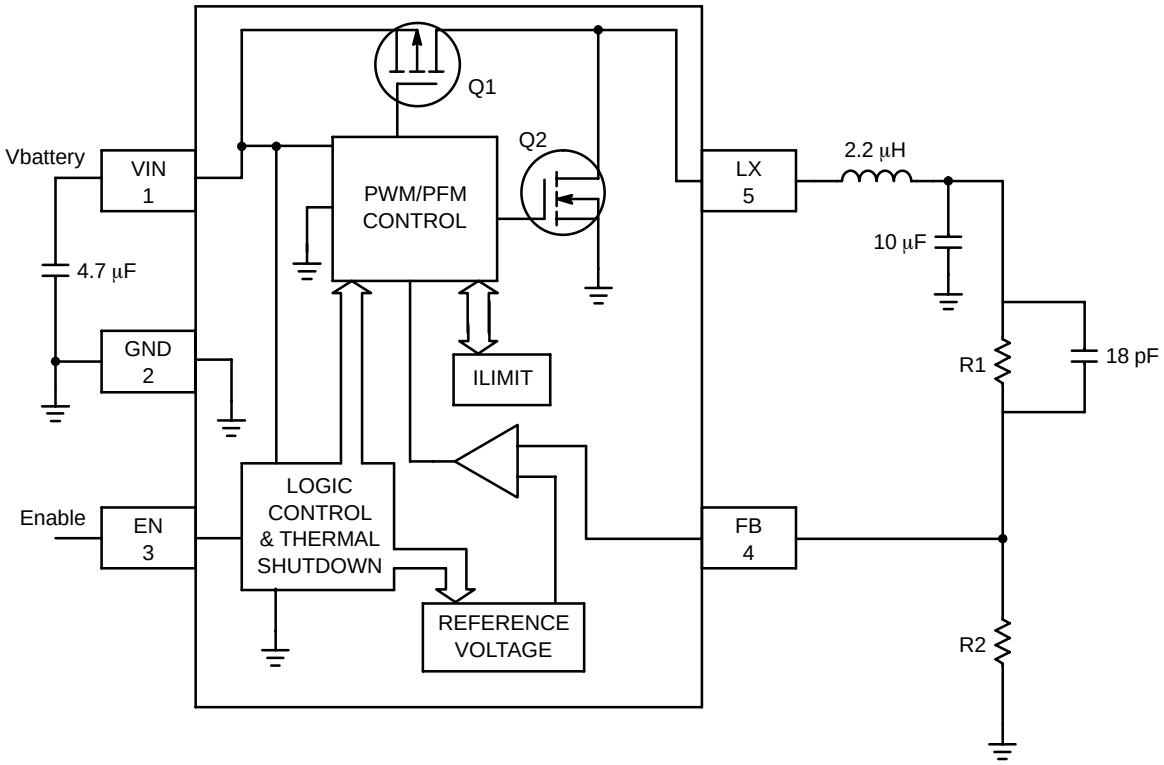


Figure 4. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. TSOP5	Pin No. UDFN6	Symbol	Function	Description
1	3	VIN	Analog Input	Power Supply Input for Analog V_{CC}.
2	2, 4	GND	Analog/Power Ground	Ground connection for the NFET Power Stage and the Analog Sections of the IC.
3	1	EN	Digital Input	Enable for Switching Regulator. This pin is active high. Do not float this pin.
4	6	FB	Analog Input	Feedback voltage from the output of the power supply. This is the input to the error amplifier.
5	5	LX	Analog Output	Connection from Power MOSFETs to the Inductor. For one option, an output discharge circuit sinks current from this pin.

PIN CONNECTIONS

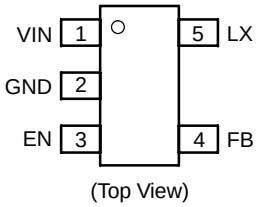


Figure 5. Pin Connections − TSOP5

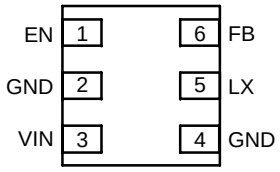


Figure 6. Pin Connections − UDFN6

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Minimum Voltage All Pins		V_{min}	−0.3	V
Maximum Voltage All Pins (Note 2)		V_{max}	7.0	V
Maximum Voltage Enable, FB, LX		V_{max}	VIN + 0.3	V
Thermal Resistance, Junction −to−Air	TSOP5 UDFN6	$R_{\theta JA}$	200 TBD	°C/W
Operating Ambient Temperature Range		T_A	−40 to 85	°C
Storage Temperature Range		T_{stg}	−55 to 150	°C
Junction Operating Temperature		T_j	−40 to 125	°C
Latch−up Current Maximum Rating (T_A = 85°C) (Note 4)		Lu	+/−100	mA
ESD Withstand Voltage (Note 3) Human Body Model Machine Model		Vesd	 2.0 200	 kV V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = 25°C.
2. According to JEDEC standard JESD22−A108B.
3. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) per JEDEC standard: JESD22−A114.
   Machine Model (MM) per JEDEC standard: JESD22−A115.
4. Latchup current maximum rating per JEDEC standard: JESD78.

ELECTRICAL CHARACTERISTICS (Typical values are referenced to T_A = +25°C, Min and Max values are referenced −40°C to +85°C ambient temperature, unless otherwise noted, operating conditions V_{IN} = 3.6 V, V_{OUT} = 1.8 V, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}	2.7	−	5.5	V
Undervoltage Lockout (V_{IN} Falling)	V_{UVLO}	2.3	2.5	2.6	V
Quiescent Current PFM No Load	I_q	−	30	45	μA
Standby Current, EN Low	Istb	−	0.3	1.2	μA
Oscillator Frequency	F_{osc}	1.3	1.5	1.8	MHz
Peak Inductor Current	I_{LIM}	−	1200	−	mA
Feedback Reference Voltage	V_{ref}	−	0.6	−	V
FB Pin Tolerance Overtemp @ I_{out} = 100 mA	VFBtol	−3.0	−	3.0	%
Reference Voltage Line Regulation	ΔVFB	−	0.1	−	%
Output Voltage Accuracy @ I_{out} = 100 mA (Note 5)	V_{OUT}	−3%	Vnom	+3%	V
Minimum Output Voltage	V_{OUT}	−	0.9	−	V
Maximum Output Voltage	V_{OUT}	−	3.3	−	V
Output Voltage Line Regulation (V_{in} = 2.7–5.5) Io = 100 mA	ΔV_{OUT}	−	0.1	−	%
Voltage Load Regulation (IO = 100 mA to 300 mA) (IO = 100 mA to 600 mA)	$V_{LOADREG}$	 − −	 0.0005 0.001	 − −	 %/mA %/mA
Load Transient Response (300 mA to 600 mA Load Step, Trise 10 μs)	V_{OUT}	−	50	−	mV
Duty Cycle	−	−	−	100	%
P−Ch On−Resistance	RLxH	−	300	−	mΩ
N−Ch On−Resistance	RLxL	−	300	−	mΩ
P−Ch Leakage Current	ILeakH	−	0.05	−	μA
N−Ch Leakage Current	ILeakL	−	0.01	−	μA
Enable Pin High	VENH	1.2	−	−	V
Enable Pin Low	VENL	−	−	0.4	V
EN << H >> Input Current, EN = 3.6 V	IENH	−	2.0	−	μA
Soft−Start Time	T_{start}	−	350	500	μs
Thermal Shutdown Threshold	T_{SD}	−	160	−	°C
Thermal Shutdown Hysteresis	T_{SDH}	−	25	−	°C

5. The overall output voltage tolerance depends upon the accuracy of the external resistor (R1, R2).

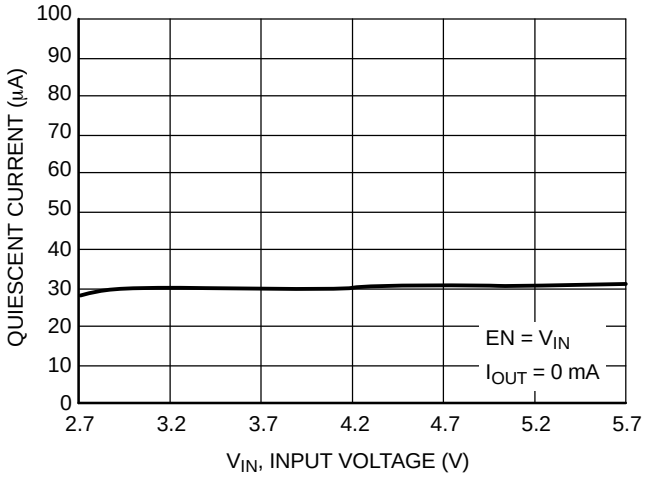


Figure 7. Quiescent Current vs. Supply Voltage

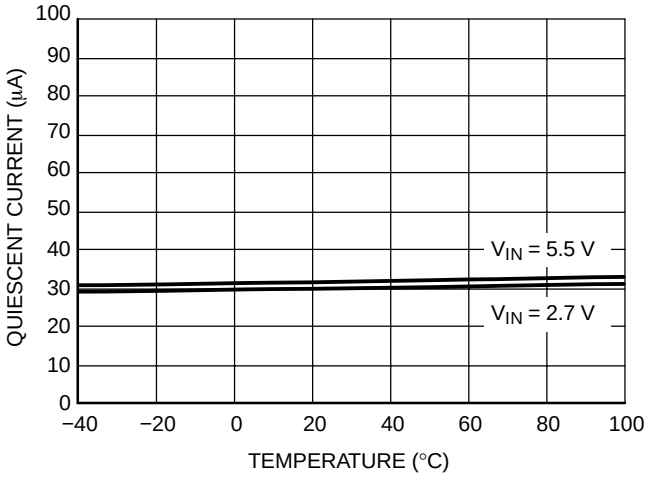


Figure 8. Quiescent Current vs. Temperature

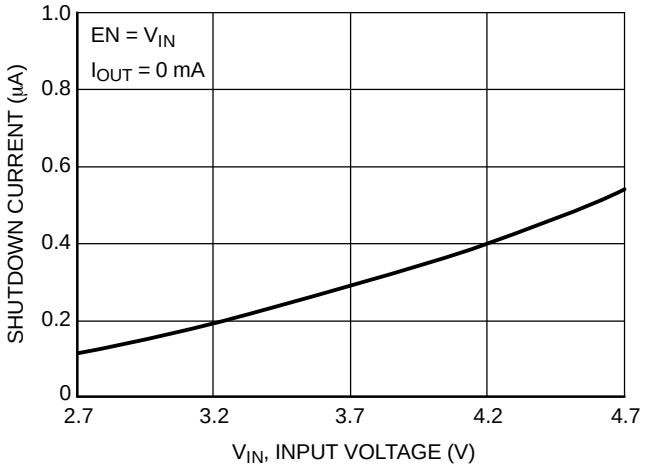


Figure 9. Shutdown Current vs. Supply Voltage

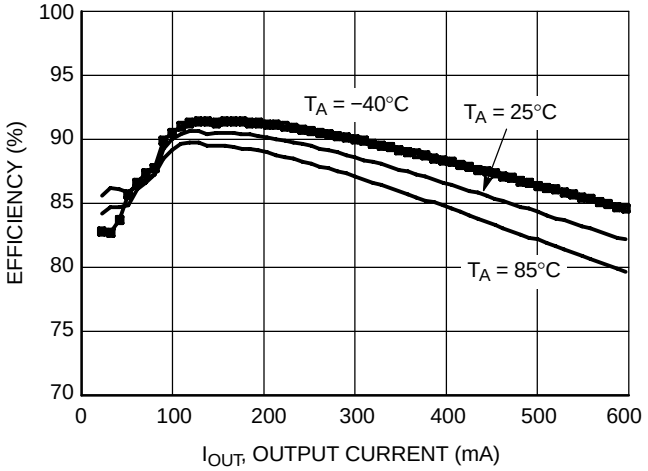


Figure 10. Efficiency vs. Output Current (V_{OUT} = 1.8 V, V_{IN} = 3.6 V)

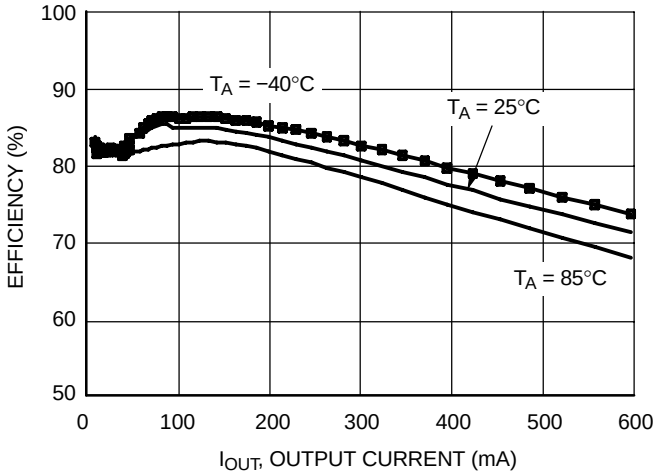


Figure 11. Efficiency vs. Output Current (V_{OUT} = 0.9 V, V_{IN} = 3.6 V)

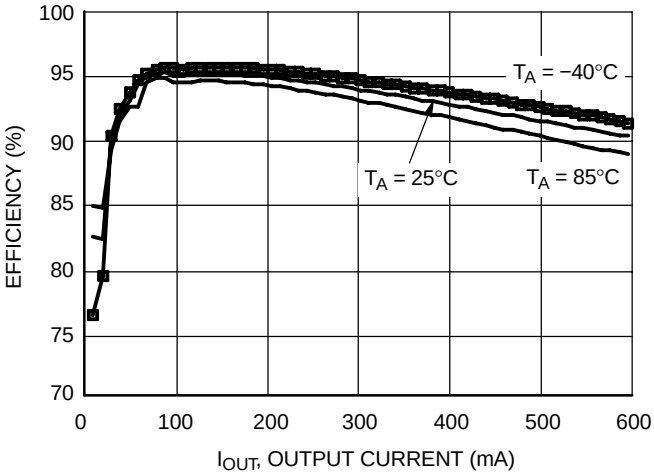


Figure 12. Efficiency vs. Output Current (V_{OUT} = 3.3 V, V_{IN} = 4.5 V)

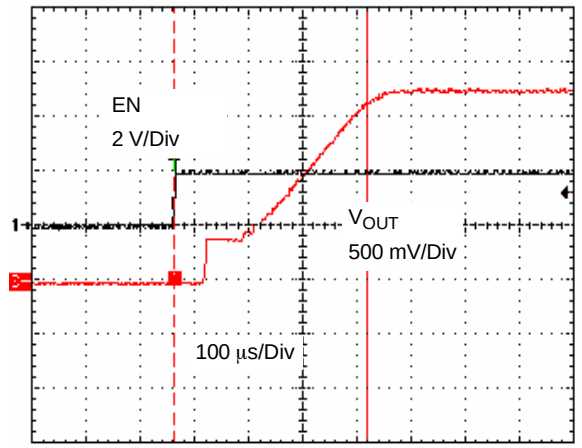


Figure 13. Soft Start Time (V_{IN} = 3.6 V)

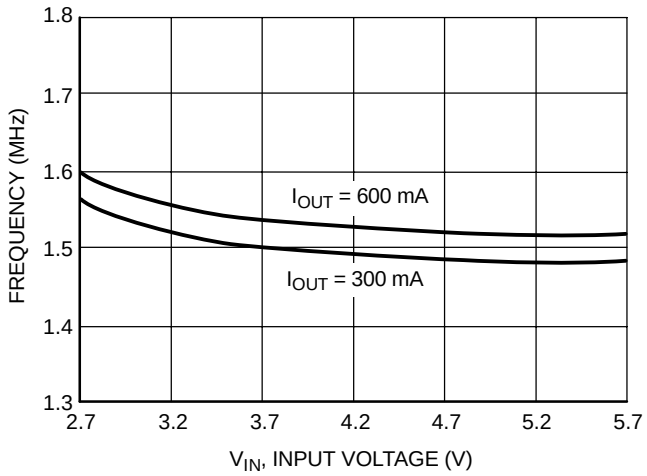


Figure 14. Frequency vs. Input Voltage

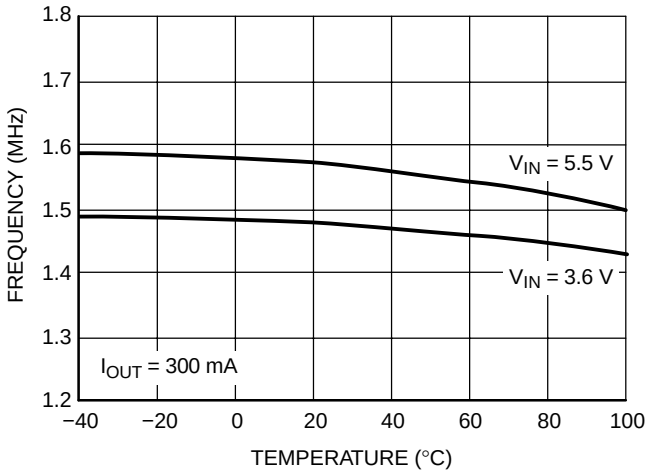


Figure 15. Frequency vs. Temperature

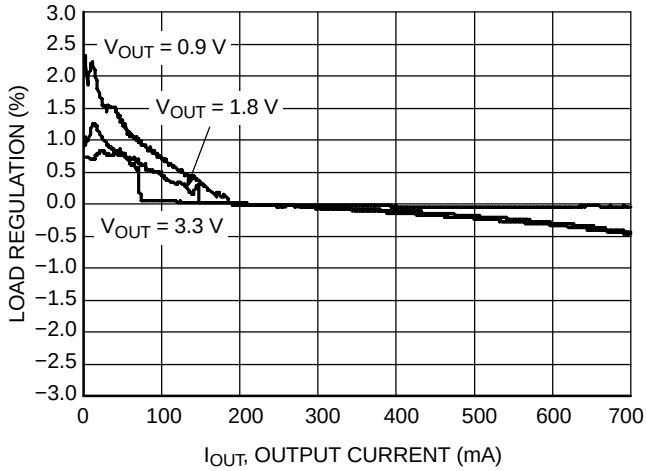


Figure 16. Load Regulation

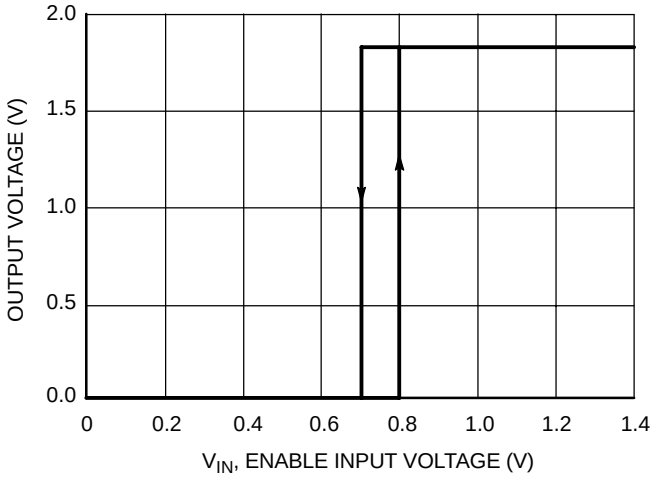


Figure 17. Output Voltage vs. Enable Input Pin Voltage

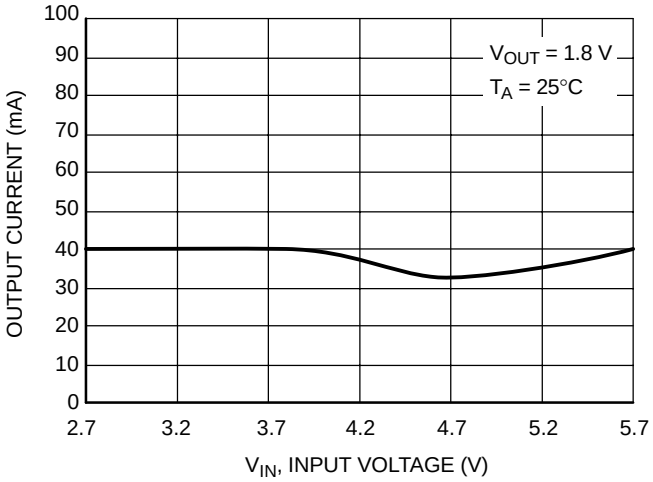


Figure 18. PFM/PWM Threshold vs. Input Voltage

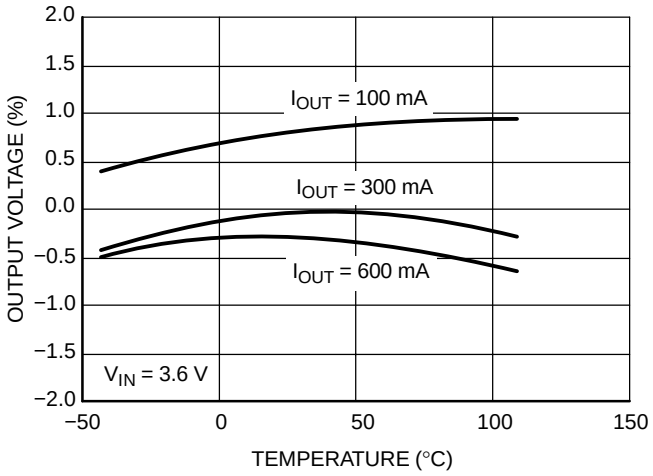


Figure 19. Output Voltage Accuracy (V_{OUT} = 0.9 V)

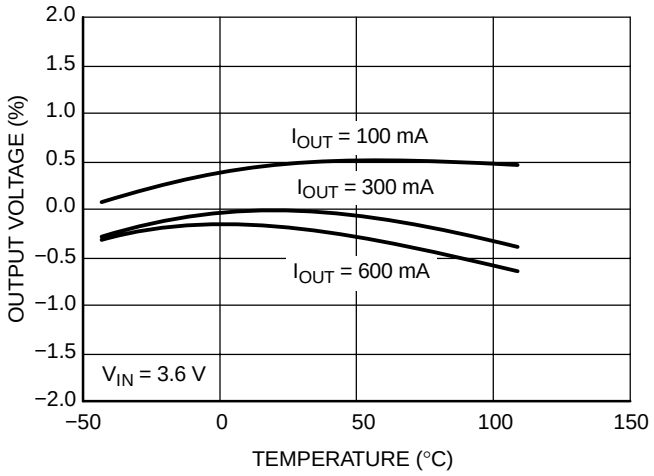


Figure 20. Output Voltage Accuracy (V_{OUT} = 1.8 V)

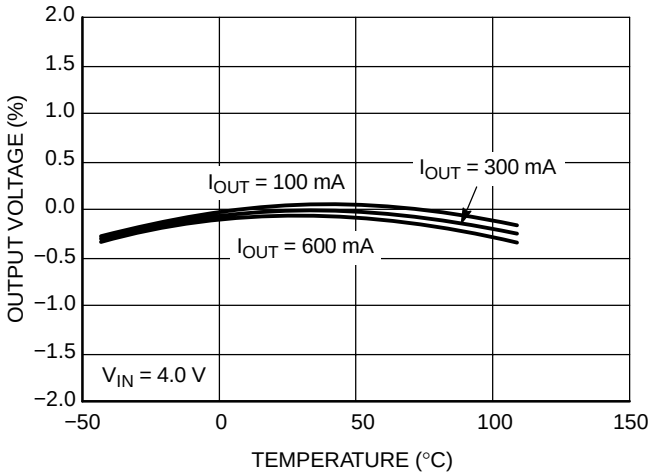


Figure 21. Output Voltage Accuracy (V_{OUT} = 3.3 V)

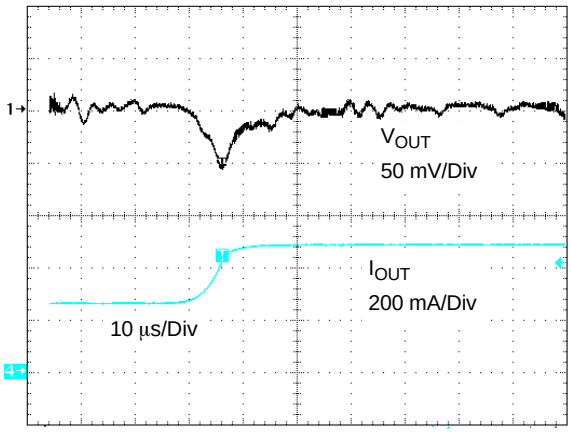


Figure 22. Load Transient Response in PWM Operation (V_{IN} = 3.6 V)

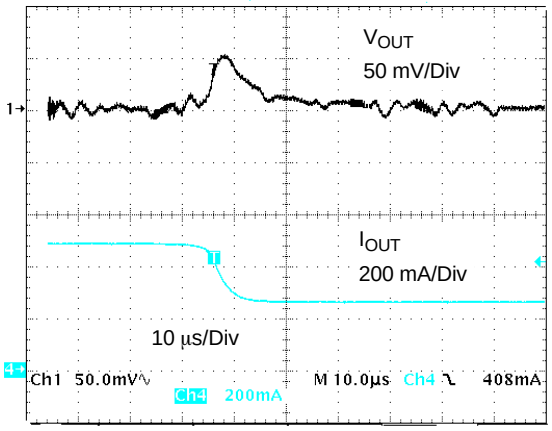


Figure 23. Load Transient Response in PWM Operation (V_{IN} = 3.6 V)

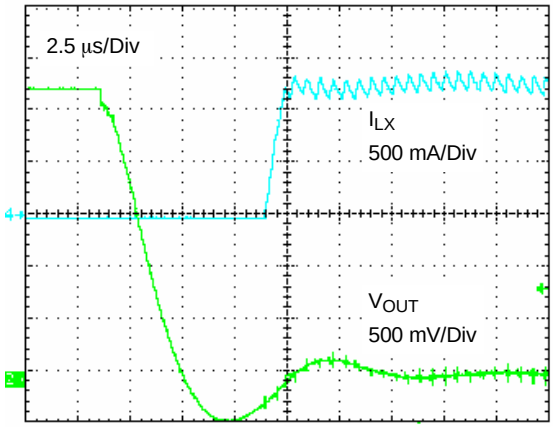


Figure 24. Short Circuit Protection (V_{IN} = 3.6 V)

OPERATION DESCRIPTION

Overview

The NCP1521 uses a constant frequency, current mode step−down architecture. Both the main (P−Channel MOSFET) and synchronous (N−Channel MOSFET) switches are internal.

It delivers a constant voltage from either a single Li−Ion or three cell NiMH/NiCd battery to portable devices such as cell phones and PDA. The output voltage is set by the external resistor divider. The NCP1521 sources at least 600 mA, depending on external components chosen.

The NCP1521 works with two modes of operation; PWM/PFM depending on the current required. The device operates in PWM mode at load currents of approximately 40 mA or higher, having voltage tolerance of ±3% with 90% efficiency or better. Lighter load currents cause the device to automatically switch into PFM mode for reduced current consumption (I_Q = 30 μA typ) and extended battery life.

Additional features include soft−start, undervoltage protection, current overload protection, and thermal shutdown protection. As shown in Figure 1, only six external components are required for implementation. The part uses an internal reference voltage of 0.6 V. It is recommended to keep the part in shutdown until the input voltage is 2.7 V or higher.

PWM Operating Mode

In this mode, the output voltage of the NCP1521 is regulated by modulating the on−time pulse width of the main switch Q1 at a fixed frequency of 1.5 MHz. The switching of the PMOS Q1 is controlled by a flip−flop driven by the internal oscillator and a comparator that compares the error signal from an error amplifier with the sum of the sensed current signal and compensation ramp. At the beginning of each cycle, the main switch Q1 is turned ON by the rising edge of the internal oscillator clock. The inductor current ramps up until the sum of the current sense signal and compensation ramp becomes higher than the error voltage amplifier. Once this has occurred, the PWM comparator resets the flip−flop, Q1 is turned OFF and the synchronous switch Q2 is turned ON. Q2 replaces the external Schottky diode to reduce the conduction loss and improve the efficiency. To avoid overall power loss, a certain amount of dead time is introduced to ensure Q1 is completely turned OFF before Q2 is being turned ON.

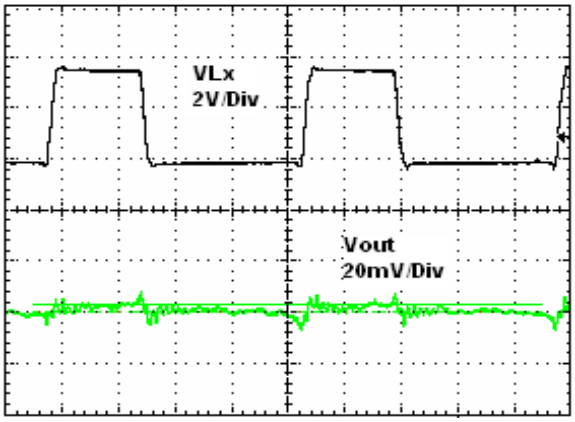


Figure 25. PWM Switching Waveform (V_{in} = 3.6 V, V_{out} = 1.8 V, I_{out} = 300 mA)

PFM Operating Mode

Under light load conditions (<40 mA), the NCP1521 enters in low current PFM mode operation to reduce power consumption. The output regulation is implemented by pulse frequency modulation. If the output voltage drops below the threshold of PFM comparator (typically Vnom−2%), a new cycle will be initiated by the PFM comparator to turn on the switch Q1. Q1 remains ON until the peak inductor current reaches 200 mA (nom). Then I_{LIM} comparator goes high to switch off Q1. After a short dead time delay, switch rectifier Q2 is turned ON. The negative current detector (NCD) will detect when the inductor current drops below zero and sends the signal to turn off Q2. The output voltage continues to decrease through discharging the output capacitor. When the output voltage falls below the threshold of the PFM comparator, a new cycle starts immediately.

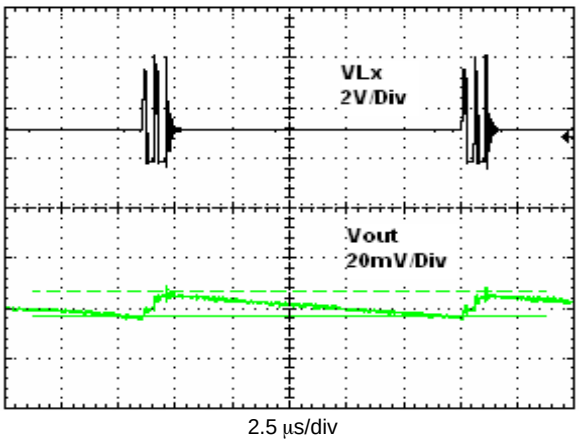


Figure 26. PFM Mode Switching Waveform (V_{in} = 3.6 V, V_{out} = 1.8 V, I_{out} = 30 mA)

Cycle−by−Cycle Current Limitation

From the block diagram (Figure 4), an I_{LIM} comparator is used to realize cycle−by−cycle current limit protection. The comparator compares the LX pin voltage with the reference voltage, which is biased by a constant current. If the inductor current reaches the limit, the I_{LIM} comparator detects the LX voltage falling below the reference voltage and releases the signal to turn off the switch Q1. The cycle−by−cycle current limit is set at 1200 mA (nom).

Short Circuit Protection

When the output is shorted to ground, the device limits the inductor current. The duty−cycle is minimum and the consumption on the input line is 300 mA (Typ). When the short circuit condition is removed, the device returns to the normal mode of operation.

Soft−Start

The NCP1521 uses soft−start (300 μs Typ) to limit the inrush current when the device is initially enabled. Soft−start is implemented by gradually increasing the reference voltage until it reaches the full reference voltage. During startup, a pulsed current source charges the internal soft−start capacitor to provide gradually increasing reference voltage. When the voltage across the capacitor ramps up to the nominal reference voltage, the pulsed current source will be switched off and the reference voltage will switch to the regular reference voltage.

Shutdown Mode

When the EN pin has a voltage applied of less than 0.4 V, the NCP1521 will be disabled. In shutdown mode, the internal reference, oscillator and most of the control circuitries are turned off. Therefore, the typical current consumption will be 0.3 μA (typical value). Applying a voltage above 1.2 V to EN pin will enable the device for normal operation. The typical threshold is around 0.7 V. The device will go through soft−start to normal operation, however, the EN pin should be tied low while the input voltage on V_{IN} pin is rising up.

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. If the junction temperature exceeds 160°C, the device shuts down. In this mode switch Q1 and Q2 and the control circuits are all turned off. The device restarts in soft−start after the temperature drops below 135°C. This feature is provided to prevent catastrophic failures from accidental device overheating, and it is not intended as a substitute for proper heatsinking.

Low Dropout Operation

The NCP1521 offers a low input to output voltage difference. The NCP1521 can operate at 100% duty cycle. In this mode the PMOS (Q1) switches completely on.

The minimum input voltage to maintain regulation can be calculated as:

$$V_{IN(min)} = V_{OUT(max)} + (I_{OUT} \times (R_{DS(on)} + R_{INDUCTOR})) \quad \text{(eq. 1)}$$

- V_{OUT}: Output Voltage (Volts)
- I_{OUT}: Max Output Current
- $R_{DS(on)}$: P−Channel Switch $R_{DS(on)}$
- $R_{INDUCTOR}$: Inductor Resistance (DCR)

APPLICATION INFORMATION

Output Voltage Selection

The output voltage is programmed through an external resistor divider connected from V_{OUT} to FB then to GND. For low power consumption and noise immunity, the resistor from FB to GND (R2) should be in the [100 k−600 k] range. If R2 is 200 k given the V_{FB} is 0.6 V, the current through the divider will be 3.0 μA.

The formula below gives the value of V_{OUT}, given the desired R1 and the R1 value:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad \text{(eq. 2)}$$

- V_{OUT}: Output Voltage (Volts)
- V_{FB}: Feedback Voltage = 0.6 V
- R1: Feedback Resistor from V_{OUT} to FB
- R2: Feedback Resistor from FB to GND

Input Capacitor Selection

In PWM operating mode, the input current is pulsating with large switching noise. Using an input bypass capacitor can reduce the peak current transients drawn from the input supply source, thereby reducing switching noise significantly. The capacitance needed for the input bypass capacitor depends on the source impedance of the input supply.

The maximum RMS current occurs at 50% duty cycle with maximum output current, which is IO, max/2.

For NCP1521, a low profile, low ESR ceramic capacitor of 4.7 μF should be used for most of the cases. For effective bypass results, the input capacitor should be placed as close as possible to the V_{IN} pin.

Table 1. List of Input Capacitor

Murata	GRM188R60J475KE
	GRM21BR71C475KA
Taiyo Yuden	JMK212BY475MG
TDK	C2012X5ROJ475KB
	C1632X5ROJ475KT

Output L−C Filter Design Considerations

The NCP1521 is built in 1.5 MHz frequency and uses current mode architecture. The correct selection of the output filter ensures good stability and fast transient response.

Due to the nature of the buck converter, the output L−C filter must be selected to work with internal compensation. For NCP1521, the internal compensation is internally fixed and it is optimized for an output filter of L = 2.2 μH and C_{OUT} = 10 μF.

The corner frequency is given by:

$$f_c = \frac{1}{2\pi\sqrt{L \times C_{OUT}}} = \frac{1}{2\pi\sqrt{2.2\ \mu H \times 10\ \mu F}} = 34\ kHz \quad \text{(eq. 3)}$$

The device is intended to operate with inductance values between 1.0 μH and maximum of 4.7 μH.

If the corner frequency is moved, it is recommended to check the loop stability depending on the output ripple voltage accepted and output current required. For lower frequency, the stability will be increased; a larger output capacitor value could be chosen without critical effect on the system. On the other hand, a smaller capacitor value increases the corner frequency and it should be critical for the system stability. Take care to check the loop stability. The phase margin is usually higher than 45°.

Table 2. L−C Filter Example

Inductance (L)	Output Capacitor (C_{out})
1.0 μH	22 μF
2.2 μH	10 μF
4.7 μH	4.7 μF

Inductor Selection

The inductor parameters directly related to device performances are saturation current and DC resistance and inductance value. The inductor ripple current (ÄI$_L$) decreases with higher inductance:

$$\Delta I_L = \frac{V_{OUT}}{L \times f_{SW}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \text{(eq. 4)}$$

ΔI_L peak to peak inductor ripple current

L inductor value

f_{SW} switching frequency

The saturation current of the inductor should be rated higher than the maximum load current plus half the ripple current:

$$I_{L(MAX)} = I_{O(MAX)} + \frac{\Delta I_L}{2} \quad \text{(eq. 5)}$$

$\Delta I_{L(MAX)}$ Maximum inductor current

$\Delta I_{O(MAX)}$ Maximum Output current

The inductor's resistance will factor into the overall efficiency of the converter. For best performances, the DC resistance should be less than 0.3 Ω for good efficiency.

Table 3. List of Inductor

FDK	MIPW3226 Series
TDK	VLF3010AT Series
Taiyo Yuden	LQ CBL2012
Coil craft	DO1605−T Series
	LPO3010

Output Capacitor Selection

Selecting the proper output capacitor is based on the desired output ripple voltage. Ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended. The output capacitor requires either an X7R or X5R dielectric.

The output ripple voltage in PWM mode is given by:

$$\Delta V_{OUT} = \Delta I_L \times \left(\frac{1}{4 \times f_{SW}^{-3} \times C_{OUT}} + ESR \right) \text{ (eq. 6)}$$

In PFM mode (at light load), the output voltage is regulated by pulse frequency modulation. The output voltage ripple is independent of the output capacitor value. It is set by the threshold of PFM comparator.

Table 4. List of Output Capacitor

Murata	GRM188R60J475KE	4.7 μF
	GRM21BR60J106ME19L	10 μF
	GRM188R60OJ106ME	10 μF
Taiyo Yuden	JMK212BY475MG	4.7 μF
	JMK212BJ106MG	10 μF
TDK	C2012X5ROJ475KB	4.7 μF
	C2012X5ROJ226M	22 μF
	C2012X5ROJ106K	10 μF

Feed−Forward Capacitor Selection

The feed−forward capacitor sets the feedback loop response and is critical to obtain good loop stability.

Given that the compensation is internally fixed, a fixed 18 pF or higher ceramic capacitor is needed. Choose a small ceramic capacitor X7R or X5R or COG dielectric.

APPLICATION BOARD

PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise and unwanted feedback that can affect the performance of the converter. Hints suggested below can be used as a guideline in most situations.

1. Use star−ground connection to connect the IC ground nodes and capacitor GND nodes together at one point. Keep them as close as possible, and then connect this to the ground plane through several vias. This will reduce noise in the ground plane by preventing the switching currents from flowing through the ground plane.
2. Place the power components (i.e., input capacitor, inductor and output capacitor) as close together as possible for best performance. All connecting traces must be short, direct, and wide to reduce voltage errors caused by resistive losses through the traces.
3. Separate the feedback path of the output voltage from the power path. Keep this path close to the NCP1521 circuit. And also route it away from noisy components. This will prevent noise from coupling into the voltage feedback trace.
4. Place the DC−DC converter away from noise sensitive circuitry, such as RF circuits.

The following shows the NCP1521 demo board schematic, layout, and bill of materials:

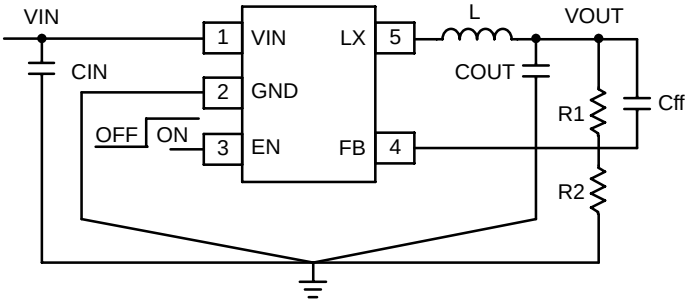


Figure 27. NCP1521 Board Schematic

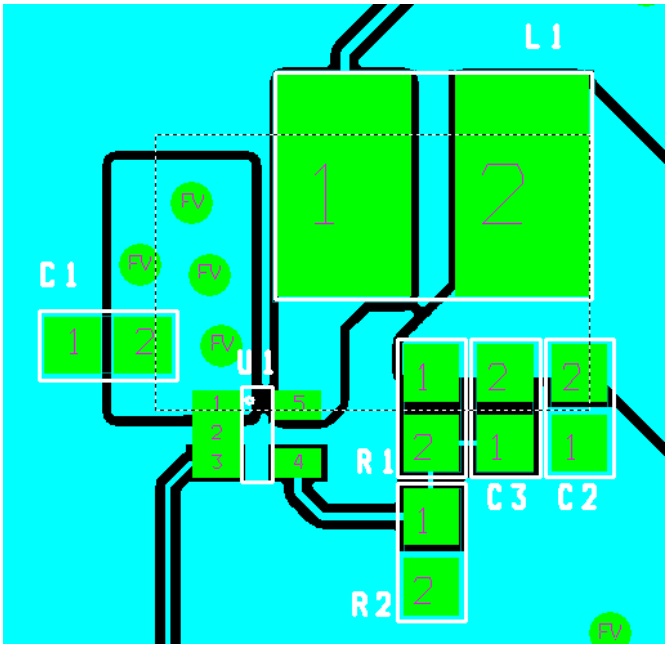


Figure 28. NCP1521 Board Layout

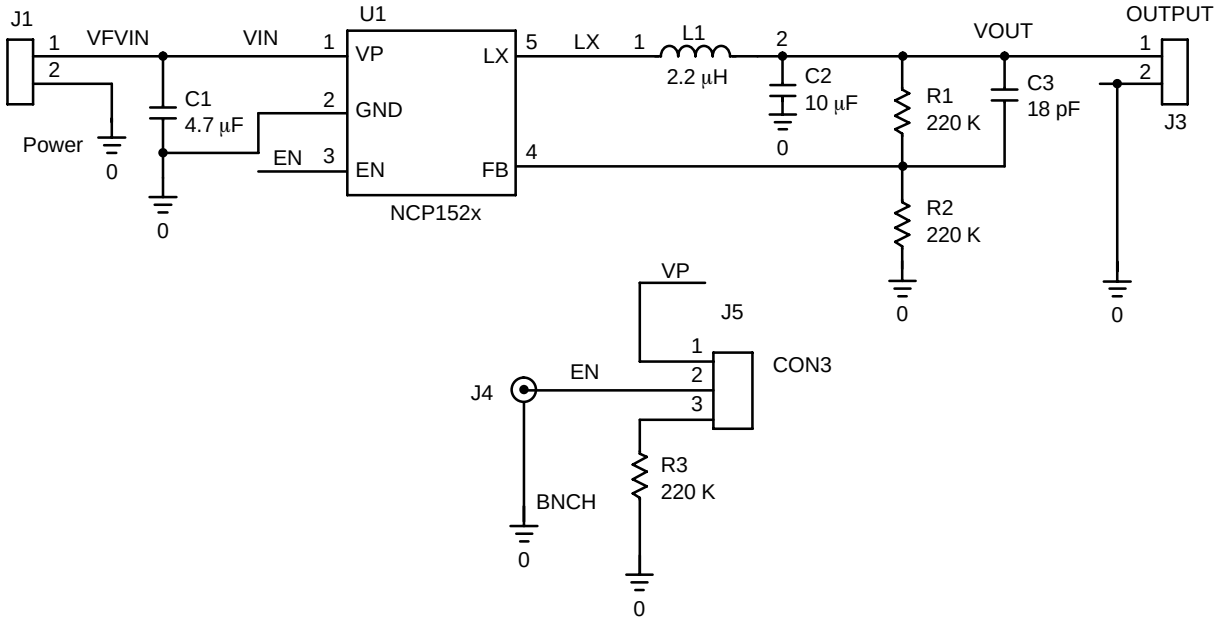


Figure 29. Schematics

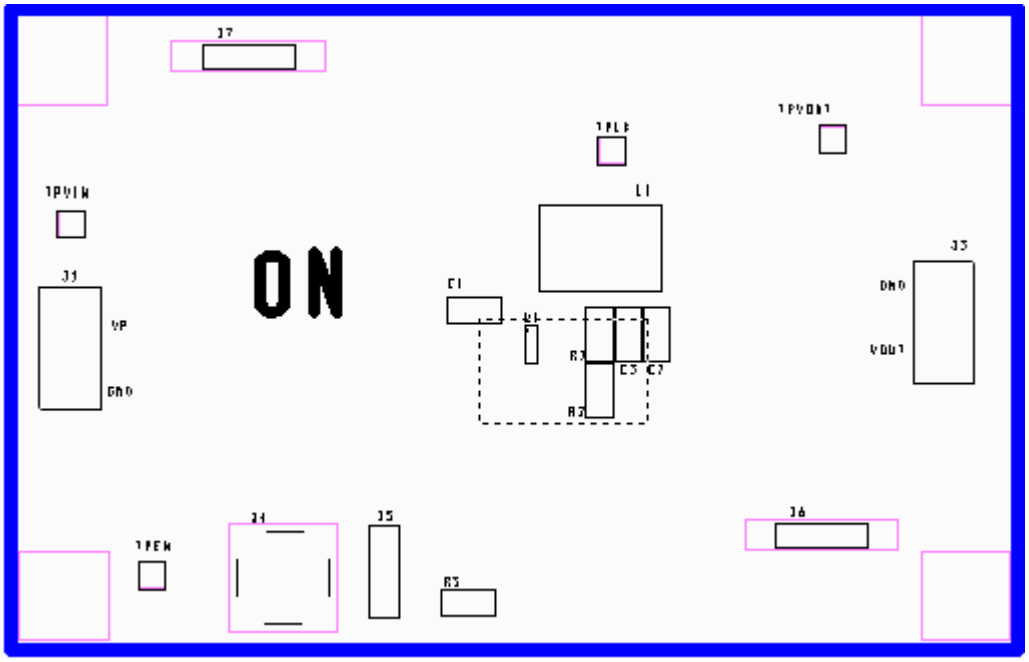


Figure 30. Silkscreen Layer

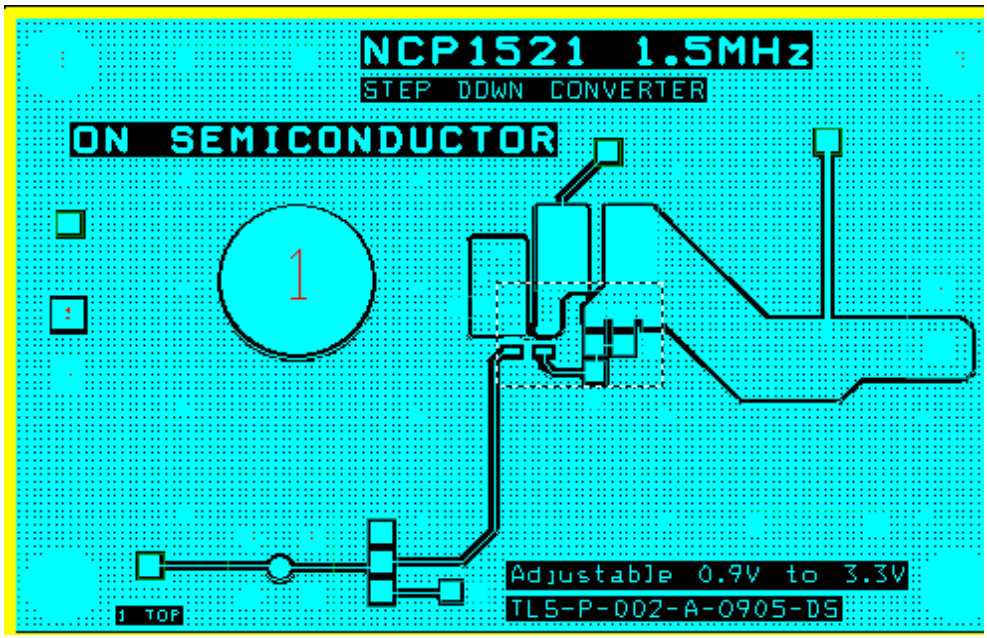


Figure 31. Board Layout (Top View)

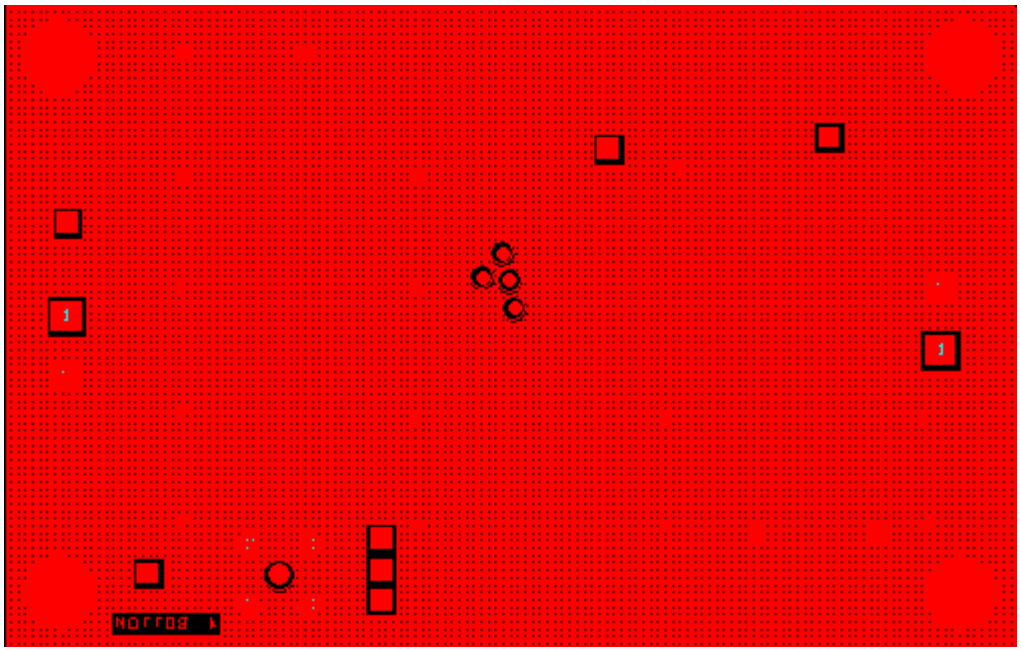


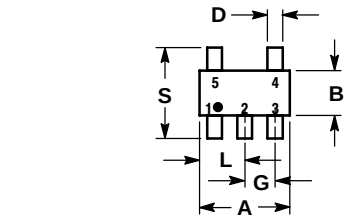
Figure 32. Board Layout (Bottom View)

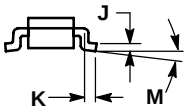
Bill of Materials

Item	Part Description	Ref	PCB Footprint	Manufacturer	Manufacturer Reference
1	NCP1521 DC−DC Converter	U1	TSOP−5	On Semiconductor	NCP1521
2	4.7 μF Ceramic Capacitor 6.3 V X5R	C1	0805	Murata	GRM21 Series
3	10 μF Ceramic Capacitor 6.3 V X5R	C2	0805	Murata	GRM21 Series
4	SMD Resistor 220 K	R1, R2, R3	0805	Vishay−Draloric	CRCW0805
5	SMD Inductor	L1	1605	Coilcraft	DO1605 Series
6	I/O Connector can be plugged by BLZ5.08/2 (Weidmüller reference)	J1, J3	−	Weidmüller	SL5.08/2/90B
7	Jumper Header vertical mount 3*1, 2.54 mm	J5	−	Tyco Electronics/AMP	5−826629−0
8	Jumper Connector, 400 mils	J6, J7	−	Harwin	D3082−B01

PACKAGE DIMENSIONS

TSOP−5
SN SUFFIX
CASE 483−02
ISSUE E

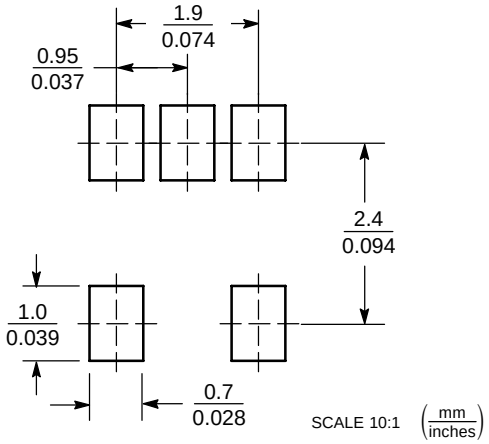




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. A AND B DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181

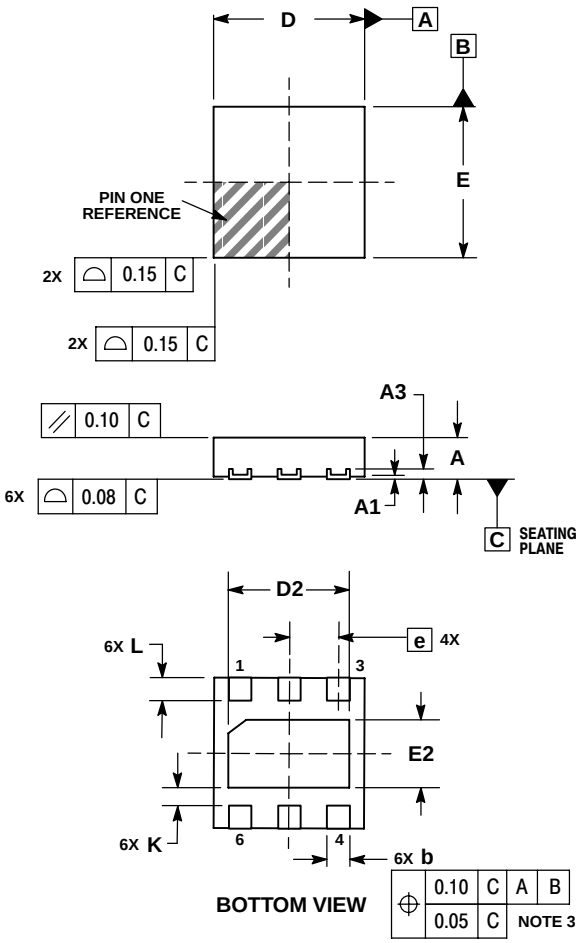
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

UDFN6, 2x2, 0.65P
MU SUFFIX
CASE 517AB−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.25	0.35
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.65 BSC	
K	0.20	---
L	0.25	0.35

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