DIGITAL TUNING SYSTEM

DESCRIPTION

The SC9318-033 is a single-chip digital tuning system optimum for portable sets such as headphone radio, etc... 5-band of FM/MW/LW/TV/SW are provided compatibly with worldwide destinations.

FEATURE

Tuning function:

- Manual tuning (up/down)
- Direct tuning
- · Seek tuning

Memory function:

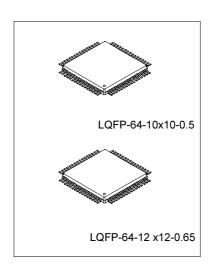
• FM/MW/LW or TV/SW/WB each band 10 stations

Clock function:

- Dual clock function
- 12/24H clock
- Sleep timer function
- Alarm timer function

Other function:

Battery check input

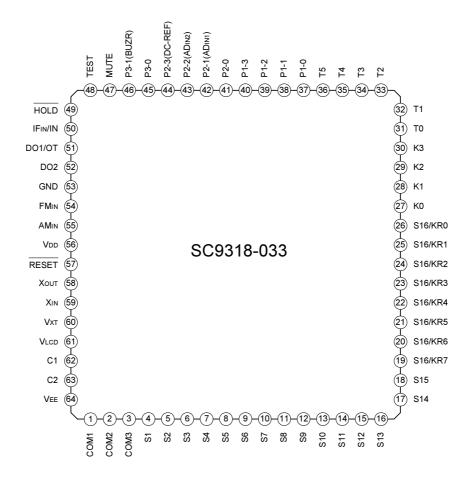


ORDERING INFORMATION

Device	Package
SC9318FA	LQFP-64-10x10-0.5
SC9318FB	LQFP-64-12x12-0.65



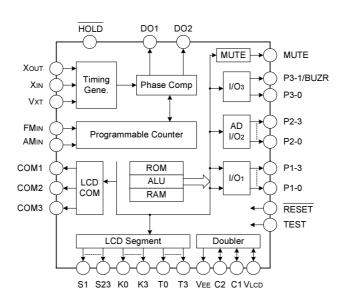
PIN CONFIGURATION



----- HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD ----



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Characteristic	Symbol	Value	Unit
Supply Voltage	VDD	1.3	V
Input Voltage	VIN	-0.3~ VDD+0.3	٧
Power Dissipation	PD	100	mW
Operating Temperature	Topr	-10~60	°C
Storage Temperature	Tstg	-55~125	°C

ELECTRICAL CHARACTERISTICS (Tamb=25°C, VDD =3.0V, unless otherwise specified)

Characteristic	Symbol	Test Condition	MIN	TYP	MAX	Unit
Range of Operating	VDD	*	1.8	3.0	3.6	V
Supply Voltage	VDD		1.0	3.0	3.0	V
Range of Memory	VHD	* Crystal oscillation stopped (CKSTP	1.0		3.6	mA
Retention Voltage	VHD	instruction executed)	1.0		3.0	IIIA

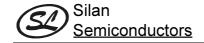
(To be continued)

----- HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD -----



Characteristic	Symbol	Test Condition	MIN	TYP	MAX	Unit
	loo.	Under ordinary operation and PLL on operation, on output VDD=3V load FMIN=230MHz input		7.0	12	
On another Comment	IDD1	Under ordinary operation and PLL on operation, no output load FMIN=130MHz input		6.0	10	
Operating Current	IDD2	Under CPU operation only (PLL off, display turned on)		40	80	
	IDD3	Soft wait mode (crystal oscillator, display circuit operating, CPU stopped, PLL off)		25	50	μА
	IDD4	Hard wait mode (crystal oscillator operating only)		15	30	
Memory Retention Current	IHD	Crystal oscillation stopped (CKSTP instruction executed)		0.1	10	
Crystal Oscillation Frequency	fxT	*		75		kHz
Crystal Oscillation Startup Time	tsT	Crystal oscillation fXT=75kHz			1.0	s
Voltage Doubler Circu	it					
Voltage Doubler Reference Voltage	VEE	GND reference (VEE)	1.3	1.5	1.7	V
Constant Voltage Temperature Characteristics	DV	GND reference (VEE)		-5		mV/°
Voltage Doubler Boosting Voltage	VLCD	GND reference (VLCD)	2.6	3.0	3.4	V
Operating frequency ra	Operating frequency ranges for programmable counter and IF counter					
FMIN (VHF Mode)	fVHF	Sine wave input when VIN =0.2Vp-p	50	~	230	
FMIN (FM Mode)	fFM	Sine wave input when VIN =0.2Vp-p	40	~	130	
AMIN (HF Mode)	fHL	Sine wave input when VIN =0.2Vp-p	1	~	45	MHz
AMIN (LF Mode)	fLF	Sine wave input when VIN =0.2Vp-p	0.5	~	12	
IFIN	fIF	Sine wave input when VIN =0.2Vp-p	0.35	~	12	
Input Amplitude	VIN	FMIN, AMIN, IFIN input	0.2	~	VDD -0.8	Vp-p

(To be continued)



(Continued)

Chara	cteristic	Symbol	Test Condition	MIN	TYP	MAX	Unit
LCD com	mon output/s	segment outp	out (COM1~COM3, S1~S23)				
Output	"H" Level	IOH1	VLCD =3V, VOH=2.7V	-0.5	-1.0		mA
Current	"L" Level	IOL1	VLCD =3V, VOH =0.3V	0.5	1.0		IIIA
Output Vo	oltage 1/2	VBS	No load	1.3	1.5	1.7	V
Level		VBS	No load	1.3	1.0	1.7	V
HOLD in	put port						
In put Lea	ak Current	ILI	VIH=3.0V, VIL=0V			±1.0	μА
Input	"H" Level	VIH1		2.4	~	3.0	V
Voltage	"L" Level	VIL1		0	~	1.2	V
A/D (N) c	onverter (A/E	DIN2, DC-RE	F)				
Analog In Voltage F	•	VAD	ADIN1, ADIN2	0	~	VDD	V
Analog R Voltage F		VREF	DC-REF, VDD =2.0~3.6V	1.0	~	VDD ×0.9	٧
Resolutio	n	VRES			6.0		bit
Conversion Error	on Total		VDD =2.0~3.6V		±1.0	±4.0	LSB
Analog In	Analog Input Leak		VIH=3.0V, VIL=0V (ADIN1, ADIN2, DC-REF)			±1.0	μА
KEY inpu	t port (K0~K3	3)		•	•		
N-ch/P-ch Resistand	•	RIN1		75	150	300	kΩ
Input	"H" Level	VIH2	When input with pull-down resistance	1.8	~	3.0	V
Voltage	"L" Level	VIL2	When input with pull-down resistance	0	~	0.3	V
Input	"H" Level	VIH3	When input with pull-up resistance	2.7	~	3.0	V
Voltage	"L" Level	VIL3	When input with pull-up resistance	0	~	1.2	V
Input Leak Current		lLi	When input resistance off, VIH=3.0V, VIL=0V			±1.0	μА
Timing ou	Timing output port (T0~T5)						
Output	"H" Level	Іон1	VOH =2.7V	-0.5	-1.0		m ^
Current	"L" Level	IOL1	VOL=0.3V,Use LCD key-return mode	0.5	1.0		mA
N-ch Loa Resistano	-	İTL	No used LCD key-return mode	75	150	300	kΩ

(To be continued)

—— HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD ——



$(C_0$			1/
11 .0	mille	II IEC	11

Chara	cteristic	Symbol	Test Condition	MIN	TYP	MAX	Unit
DO1/OT,	DO2 output;	MUTE outpu	ıt				
Output	"H" Level	IOH1	VOH =2.7V	-0.5	-1.0		
Current	"L" Level	IOL1	VOL =0.3V	0.5	1.0		mA
Output O	ff Leak	_	VTLH=3.0V, VTLL=0V			. 400	
Current		ITL	(DO1, DO2)			±100	nA
General-p	ourpose I/O p	orts (P1-0~F	23-1)				
Output	"H" Level	IOH1	VOH =2.7V	-0.5	-1.0		A
Current	"L" Level	IOL1	VOL =0.3V	0.5	1.0		mA
Input Le	ak Current	ILI	VIH=3.0V, VIL=0V			±1.0	μА
Input	"H" Level	VIH4		2.4	~	3.0	V
Voltage	"L" Level	VIL4		0	~	0.6	V
IN, RESE	 T input port						
Input Le	ak Current	ILI	VIH=3.0V, VIL=0V			±1.0	μА
Input	"H" Level	VIH4		2.4	~	3.0	V
Voltage	"L" Level	VIL4		0	~	0.6	V
Others							
Input Pull Resistand		RIN2	(TEST)	25	50	100	kΩ
XIN Amp Resistand	Feedback ce	RfXT	(XIN-XOUT)		20		ΜΩ
Xout Out	•	Rout	(Хоит)		3		kΩ
Input Am	p Feedback	RfIN1	(FMIN, AMIN)	150	300	600	
Resistand	Resistance		(IFIN)	500	1000	2000	kΩ
Voltage L	Jsed to	RfIN2	· ·				
Detect Supply		VSTP	VDD	1.3	1.5	1.6	V
Voltage Drop							
Supply Voltage Drop							
Detection	l	DS	VDD		-2		mV/°C
Temperat		טט	V V D D				IIIV/ C
Characte	ristics						

----- HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD -----



PIN DESCRIPTION

Pin No.	Symbol	Pin Name	Internal Connection	Description
1	COM1		₽ VLCD	Output common signal to the LCD panel. Through a matrix with pins S1~S23, a maximum of 69 segments can be displayed.
2	COM2	LCD common output	VEE -	Three levels, VLCD, VEE, and GND, are output at 83Hz every 2ms. VEE is output after
3	СОМЗ		÷	SYSTEM RESET and CLOCK STOP are released, and a common signal is output after the DISP OFF bit is set to "0".
4~18	S1~S15	LCD segment output	Z VI.CD	Segment signal output pins for the LCD panel. Together with COM1, COM2, and COM3, a matrix is formed that can display a maximum of 69 segments. The signals for the key matrix
19~26	S16/KR7 ~	LCD segment output/Key	S16/KR7~S23/KR0 are output	and the segment signals from pins S16/KR7~S23/KR0 are output on a time division basis. 4 X 8=32 key matrix can be
	S23/KR0	return timing output		created in conjunction with key input ports K0~K3.
27~30	K0~K3	Key input ports	A THE THE PART OF	4 bit input ports for key matrix input. Combined in a matrix with key return timing outputs the LCD segment pins, data from a maximum of 4X8=32 keys can be input and pins are pulled up. On the key setting output pin, data from 4X6=24 keys can be input and pins are pulled down. The WAIT mode is released when high level is applied to key input ports set to pull-down.
31~36	T0~T5	Key return timing output port	Row July	These ports output the timing signal for key matrix. To form the key matrix, load resistance has been built-in the N-channel side. When the key matrix combined with push-key that does not need a key matrix diode.

(To be continued)



(Co	ntini	ued)
100		ucu,

Pin No.	Symbol	Pin Name	Internal Connection	Description
37~40	P1-0 ~ P1-3	I/O port 1		The input and output of these 4 bit I/O ports can be programmed in 1 bit units. By altering the input to I/O ports set to input, the CLOCK STOP and WAIT modes can be released, and the MUTE bit of the MUTE pin can be set to "1".
41~44	P2-0 P2-1/ ADIN1 P2-2/ ADIN2 P2-3/ DC-REF	I/O port 2 /AD analog voltage input /AD analog voltage input /Reference voltage input	To A/D converter (P2-0 pin is excluded)	4 bit I/O ports. Input and output may be programmed in 1 bit units. Pins P2-1 through P2-2 can also be used for analog input to the built-in 6 bit, 2-channel A/D converter. Conversion time of the built-in A/D converter using the successive comparison method is 280μs. The necessary pin can be programmed to A/D analog input in 1 bit units, and P2-3 can be set to the reference voltage input. Internal power supply (VDD) or constant voltage (VEE) can be used as the reference voltage. In addition, constant voltage (VEE) can be input to the A/D analog input so battery voltage, etc., can be easily detected. The reference voltage input, for which a built-in operational amp is used, has high impedance. The A/D converter, and their control are all executed by program.
45~46	P3-0 P3-1/ BUZR	I/O port 3 /Buzzer output		2 bit I/O ports, whose input/output can be programmed in 1 bit units. The P3-1 pin also functions as the output for the built-in buzzer circuit. The buzzer sound can be output in 254 different tones between 18.75kHz and 147Hz, and at a duty of 50%. The buzzer output, and all associated controls can be programmed.

(To be continued)



Pin No.	Symbol	Pin Name	Internal Connection	Description
47	MUTE	Muting output port		1 bit output port. Normally, this port is used for muting control signal output. This pin can set the internal MUTE bit to "1" according to a change in the input of I/O port 1. MUTE bit output logic can be changed; PLL phase difference can also be output using this pin.
49	HOLD	HOLD mode control input		Input pin for request/release HOLD mode. Normally, this pin is used to input radio mode selection signals or battery detection signals. HOLD mode includes CLOCK STOP mode (stops crystal oscillation) and WAIT mode (halts CPU). Setting is implemented with the CKSTP instruction or the WAIT instruction. When the CKSTP instruction is executed, request/release of the HOLD mode depends on the internal MODE bit. If the MODE bit is "0" (MODE-0), executing the CKSTP instruction while the HOLD pin is at low level stops the clock generator and the CPU and changes to memory back-up mode. If the MODE bit is "1" (MODE-1), executing the CKSTP instruction enters memory back-up mode regardless of the level of the HOLD pin. Memory back-up is release when the HOLD pin goes high in MODE-0, or when the level of the HOLD pin low in MODE-1. When memory back-up mode is entered by executing a WAIT instruction, any change in the HOLD pin input releases the mode. In memory back-up mode, current consumption is low (below 10µA), and all the output pins (e.g., display output, output ports) are automatically set to low level.

(To be continued)



(Co	ntini	ued)
100		ucu,

Pin No.	Symbol	Pin Name	Internal Connection	Description
48	TEST	TEST mode control input	RINZ	Input pin used for controlling TEST mode. High level indicates TEST mode, while low level indicates normal operation. The pin is normally used at low level or no-connection (NC). (A pull-down resistor is built-in).
50	IF _{IN} /IN	IF signal input/Input port	Rrinn2	IF counter's IF signal input for counting the IF signals of the FM and AM bands and detecting the automatic stop position. The input frequency is between 0.35~12MHz (0.2VP-P(Min)). A built-in input amp and C coupling allow operation at low-level input. The IF counter is a 20 bit counter with optional gate times of 1, 4, 16, and 64ms. 20 bit of data can be readily stored in memory. This input pin can be programmed for use as an input port (IN port). CMOS input is used when the pin is set as an IN port.
51	DO1/OT	Phase comparison output /Output port	<u></u>	PLL's phase comparison tri-state output pins. When the programmable counter's prescaler output is higher than the reference frequency, output is at high level. When output is lower than the reference frequency, high impedance output is obtained.
52	DO2	Phase comparison output	- L	Because DO1 and DO2 are output in parallel, optimal filter constants can be designed for the FM/VHF and AM bands. Pin DO1 can be programmed to high impedance or programmed as an output port (OT). Thus the pins can be used to improve lock-up time or used as output ports.

(To be continued)



Pin No.	Symbol	Pin Name	Internal Connection	Description
56	VDD	Power-supply	VDD O—	Pins to which power is applied. Normally, VDD=1.8~3.6V (3.0V Typ.) is applied. In back-up mode (when CKSTP instructions are being executed), voltage can be lowered to 1.0V. If voltage falls below 1.5V while the CPU is operating, the CPU stops to prevent malfunction (STOP mode). When the voltage rises above 1.5V, the CPU restarts. STOP mode can be detected by checking the STOP F/F bit. If necessary, execute initialization or adjust clock by program.
53	GND	pins	○ - GND	When detecting or preventing CPU malfunctions using an external circuit, STOP mode can be invalidated and rendered non-operative by program. In that case, all four bits of the internal TEST port should be set to "1". If more than 1.8V is applied when the pin voltage is 0, the device's system is reset and the program starts from address "0". (power on reset).(Note) To operate the power on reset, the power supply should start up in 10~100ms.
54	FMIN	FM programmabl e counter input	RfIN2 RfIN2	Programmable counter input pin for FM,VHF band. The 1/2+pulse swallow system (VHF mode) and the pulse swallow system (FM mode) are selectable freely by program. At the VHF mode, local oscillation output (VCO output) of 50~230MHz (0.2VP-P(Min)) is input and FM mode, 40~130MHz (0.2VP-P (Min)) is input. A built-in input amp and C coupling allow operation at low-level input. (Note) when in the PLL OFF mode or when set to AMIN input, the input is pulled down.

(To be continued)

----- HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD -----



Pin No.	Symbol	Pin Name	Internal Connection	Description
55	AMIN	AM local oscillator signal input	Rfin2	Programmable counter input pin for AM band. The pulse swallow system (HF mode) and direct dividing system (LF mode) are freely selectable by program. At the HF mode, local oscillation output (VCO output) of 1~45MHz (0.2VP-P(Min)) is input and LF mode, 0.5~12MHz (0.2VP-P(Min)) is input. Built-in input amp operates with low-level input using a C coupling. (Note) When in PLL OFF mode or when set to FMIN input, the input is pulled down.
57	RESET	Reset input		Input pin for system reset signals. RESET takes place while at low level; at high level, the program starts from address"0". Normally, if more than 1.8V is supplied to VDD when the voltage is 0, the system is reset (Power on reset). Accordingly, this pin should be set to high level during operation.
58	XOUT		Xout O Rout	Crystal oscillator pins.
59	XIN		RfXT	A reference 75kHz crystal oscillator is
60	VXT	Crystal oscillator pins	XINO	connected to the XIN and XOUT pins. The oscillator stops oscillating during CKSTP instruction execution. The VXT pin is the power supply for the crystal oscillator. A stabilizing capacitor (0.47 μ F Typ.) is connected.

(To be continued)



Pin No.	Symbol	Pin Name	Internal Connection	Description
61	VLCD			Voltage doubler boosting pin for driving the LCD. A capacitor (0.1µF Typ.) is connected to boost the voltage. The VLCD pin outputs voltage (3.0V), which has
62	C1	Voltage double boosting pin	VLCD	been doubled from the constant voltage (VEE: 1.5V) using the capacitors connected between C1 and C2. That potential is supplied to the LCD drivers. If the internal VLCD OFF bit is set to "1" by program, an external power supply
63	C2			can be input through the VLCD pin to drive the LCD. At this time, the VLCD/2 potential, whose VLCD voltage is divided using registers, is output from the C2 pin.
64	VEE	Constant voltage supply pin		1.5V constant voltage supply pin for driving the LCD. A stabilizing capacitor $(0.1\mu F\ Typ.)$ is connected. This is a reference voltage for the A/D converter, key input, and the LCD common output's bias potential.

Note: 1. When the device is reset (voltage higher than 1.8V, or when RESET =low→high), I/O ports are set to input, the pins for I/O ports and additional functions (e.g., A/D converter) are set to I/O port input pins, while the IFIN/IN pins become IF input pins.

- 2. When in PLL OFF mode (when the three bits in the internal reference ports all show "1"), the IFIN and FMIN, AMIN pins are pulled down, and DO1 And DO2 are at high impedance.
- 3. When in CLOCK STOP mode (during execution of CKSTP instruction), the output port and the LCD output pins are all at low level, while the constant voltage circuit (VEE), the voltage doubler circuit (VLCD), and the power supply for the crystal oscillator (VXT) are all off.
- 4. When the device is being reset, the contents of the output ports and internal ports are undefined and initialization by program is necessary.

----- HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD -----



FUNCTIONAL DESCRIPTION

RECEIVING BAND

		Co	de		Step	Fref.	
Area	Band	A1	A0	Receiving range	(Hz)	(Hz)	IF(Hz)
	FM			87.5~108.0M	50/200k	25k	10.7M
	B 43.07			522~1620k	9k	3k	4501-
U.S.A. *1	MW	0	0	520~1710k	10k	5k	450k
"1	TV			2~13ch	1ch	25k	40.714
	WB			162.400~162.550M	25k	12.5k	10.7M
	FM			87.5~108.0M	50/100k	25k	10.7M
				522~1620k	9k	3k	
General	MW	0	1	520~1620k	10k	5k	450k
	LW			144~281k	1k	1k	
	- FN4			65.0~74.0M	50k	25k	10.7M
Europe	FM			87.5~108.0M	50k	25k	10.7M
east/Europe	B 43 A /	1	0	531~1611k	9k	3k	
*2	MW			530~1610k	10k	5k	450k
	LW			144~281k	1k	1k	
				76.0~108.0M	100k	25k	-10.7M
	FM			76.0~90.0M	100k	25k	-10.7M
Japan		4	1	76.0~3ch	100k	25k	-10.7M
*3	B 43 A /	1	1	522~1629k	9k	3k	4501-
	MW			520~1620k	10k	5k	450k
	TV			1~12ch	1ch	25k	-10.7M
		SW1	SW0				
	CW	0	1	5.95~15.6	- FI.	El.	4501
	SW	0	1	3.8~12.5	5k	5k	450k

Note: *1. If step is 200kHz. Range is 87.5~108.1MHZ

---- HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD ----

^{*2.} The frequency range of FM in Europe area is according to FM step jumper.

^{*3.} The frequency range of FM in Japan area is according to FM step and LW/TV enable jumper.



KEY MATRIX

	K0	K1	K2	K3
то	A0 *	A1 *	SW0 *	SW1 *
T1	LW/TV * Enable	WB* Enable	FM step *	MW step *
T2	IF count * Enable	1/8 IF *	POWER KEY *enable	BAND * OUT
Т3	CLOCK * disable	DUAL * disable	CLOCK * 12/24 H	+5KEY * enable
T 4	BAND/DUAL	MEMORY/ CK ADJ	UP/ HOUR	DOWN/ MIN
Т5	Minc	Mdec	ALARM	SLEEP

(*: Diode jumper)

KEY MATRIX (AD in1 and AD in2)

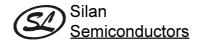
AD1	AD2
1	7
2	8
3	9
4	0
5	FM
6/+5	AM

KEY MATRIX EXPLANATION OF FUNCTION

Symbol	Explanation of function
0~9	Calling and writing preset memory.
+5	Indirect tuning mode, used for input frequency
AM	Indirect tuning mode. Changing direct tuning mode of each band.
FM	When the key pushing again, mode is released.
BAND/DUAL	The receiving band is changed.
	In clock mode, the two clocks is changed cyclically

(To be continued)





(Ooritinada)	
Symbol	Explanation of function
MEMORY/	The writing preset memory in frequency display.
CK ADJ	The clock adjustment in clock display.
UP/ HOUR	The receiving frequency is up.
	The hour of time is up in clock adjustment mode.
DOWN/	The receiving frequency is down.
MIN	The minute of time is up in clock adjustment mode.
Minc	In calling and writing preset memory, select of channel.
Mdec	
ALARM	The alarm function is on/off
SLEEP	The sleep function is on/off

DIODE MATRIX

EXPLANATION OF FUNCTION

Symbol	Explanation of function				
	Setting area				
	A1	A0	ARAE		
A0	0	0	U.S.A		
A1	0	1	General		
i	1	0	Europe/ E-Europe		
	1	1	Japan		
	Setting of the	receiving b	and of SW		
	SW1	SW0	Receiving band (MHz)	Note	
SW0	0	0	No SW		
SW1	0	1	5.95~15.6	SWA	
	1	0	3.80~12.50	SWB	
	Setting of LW	//TV band			
LW/TV	The with diode: TV enable (Japan, U.S.A)				
Enable	The with diode: LW enable (other)				
Lilabie	The withou	t diode: TV d	isable (Japan, U.S.A)		
	The withou	t diode: LW	disable (other)		

(To be continued)





10-		ned)
11 .0	miller	116(11

Symbol	Explanation of function					
WB enable	Setting of WB band The with diode: WB enable The without diode: WB disable					
	Setting of FM step					
	FM step	Step	FM receiving frequence	су		
	0	200kHz	87.5~108.0M			
	1	50kHz	87.5~108.0M			
	General area					
	FM step	Step	FM receiving frequence	су		
	0	100kHz	87.5~108.0M			
	1	50kHz	87.5~108.0M			
	Europe area					
	FM step	Step	FM receiving frequence	су		
FM STEP	0	50kHz	65.0~74.0M 87.5~108.0M			
	1	50kHz	87.5~108.0M			
	Japan area (ste					
	FM step LW/TVena		FM receiving	TV receiving		
	T iii Stop	20071 Vena	frequency	frequency		
	0	0	76.0~108.0M			
	0	1	76.0~108.0M	1~12ch		
	1	0	76.0~3ch			
	1	1	76.0~90.0M	1~12ch		
	Setting of MW s	ten				
MW STEP		•)			
	The with diode: MW 10kHz step The without diode: MW 9kHz step					
	Setting of the IF count detection					
IF count		: IF count detect				
Enable	The without di	ode: SD input det	tection			
	Setting of IF cou	ınter input				
1/8 IF	The with diode	e: IF 1/8 input				
	The without di	ode: IF direct inp	ut			

(To be continued)

—— HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD ——



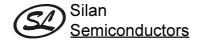
Symbol	Explanation of function			
POWER	Setting of power key			
KEY	The with diode: tact key			
enable	The without diode: slide key			
	Setting of BAND IN/OUT			
BAND OUT	The with diode: BAND OUT			
	The without diode: BAND IN			
CLOCK disable	Setting of clock function The with diode: clock disable The without diode: clock enable			
Dual disable	Setting of dual clock function The with diode: dual clock disable The without diode: dual clock enable			
CLOCK 12/24H	Setting of clock function The with diode: 24H CLOCK The without diode: 12 CLOCK			
+5 KEY enable	Setting of +5 key The with diode: +5 key enable The without diode: +5 key disable			

I/O MAP

Port	Pin	Name	I/O	Function	Active	Init	Case of Not use
DO1/OT	51	POOWER out	0	Power output	Н	L	Open
IN	50	IF IN/SDIN	1	IF count input/SD input			
HOLD	48	BATTERY	I	I Battery input L: back up, H: normal		-	GND
MUTE	47	MUTE	0	O MUTE output		Н	Open
P3-1	46	BUZR	0	O BUZR output			Open
P3-0	45	BATTERY INDICATOR	I	Battery indicator input L: battery mark flashing H: no mark	н		VDD
P2-3	44	STEREO	1	Stero input L: mono H: stereo	Н	-	GND
P2-2	43	ADIN2	I	Key AD input			VDD

(To be continued)

—— HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD ——



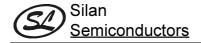
(Continued)

Port	Pin	Name	I/O	Function	Active	Init	Case of Not use
P2-1	42	ADIN1	I	Key AD input		-	VDD
P2-0	41	B2/TVout	0	Refer to another sheet.			
P1-3	40	BAND1	I/O			-	
P1-2	39	BAND0	I/O			-	
P1-1	38	LOCK	1	Key lock input L: unclock H: lock	Н	ŀ	GND
P1-0	37	POWER in	I	Power input/ power key		-	
T5	36	T5	0	Key timing output	Н	L	Open
T4	35	T4	0	Key timing output	Н	L	Open
T3	34	Т3	0	Key timing output	Н	L	Open
T2	33	T2	0	Key timing output	Н	L	Open
T1	32	T1	0	Key timing output	Н	L	Open
T0	31	ТО	0	Key timing output	Н	L	Open

LCD MAP

			Segment name)	
Symbol	Pin no.	COM1	COM2	COM3	Function
S1	4	FM	MW	ALARM	FM: FM band MW: MW band ALARM: alarm mark
S2 S3	5 6	1 2	SW TV	LW PM	SW, 1, 2: SW band TV: TV band PM: PM (clock)
S4 S5	7 8	1a' 1c	AM 1b	SLEEP Colon	AM: AM (clock) SLEEP: sleep mark 1a, 1c, 1b: 21.885 colon: (clock)
S6 S7 S8	9 10 11	2e 2c SWdot	2f 2g 2c	ST 2a 2b	2a-g: 21.885 ST: stereo mark SWdot: 21_855

(To be continued)



(Continued)

0			Segment name		
Symbol	Pin no.	COM1	COM2	COM3	Function
S9	12	3e	3f	LOCK	3a-g: 10 <u>7</u> .95
S10	13	3d	3g	3a	LOCK: key lock mark
S11	14	FMdot	3c	3b	FMdot: 107_95
S12	15	4e	4f	BATT	4a-g: 107. <u>9</u> 5
S13	16	4d	4 g	4a	BATT: no battery mark
S14	17	5	4c	4b	5: 107.9 <u>5</u>
S15	18	KHz	MHz	МЕМО	KHz: kHz mark MHz: MHz mark MEMO: memory mark
S16	19	7e	7f	6bc	6bc: 107.95 <u>1</u> 5
S17	20	7d	7g	7a	CH: CH mark
S18	21	СН	7c	7b	7a-g: 107.95 1 <u>5</u>
S19	22	wb	+5		Wb: WB band & <u>16</u> 2.xx +5 :+5 mark





When BAND OUT is selected

OUT OUT OUT B0 В1 B2 FM SW Н Н L MW Н LW Н WB Н Н 2-6ch L L TV USA 7-13ch L L Н 1-3ch TV JPN 4-12ch Н

When BAND IN is selected With LW/TV enable diode jumper

USA/JPN		IN	IN	OUT
		В0	B1	TVout
FM		L	L	L
MW		Н	L	L
WB		L	Η	Η
TV USA	2-6ch	Н	Η	L
	7-13ch	Н	Η	Н
F	1-3ch	Н	Η	L
TV JPN	4-12ch	Н	Н	Н

When TV is enable, SW can not be selected.

Without LW/TV enable diode jumper

	IN	IN	OUT
	В0	B1	TVout
FM	L	L	L
SW	Н	Η	L
MW	Н	Ш	L
WB	L	Η	Н

EUR/GEN	IN	IN	OUT
	В0	B1	TVout
FM	L	L	L
SW	Н	Н	L
MW	Н	L	L
WB	L	Н	L

When LW is enable, WB can not be selected.

BAND CHANGE

1.Principal function

The receiving band is changed

2. input ports and keys to be used

BAND key, BAND0 in/out, BAND1 in/out, BAND2/TV output, BAND OUT jumper.

3.Function

With BAND OUT jumper

- a. The receiving band is changed cyclically pushing [BAND] key.
- b. The receiving band is changed as shown below.

----- HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD -----

2 band selection (SW0, SW1, LW/TVenable jumper,WBenable jumper = 0)

3 band selection (LW/TVenable jumper, WBenable jumper = 0)

$$\rightarrow$$
 FM \longrightarrow MW \longrightarrow SW-A/B

3 band selection (SW0,SW1, WBenable jumper = 0)

$$\rightarrow$$
 FM \longrightarrow MW \longrightarrow LW/TV \longrightarrow

4 band selection (WBenable jumper = 0)

$$\rightarrow$$
 FM \longrightarrow MW \longrightarrow LW/TV \longrightarrow SW-A/B

In case of USA case

$$\rightarrow$$
 FM \longrightarrow MW \longrightarrow (TV) \longrightarrow (SW-A/B) \longrightarrow (WB)

c. In case of +5 KEYenable jumper is off, when the AM key and 0~9 key is used, frequency is setting direct.

But the frequency is outside, the "err" mark is flashed.

Without BAND OUT jumper:

- a. The receiving band is changed by BAND0 and BAND1 input.
- b. The receiving band is changed as shown below

With LW/TV enable jumper

	IN	IN	OUT
	В0	B1	TVout
	L	L	L
	Н	L	L
	L	Η	Н
2-6ch	Η	Η	L
7-13ch	Н	Н	Н
1-3ch	Н	Н	L
4-12ch	Н	Н	Н
	7-13ch 1-3ch	B0 L H L 2-6ch H 7-13ch H	B0 B1 L L H L L H 2-6ch H H 7-13ch H H

EUR/GEN	IN	IN	OUT
	В0	B1	TVout
FM	L	L	L
SW	Н	Н	L
MW	Η	L	L
WB	L	Н	L

When LW is enable, WB can not be selected.

When TV is enable, SW cannot be selected.

WB is selected at USA area

----- HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD -----



Without LW/TV enable jumper

	IN	IN	OUT
	В0	B1	TVout
FM	L	L	L
SW	Н	Н	L
MW	Н	Ш	L
WB	L	Н	Н

WB is selected at USA area

MANUAL TUNING/SEEK TUNING

1. Principal function

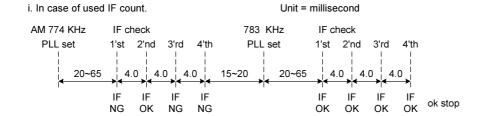
1 push/ 1 step and seek tuning.

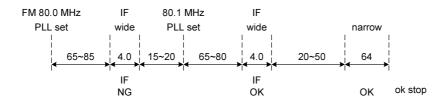
2. Input ports and keys be used.

UP key, DOWN key

- 3. Function
 - a. 1 push/ 1 step tuning by UP/DOWN key.
 - b. When UP/DOWN key is pushed for more than 500ms, seek tuning is started.
 - c. The seek tuning is stopped. If IFcount-enable jumper is "ON", the stop signal specified is input on IF INPUT, else IFcount-enable jumper is "OFF", the stop signal specified is input on SD INPUT.
 - d. But seek tuning is not stopped even when a station was detected, in case UP/DOWN key is pushing continue.
 - e. The scan time is 200ms/ step in TV/WB band. In other bands, it is 100ms/step.
 - f. The tuning method is the saw tooth wave form method, and when the receiving frequency rearch the band edge, if goes to the opposite side and the continuous tuning is hold for 500ms. In case of meter band, refer explanation of the meter band.
 - g. When the LW band received, manual tuning is 1kHz/step, but seek tuning is 9kHz/step.
 - h. In case of used SD signal.







	Wide			Narrow			
Band	Range (Hz)	Gate time (ms)	Times	Range (Hz)	Gate time (ms)	Times	
FM	10.7M ± 80k	4	1/1	10.7M ± 20k	64	1/1	
TV/WB	10.7M ± 80k	4	1/1	10.7M \pm 30k	64	1/1	
LW/MW/SW	450 ± 0.5k	4	2/4				

PRESET MEMORY

1. Principal function

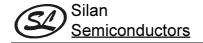
Calling and writing in preset memory.

2. Input ports and keys to be used.

0~9 keys, Minc key, Mdec key, MEMORY key, AM key, FM key, +5 KEYenable jumper.

- 3. Function
 - a. The each band have the fixed preset memory 10ch.
 - b. The fixed preset memory is called when 0~9 was pushed.
 Incase of +5 KEYenable jumper is set, the +5 key at first pushing is only flashing "+5" mark. A preset memory number is fixed when 1~5 key was pushed during "+5" mark is flashed. If second pushing is nothing for 5 second, it canceled "+5" mark flashing mode.

—— HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD ——



- When the Minc key is pushed, the preset memory called next ch.
 When the Mdec key is pushed, the preset memory is decrement.
- d. In case of +5KEYenable jumper is off, when the AM or FM key is used. Frequency is setting direct. AM or FM key push, changed the direct input mode, and frequency is setting by pushed 0~9 key. If input frequency is inside. The frequency is received, but the frequency is outside, the "Err" mark is flashed, and canceled this mode.
- e. The memory mode is set, when MEMORY key was pushed.
- f. The memory mode is released automatically after 5 seconds.
- g. The "MEMO" mark is flashed in the memory mode.
- h. A receiving frequency is written in the fixed preset memory, when MEMORY key is pushed after 0~9 key was pushed in the memory mode.

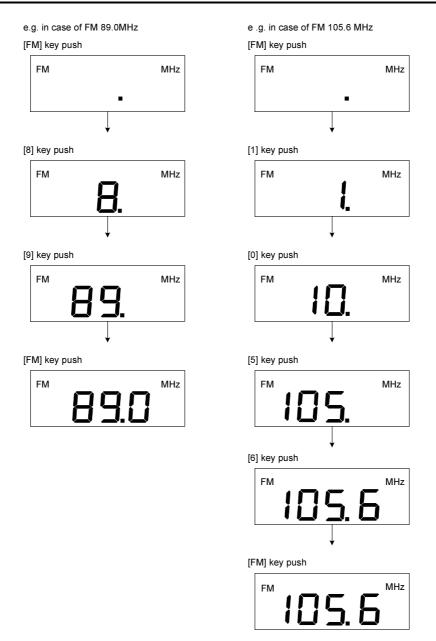
In case of Minc or Mdec key is used. It is selected the each ch in the memory mode, and you pushed MEMORY key again.

DIRECT TUNING

- 1. Principal function
 - Direct tuning
- 2. Input ports and keys be used.
 - FM, AM, 0~9 key, +5 KEYenable jumper
- 3. Function
 - a. In case of +5 KEYenable jumper is off, this function is enable.

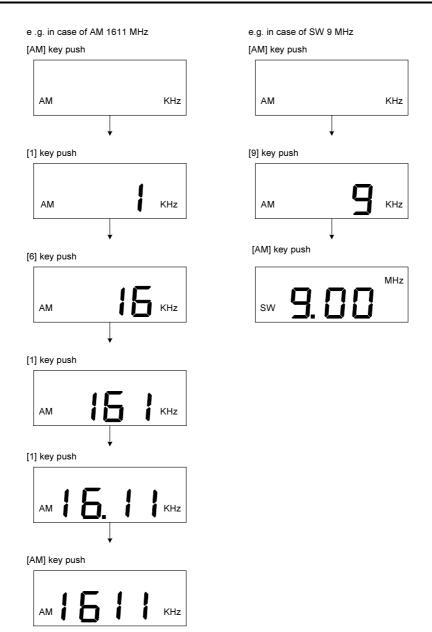
—— HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD —

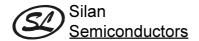


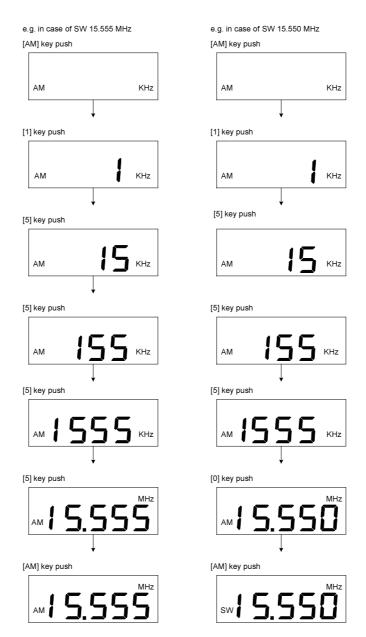


----- HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD ---









TRACKING DATA

FM (unit: MHz)

	1 ch	2 ch	3 ch	4 ch	5 ch
U.S.A	Lower	90.1	98.1	106.1	Upper
Gen.	Lower	90.1	98.1	106.1	Upper
Europe	Lower	90.1	98.1	106.1	Upper
Japan	Lower	90.1	98.1	108.1	Upper

MW9k (unit: KHz)

	1 ch	2 ch	3 ch	4 ch	5 ch
U.S.A	Lower	612	999	1404	Upper
Gen.	Lower	612	999	1404	Upper
Europe	Lower	612	999	1404	Upper
Japan	Lower	612	999	1404	Upper

MW10k (unit:KHz)

	1 ch	2 ch	3 ch	4 ch	5 ch
U.S.A	Lower	610	1000	1400	Upper
Gen.	Lower	610	1000	1400	Upper
Europe	Lower	610	1000	1400	Upper
Japan	Lower	610	1000	1400	Upper

LW (unit: kHz)

1ch	2ch	3ch	4ch	5ch
148	164	218	272	281

TV

	1 ch	2 ch	3 ch	4 ch	5 ch
U.S.A	2	4	5	9	13
Japan	1	3	4	8	12

---- HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD ----

SW (unit: MHz)

	1 ch	2 ch	3 ch	4 ch	5 ch
SW0=1, SW1=0	5.95	6.50	10.00	14.00	15.60
SW0=0, SW1=1	3.80	5.00	7.00	11.00	12.50

WB

1ch	2ch	3ch	4ch	5ch
1	2	4	6	7

SLEEP

1. Principal function

The power is off after sleep time.

2. Input ports end key to be used.

SLEEP key

- 3.Function
 - a. When the SLEEP key is pushed. The sleep function is set and the time is displayed for 5 seconds.
 - b. The sleep times is changed as shown below, every pushing the SLEEP key during the sleep time is displayed.

$$90 \longrightarrow 80 \longrightarrow 70 \longrightarrow 60 \longrightarrow 50 \longrightarrow 40 \longrightarrow 30 \longrightarrow 20 \longrightarrow 10 \longrightarrow \text{off}$$

- c. the sleep mark is on during the sleep function is set.
- d. The sleep function is cleared. If the SLEEP key was pushed when the sleep time is not displayed and sleep function is set.
- e. The power is automatically off after sleep time, when function is set.

CLOCK

1. Principal function

The clock of 12H and 24H

2. Key to be used

UP/HOUR key. DOWN/MIN key. MEMORY/CLOCK-ADJUSTMENT key, BAND-DUAL key. DUAL-dis jumper. CLOCK-dis jumper, 12/24h jumper.

3. Functions

---- HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD ----



a. The condition of the clock function is set as shown below according to setting of the CLOCK-dis jumper.

Without CLOCK-dis jumper: clock enable

With CLOCK-dis jumper: clock disable

- b. The clock function is only the power off. So clock display and clock adjustment is not disable when power is on.
- c. If the MEMORY/CLOCK-ADJUSTMENT key is pushed in clock display, the clock adjusting enable state is set for 5 second.
- d. In that state, the hour of the clock is adjusted by pushing the UP/HOUR key, and the minute of clock is adjusted by pushing the DOWN/MIN key.
- e. If the UP/HOUR key, the DOWN/MIN key is not pushed for 5 seconds in clock adjusting enable state, that state will be released. In this case, the second is not set the zero.
- f. When the MEMORY/CLOCK-ADJUSTMENT key is pushed in the clock adjusting enable state, the second of the clock is set to the zero and that state are released.
- g. The minute or the hour step up by 1 step/1 push, when the UP/HOUR key or the DOWN/MIN key is pushed for less than 500ms in clock adjusting enable state. The hour step up continuously by 1 step /250 ms by UP/HOUR key is pushed for more than 500ms. the minute step up continuously by 1 step/150ms by the [DOWN/MIN] key is pushed for more than 500ms
- h. The condition of the clock display is set as shown according to setting of the 12/24h jumper.

Without 12/24 jumper 12H display

With 12/24 jumper 24H display

i. The condition of the how many clocks is set as shown below according to setting of the DUAL-dis, jumper.

Without DUAL-dis. jumper: 1 clock

With DUAL-dis. jumper: 2 clocks

In case of 2 clocks, the clocks have minute in common, so it can change only hour. The clock changed to clock1 or clock2 by BAND-DUAL key.

ALARM

1.Principal function

The alarm is set.

2.Key to be used

UP/HOUR key, DOWN/MIN key, MEMORY/CLOCK-ADJUSTMENT key, ALARM key, BUZR (p3-1) output.

—— HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD —



3.Functions

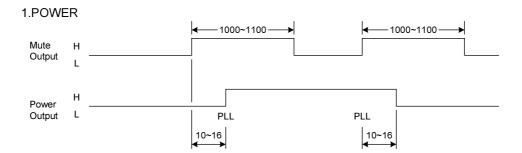
- a. When the clock is disable, the alarm is disable.
- b. The alarm is enable when power is on and power is off.
- c. If the ALARM key is pushed. The alarm adjusting enable state is set for 5 seconds, and the alarm times flash at 1 Hz rate.
 - In that state, the hour of the alarm is adjusted by pushing the UP/HOUR key, and the minute of alarm is adjusted by pushing the DOWN/MIN key.
- d. If the any keys are not pushed for 5 seconds, the alarm adjusting enable state will be released.
- e. When the MEMORY/CLOCK-ADJUSTMENT key is pushed in the alarm adjusting enable state, that state is released and alarm times is changed flash to on. So if the any keys are not pushed 5 seconds, the alarm display state is released.
- f. The hour or the minute step up by 1 step/ 1 push, if the key is pushed for less than 500ms in alarm adjusting enable state.
 - If the key is pushed more than 500 ms in this state, the hour step up continuously by 1 step/ 250ms, the minute step up continuously by 1 step/150ms.
- g. If alarm time comes same to clock time, the alarm sound is output by BUZR (p3-1) port. In that state if the any keys are pushed, the alarm sound is released. But if the any keys are not pushed, the alarm sound is output for 60 minutes.

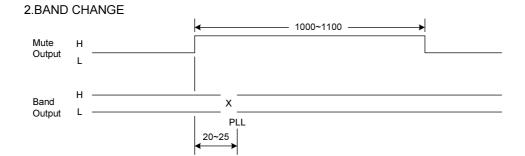


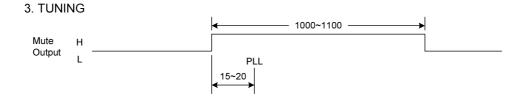
TIMING

PLL.....The timing to set the PLL data

CAUTION: If there is not instruction about the numerical value, their unit is millisecond.

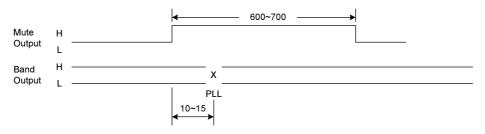




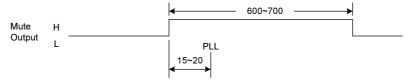




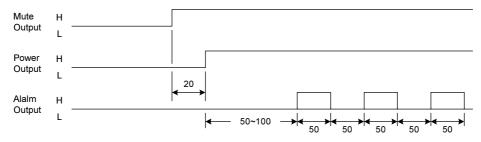
4. FREQUENCY INPUT DIRECTLY



5.PRESET MEMORY



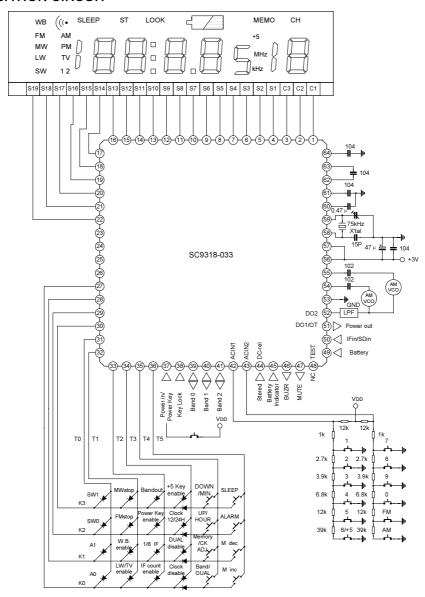
6. ALARM FUNCTION



BEEP sound freq = 3.125kHz



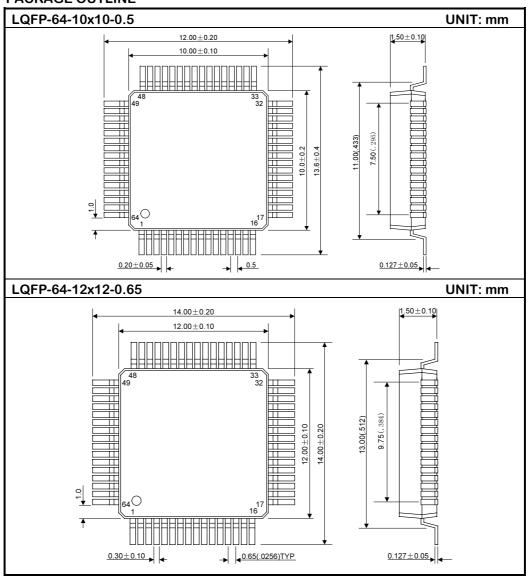
APPLICATION CIRCUIT



----- HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD ----



PACKAGE OUTLINE



---- HANGZHOU SILAN MICROELECTRONICS JOINT-STOCK CO.,LTD ----