Keyboard Encoder

FEATURES

- One integrated circuit required for complete keyboard assembly
- N key rollover or lock out operation
- Quad mode operation
- Lock out/rollover selection under external control (option)
- Self-contained or slave oscillator circuit
- 10 output data bits available
- Outputs directly compatible with TTL/DTL or MOS logic arrays
- Output data buffer register included
- Output enable provided (option)
- External data complement control provided (option)
- Pulse or level data ready output signal provided (option)
- "Any Key Down" output provided (option)
- Externally controlled delay network provided to eliminate the effect of contact bounce
- Programmable coding with a single mask change
- Static charge protection on all input and output terminals
- Entire circuit protected by a layer of glass passivation

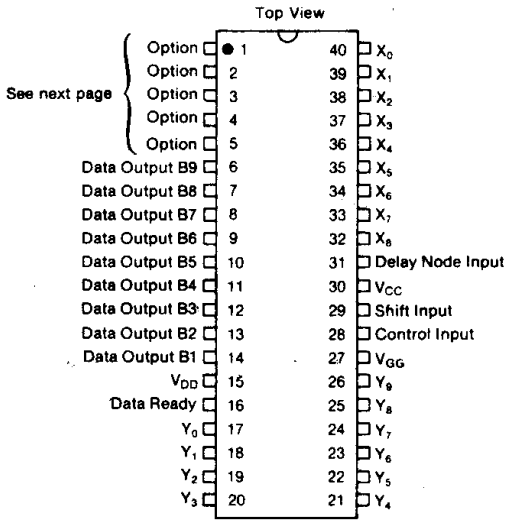
DESCRIPTION

The General Instrument AY-5-3600 is a Keyboard Encoder containing a 3600 bit Read Only Memory and all the logic necessary to encode single pole single throw keyboard closures into a usable 10 bit code. Data, Any Key Down and Data Ready outputs are directly compatible with TTL/DTL or MOS logic arrays without the need for any special interface components.

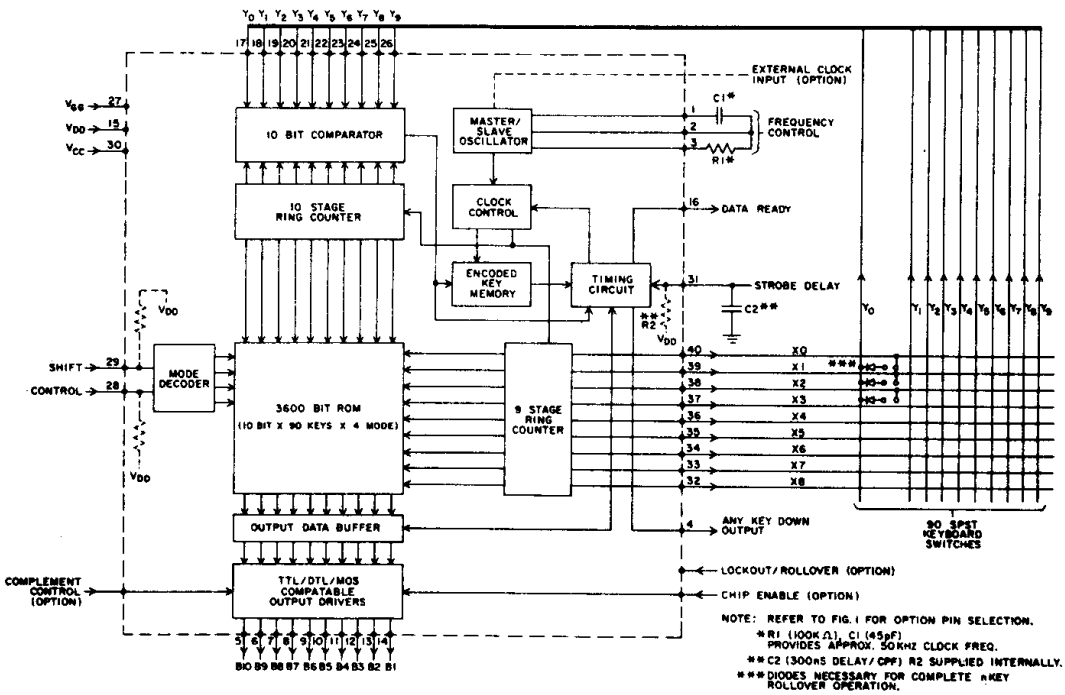
The AY-5-3600 is fabricated with MTNS technology and contains 5000 P channel enhancement mode transistors on a single monolithic chip.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



CUSTOM CODING INFORMATION

The custom coding information for General Instrument's AY-5-3600 Keyboard Encoder ROM should be transmitted to General Instrument in the form of 80 column punched cards. Each ROM pattern requires 92 cards (1 title card, 1 circuit option card and 90 ROM pattern cards). (See Note 1)

If it is not possible to supply punched cards, then the Truth Table should be completed (See Note 1). However, there would be a substantial savings in both the coding charge and turn-around time if punched cards were used. Upon receipt of the punched cards or the Truth Table, General Instrument will prepare a computer-generated Truth Table which will be returned to the user for verification.

NOTE 1: Card and Truth Table format available upon request.

PIN OPTIONS

Pins 6-40 of the AY-5-3600 are permanently assigned. The functions assigned to pins 1-5 depend on which functional options are selected from the following:

External Clock
—requires one package pin to input an external clock source.
Internal Oscillator
—requires three package pins interconnected with an external RC network to develop the clock required.
Lockout/Rollover (LO/RO)
—requires one package pin to externally select N-Key Lockout or N-Key Rollover. LO = +5V, RO = GND.
Complement Control (CC)
—requires one package pin to externally control the logic state of the data bits (B1-B10) and, if required, the Data Ready output.
Chip Enable (CE)
—requires one package pin to control the data bits (B1-B10) and, if required, the Data Ready and Any Key Output.
Any Key Output (AKO)
—requires one package pin to indicate a key depression.
Output Data Bit 10 (B10)
—requires one package pin when ten data bits are required to encode each key.

Select the pin options desired:
External Clock + 4 of the following functions
OR
Internal Oscillator + 2 of the following functions
LO/RO, CC, CE, AKO, BIO

The following chart lists the pin assignments according to the functions selected above:

PIN 1	PIN 2	PIN 3	PIN 4	PIN 5
External Clock	LO/RO	CC	CE	AKO
External Clock	LO/RO	CC	CE	BIO
External Clock	LO/RO	CC	AKO	BIO
External Clock	LO/RO	CE	AKO	BIO
External Clock	CC	CE	AKO	BIO
Internal Oscillator			LO/RO	CC
			LO/RO	CE
			LO/RO	AKO
			LO/RO	BIO
			CC	CE
			CC	AKO
			CC	BIO
			CE	AKO
			CE	BIO
			AKO	BIO

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} and V_{GG} (with respect to V_{CC}) . . . . . −20V to +0.3V
Logic input voltages (with respect to V_{CC}) . . . . . −20V to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature Range. . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts
V_{GG} = −12 Volts ±1.0 Volts, V_{DD} = GND
(V_{CC} = Substrate Voltage)
Operating Temperature (T_A) = 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
Clock Frequency	f	10	50	100	kHz	See Block diagram footnote* for typical R-C values
External Clock Width		7	—	—	μs	
Clock Input						
	V_{I0}	V_{GG}	—	.15	V	
	V_{I1}	V_{CC} −1.4	—	V_{CC} +0.3	V	
Data Input						
(Shift, Control, Complement Control, Lockout/Rollover, Chip Enable & External Clock)						
Logic "0" Level	V_{I0}	V_{GG}	—	+0.75	V	
Logic "1" Level	V_{I1}	V_{CC} −1.1	—	V_{CC}+0.3	V	
Shift & Control Input Current	I_{NSC}	75	95	120	μA	V_I = +5V
X Output (X_0-X_8)						
Logic "1" Output Current	I_{XI}	40	170	400	μA	V_{OUT} = V_{CC} (See Note 2)
		600	1300	2500	μA	V_{OUT} = V_{CC}−1.3V
		900	1600	3500	μA	V_{OUT} = V_{CC}−2.0V
		1500	3800	6000	μA	V_{OUT} = V_{CC}−5V
		3000	6000	10000	μA	V_{OUT} = V_{CC}−10V
Logic "0" Output Current	I_{XO}	8	15	50	μA	V_{OUT} = V_{CC}
		6	11	35	μA	V_{OUT} = V_{CC}−1.3V
		5	10	30	μA	V_{OUT} = V_{CC}−2.0V
		2	5	15	μA	V_{OUT} = V_{CC}−5V
		—	0.5	5	μA	V_{OUT} = V_{CC}−10V
Y Input (Y_0-Y_9)						
Trip Level	V_Y	V_{CC}−5	V_{CC}−3	V_{CC}−2	V	Y Input Going Positive (See Note 2)
Hysteresis	ΔV_Y	0.5	0.9	1.4	V	(See Note 1)
Selected Y Input Current	I_{YS}	18	36	100	μA	V_{IN} = V_{CC}
		14	28	90	μA	V_{IN} = V_{CC}−1.3V
		13	25	80	μA	V_{IN} = V_{CC}−2.0V
		6	12	60	μA	V_{IN} = V_{CC}−5V
		—	1	30	μA	V_{IN} = V_{CC}−10V
Unselected Y Input Current	I_{YU}	9	18	50	μA	V_{IN} = V_{CC}
		7	14	45	μA	V_{IN} = V_{CC}−1.3V
		6	13	40	μA	V_{IN} = V_{CC}−2.0V
		3	6	30	μA	V_{IN} = V_{CC}−5V
		—	0.5	15	μA	V_{IN} = V_{CC}−10V
Input Capacitance	C_{IN}	—	3	10	pF	at 0V (All Inputs)
X-Y Precharge Characteristics	φP	1500	3500	5000	μA	V = V_{CC}
		200	600	1500	μA	V = V_{CC}−5 (See Note 2)
Switch Characteristics						
Minimum Switch Closure	—	—	—	—	—	See Timing Diagram
Contact Closure Resistance	Z_{CC}	—	—	300	Ω	
	Z_{CO}	1 × 10^7	—	—	Ω	
Strobe Delay						
Trip Level (Pin 31)	V_{SD}	V_{CC}−4	V_{CC}−3	V_{CC}−2	V	
Hysteresis	V_{SD}	0.5	0.9	1.4	V	(See Note 1)
Quiescent Voltage (Pin 31)		−3	−5	−9	V	With Internal Switched Resistor
Data Output (B1-B10), Any Key Down Output, Data Ready						
Logic "0"	—	—	—	.55	V	I_{OL} = .25mA
	—	—	—	0.8	V	I_{OL} = 1.6mA
Logic "1"	—	V_{CC} −1.3	—	—	V	I_{OH} = .95mA
Power						
I_{CC}	—	—	8	13	mA	V_{CC} = +5V
I_{GG}	—	—	8	13	mA	V_{GG} = −12V

**Typical values are at +25°C and nominal voltages.

NOTE

1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Precharge of X outputs and Y inputs occurs during each scanned clock cycle.

OPERATION

The AY-5-3600 contains (see Block Diagram) a 3600 bit ROM, 9-stage and 10-stage ring counters, a 10 bit comparator, timing circuitry, a 90 bit memory to store the location of encoded keys for n key rollover operation, an externally controllable delay network for eliminating the effect of contact bounce, an output data buffer, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 360 by 10 bit memory arranged into four 90-word by 10-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the four 90-word groups; the 90-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

The external outputs of the 9-stage ring counter and the external inputs to the 10-bit comparator are wired to the keyboard to form an X-Y matrix with the 90-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM, thereby scanning the key switches for key closures.

When a key is depressed, a single path is completed between one output of the 9-stage ring counter (X0 thru X8) and one input of the 10-bit comparator (Y_0-Y_9). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 10-stage ring counter.

N KEY ROLLOVER

— When a match occurs, and the key has not been encoded, the switch bounce delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears, a one is stored in the encoded key memory and the scan sequence is resumed. If a match occurs at another key location, the sequence is repeated thus encoding the next key. If the match occurs for an already encoded key, the match is not recognized. The code of the last key encoded remains in the output data buffer.

N KEY LOCKOUT

— When a match occurs, the delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears and the remaining keys are locked out by halting the scan sequence. The scan sequence is resumed upon key release. The output data buffer stores the code of the last key encoded.

SPECIAL PATTERNS

— Since the selected coding of each key and all the options are defined during the manufacture of the chip, the coding and options can be changed to fit any particular application of the keyboard. Up to 360 codes of up to 10 bits can be programmed into the AY-5-3600 ROM covering most popular codes such as ASCII, EBCDIC, Selectric, etc., as well as many specialized codes. The ASCII code in conjunction with internal oscillator, 10 data outputs and any key down output, is available as a standard pattern (See Figure 2).

TIMING DIAGRAM

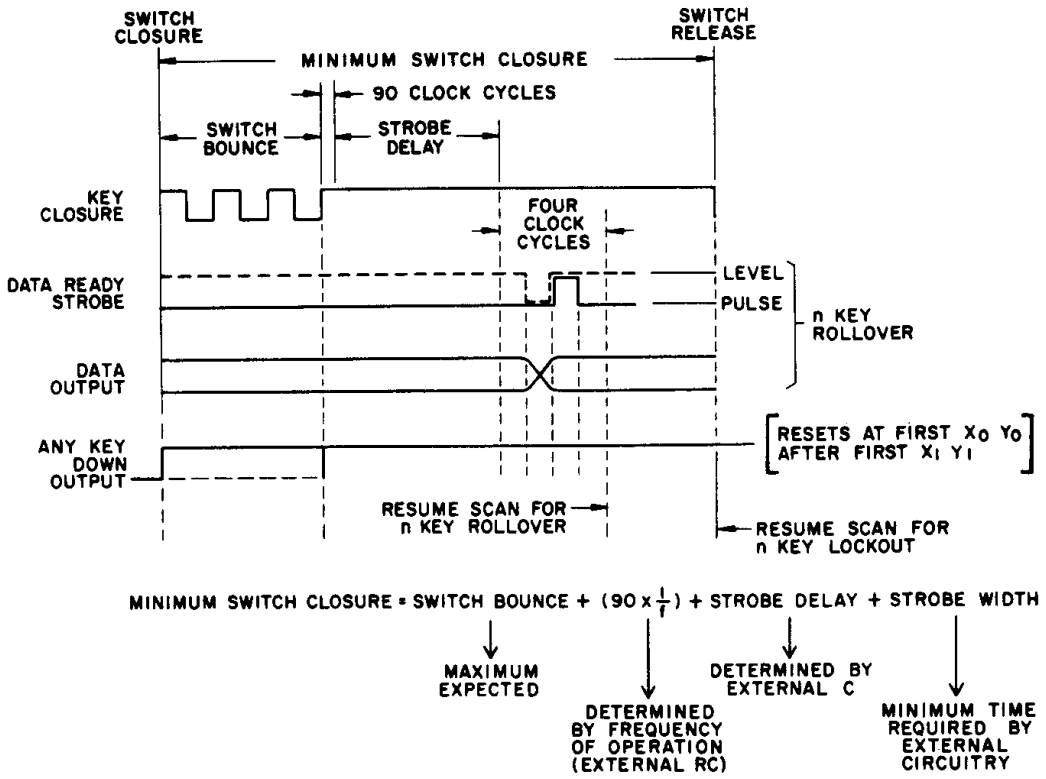


Fig.1

SYMBOL	MODE N	MODE S	MODE C	MODE SC
@		X1 Y0, X0 Y8		
A		X0 Y2		X1 Y2
B		X5 Y3		X2 Y2
C		X2 Y3		X3 Y2
D		X2 Y2		X4 Y2
E		X2 Y1		X5 Y2
F		X3 Y2		X6 Y2
G		X4 Y2		X7 Y2
H	X0 Y5	X0 Y5, X5 Y2	X0 Y5	X0 Y5
I		X7 Y1		X0 Y4
J		X6 Y2		X6 Y6
K		X7 Y2		X3 Y6
L	X2 Y6	X2 Y6, X8 Y2	X2 Y6	X2 Y6
M		X7 Y3		X3 Y5
N		X6 Y3		X4 Y5
O		X8 Y1		
P		X6 Y6		X0 Y2, X0 Y3
Q		X0 Y1		X1 Y3
R		X3 Y1		X2 Y3
S		X1 Y2		X4 Y3
T		X4 Y1		X5 Y3
U		X0 Y1		X6 Y3
V		X4 Y3		X7 Y3
W		X1 Y1		X6 Y5
X		X1 Y3		X8 Y2
Y		X5 Y1		X5 Y6
Z		X0 Y3		X5 Y5
a	X0 Y2		X0 Y2	
b	X5 Y3		X5 Y3	
c	X2 Y3		X2 Y3	
d	X2 Y2		X2 Y2	
e	X2 Y1		X2 Y1	
f	X3 Y2		X3 Y2	
g	X4 Y2		X4 Y2	
h	X5 Y2		X5 Y2	
i	X7 Y1		X7 Y1	
j	X6 Y2		X6 Y2	
k	X7 Y2, X2 Y9		X7 Y2	
l	X8 Y2		X8 Y2	
m	X7 Y3, X1 Y6		X7 Y3	
n	X6 Y3, X1 Y8		X6 Y3	
o	X8 Y1		X8 Y1	
p	X6 Y6, X0 Y8		X6 Y6	
q	X0 Y1		X0 Y1	
r	X3 Y1		X3 Y1	
s	X1 Y2		X1 Y2	
t	X4 Y1		X4 Y1	
u	X6 Y1		X6 Y1	
v	X4 Y3		X4 Y3	
w	X1 Y1		X1 Y1	
x	X1 Y3		X1 Y3	
y	X5 Y1		X5 Y1	
z	X0 Y3		X0 Y3	
[		X8 Y6, X2 Y9		X4 Y6, X8 Y6
\				X1 Y1
]	X8 Y6	X1 Y6	X8 Y6	X8 Y1
^		X1 Y8		X2 Y4
_	X4 Y7, X8 Y7		X4 Y7, X8 Y7	X4 Y7
`	X3 Y6	X3 Y6	X3 Y6	
{	X4 Y5	X4 Y5	X4 Y5	
|				X6 Y4
}		X2 Y8		X2 Y9
~			X5 Y7, X0 Y8	X5 Y7, X0 Y8
DEL				
NULL	X5 Y7	X5 Y7		

SYMBOL	MODE N	MODE S	MODE C	MODE SC
SOH			X0 Y9	X5 Y0, X0 Y8
STX			X1 Y9	X4 Y0, X1 Y8
ETX	X4 Y4	X4 Y4	X4 Y4	X4 Y4, X6 Y0
EOT				X4 Y1
ENQ				X3 Y1
ACK			X2 Y8	X7 Y1, X2 Y8
BEL			X3 Y8	X6 Y1, X3 Y8
BS				X3 Y4
HT	X0 Y4	X0 Y4	X0 Y4, X8 Y8	X8 Y8
LF	X7 Y6	X7 Y6	X7 Y6	
VT	X3 Y7	X3 Y7	X3 Y7	X3 Y7
FF	X7 Y8		X7 Y8	X7 Y8
CR	X3 Y5	X3 Y5	X3 Y5, X1 Y6	X1 Y6
SO	X0 Y7		X0 Y7, X1 Y8	X0 Y7, X1 Y8
SI	X1 Y7	X1 Y7	X1 Y7	X1 Y7
DLE				X0 Y1
DC1				X5 Y1
DC2				X6 Y7
DC3				X2 Y1
DC4				X3 Y0
NAK				X2 Y0
SYN				X5 Y4
ETB				X1 Y0
CAN	X3 Y4		X3 Y4	
EM				X8 Y0
SUB				X0 Y0
ESC				X7 Y0
FS				X1 Y4
GS				X7 Y6
RS	X1 Y4	X1 Y4	X1 Y4	
US	X2 Y7	X2 Y7	X2 Y7	X2 Y7
SP	X3 Y3, X4 Y9	X4 Y9, X3 Y3	X4 Y9, X3 Y3	X4 Y9, X3 Y3
!	X5 Y9	X5 Y9, X0 Y9	X5 Y9	X5 Y9
"	X3 Y9	X3 Y9, X7 Y5, X1 Y9	X3 Y9	X3 Y9, X7 Y5
#	X8 Y9	X6 Y9, X2 Y0	X6 Y9	X6 Y9
$	X2 Y5	X2 Y5, X3 Y0	X2 Y5	X2 Y5
%	X1 Y5	X1 Y5, X4 Y0	X1 Y5	X1 Y5
&	X6 Y8	X6 Y0, X6 Y8, X2 Y8	X6 Y8	X6 Y8
'	X7 Y5	X3 Y8	X7 Y5	X7 Y4
(	X7 Y9	X7 Y4, X3 Y4, X8 Y0	X7 Y9	X7 Y9
)	X4 Y8	X4 Y8, X6 Y7, X8 Y9	X4 Y8	X4 Y8
*	X5 Y8	X5 Y8, X7 Y0, X5 Y4	X5 Y8	X5 Y8
+	X0 Y6	X0 Y6, X5 Y6, X7 Y7	X0 Y6	X0 Y6, X7 Y7
,	X8 Y3	X8 Y3	X8 Y3	X8 Y3
-	X2 Y4	X2 Y4, X8 Y7	X2 Y4	X8 Y7
.	X8 Y4	X8 Y4	X8 Y4	X8 Y4
/	X7 Y4		X7 Y4	
0	X6 Y7, X8 Y8	X8 Y8	X6 Y7, X8 Y8	X8 Y8
1	X0 Y0, X0 Y9		X0 Y0	
2	X1 Y0, X1 Y9		X1 Y0	
3	X2 Y6		X2 Y0	
4	X3 Y0		X3 Y0	
5	X4 Y0		X4 Y0	
6	X5 Y0, X2 Y8		X5 Y0	
7	X6 Y0, X3 Y8		X0 Y0	
8	X7 Y0		X7 Y0	
9	X8 Y0, X8 Y9		X8 Y0	
:	X5 Y4	X8 Y5	X5 Y4	X8 Y5
;	X8 Y5, X5 Y8		X8 Y5, X5 Y6	
<	X6 Y5	X7 Y8, X6 Y5, X0 Y0	X8 Y5	
=	X8 Y4, X7 Y7	X7 Y7, X6 Y4, X4 Y7	X8 Y4	
>	X5 Y5	X5 Y5, X5 Y0, X0 Y7	X5 Y5	
?	X4 Y8	X4 Y6, X7 Y4	X4 Y6	

Note 1. Bits 1 to 6 and bit 8 of the AY-5-3600 correspond to bits 1 to 7 of ASC II.

Note 2. Codes 0000011 and 0011111 are not present in the standard AY-5-3600 pattern.

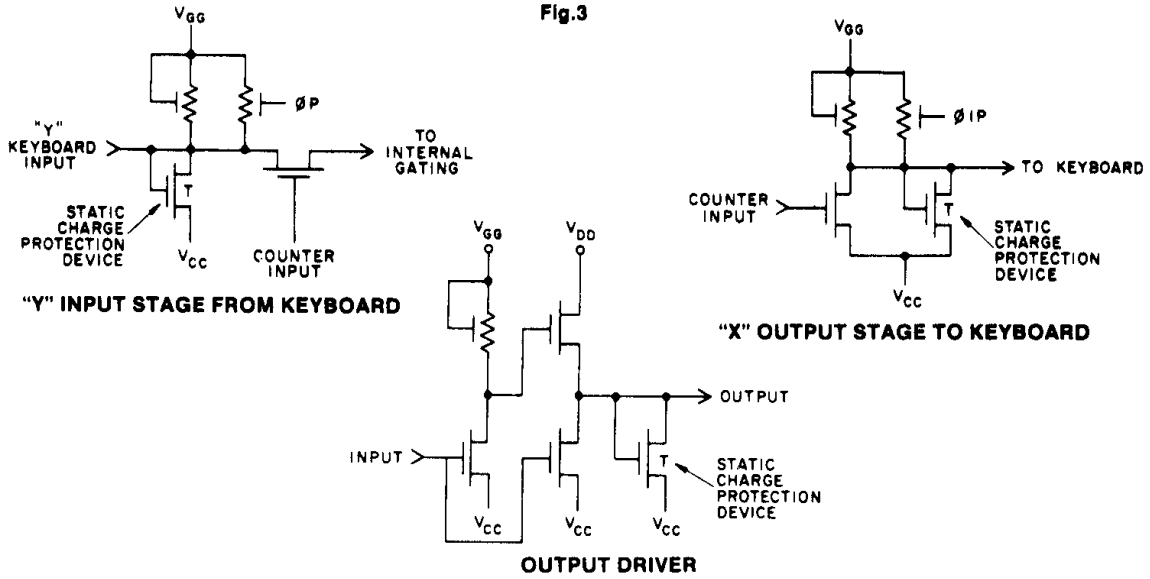
Fig.2 STANDARD AY-5-3600 CODE ASSIGNMENTS (ASCII CODE)

OPTIONS PROVIDED WITH STANDARD ENCODER

- Device Marking: AY-5-3600
- Internal Oscillator on Pin Nos. 1, 2, 3
- Any Key Output on Pin No. 4
- Any Key Output True (Logic 1) During Key Depression
- Output Data Bit B10 on Pin No. 5
- N-Key Rollover Only
- True Outputs Only
- Pulse Data Ready Signal
- Internal Resistor to V_{DD} on Shift/Control Pin
- Plastic Package

ROM

Fig.3



NOTE: Output driver capable of driving one TTL load with no external resistor.
Capable of driving two TTL loads using an external 6.8KΩ resistor to V_{CC}.

TYPICAL CHARACTERISTIC CURVES

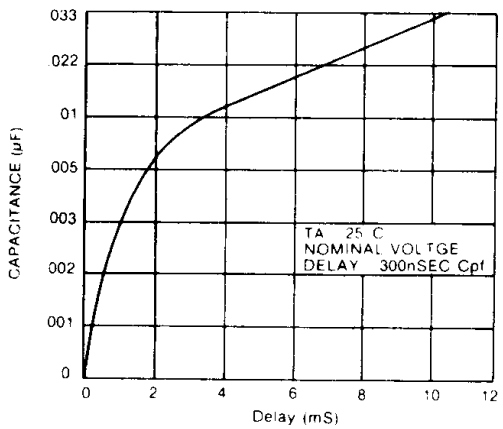


Fig.4 STROBE DELAY vs. C_1

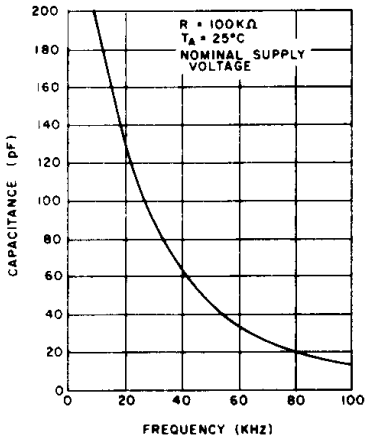


Fig.5 OSCILLATOR FREQUENCY vs. C_2

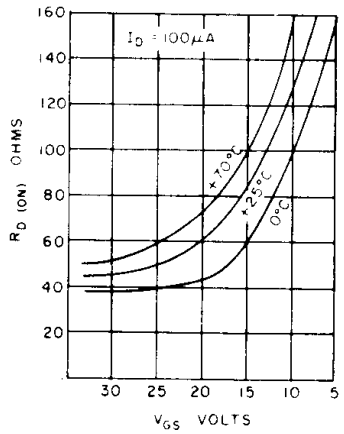


Fig.6 TYPICAL OUTPUT ON RESISTANCE (R_{DON}) vs. GATE BIAS VOLTAGE (V_{GS})

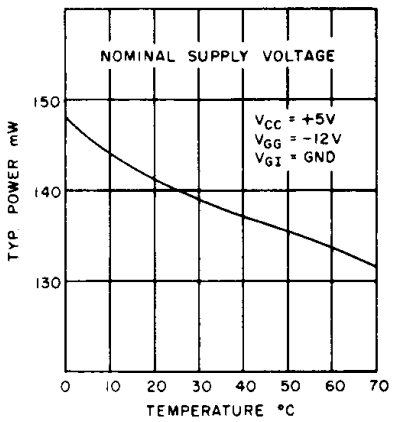


Fig.7 TYPICAL POWER CONSUMPTION (mW)