e2v technologies

CCD47-20
High Performance CCD Sensor

FEATURES

- 1024 by 1024 1:1 Image Format
- Image Area 13.3 x 13.3 mm
- Frame Transfer Operation
- 13 μm Square Pixels
- Symmetrical Anti-static Gate Protection
- Very Low Noise Output Amplifiers
- Gated Dump Drain on Output Register
- 100% Active Area

APPLICATIONS

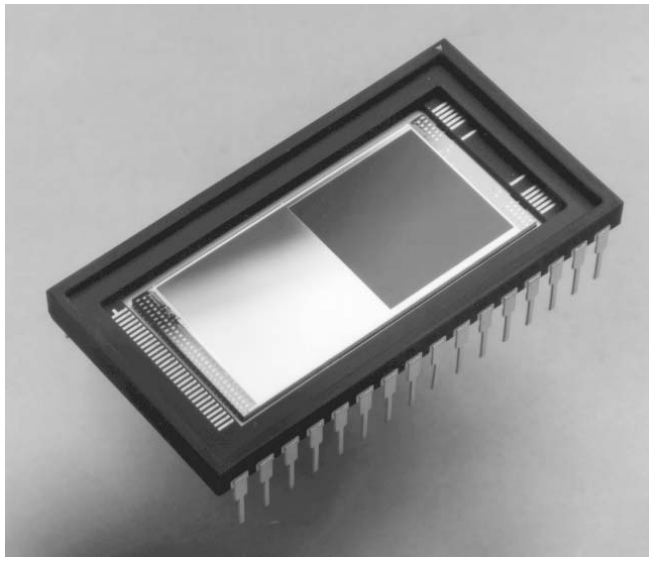
- Spectroscopy
- Scientific Imaging
- Star Tracking
- Medical Imaging

INTRODUCTION

This version of the CCD47-20 is a front-face illuminated, frame transfer CCD sensor with high performance low noise output amplifiers, suitable for use in slow-scan imaging systems. The image area contains a full 1024 by 1024 pixels which are 13 μm square. The output register is split, allowing either or both of the two output amplifiers to be employed, and is provided with a drain and control gate for charge dump purposes.

In common with all e2v technologies CCD Sensors, the CCD47-20 is available with a fibre-optic window or taper, a UV coating or a phosphor coating for X-ray detection. Other variants of the CCD47-20 include IMO, back-thinned and full-frame devices.

Designers are advised to consult e2v technologies should they be considering using CCD sensors in abnormal environments or if they require customised packaging.



TYPICAL PERFORMANCE

Maximum readout frequency	5	MHz
Output responsivity	4.5	μV/e^-
Peak signal	120	ke^-/pixel
Dynamic range (at 20 kHz)	~60 000:1	
Spectral range	400 - 1100	nm
Readout noise (at 20 kHz)	2.0	e^- rms
QE at 700 nm	45	%

GENERAL DATA

Format

Image area	13.3 x 13.3	mm
Active pixels (H)	1024	
(V)	1024	
Pixel size	13 x 13	μm
Storage area	13.3 x 13.3	mm
Pixels (H)	1024	
(V)	1024	

Additional pixels are provided in both the image and storage areas for dark reference and over-scanning purposes.

Number of output amplifiers	2	
Weight (approx, no window)	7.5	g

Package

Package size	22.7 x 42.0	mm
Number of pins	32	
Inter-pin spacing	2.54	mm
Window material	quartz or removable glass	
Type	ceramic DIL array	

e2v technologies limited, Waterhouse Lane, Chelmsford, Essex CM1 2QU England Telephone: +44 (0)1245 493493 Facsimile: +44 (0)1245 492492
e-mail: enquiries@e2vtechnologies.com Internet: www.e2vtechnologies.com Holding Company: e2v holdings limited

e2v technologies inc. 4 Westchester Plaza, PO Box 1482, Elmsford, NY10523-1482 USA Telephone: (914) 592-6050 Facsimile: (914) 592-5148
e-mail: enquiries@e2vtechnologies.us

PERFORMANCE

	Min	Typical	Max	
Peak charge storage (see note 1)	80k	120k	–	e^-/pixel
Peak output voltage (no binning)	–	540	–	mV
Dark signal at 293 K (see notes 2 and 3)	–	10k	20k	e^-/pixel/s
Dynamic range (see note 4)	–	60 000	–	
Charge transfer efficiency (see note 5):				
parallel	–	99.9999	–	%
serial	–	99.9993	–	%
Output amplifier responsivity (see note 3)	3.0	4.5	6.0	$\mu V/e^-$
Readout noise at 243 K (see notes 3 and 6):				
grade 0 and 1	–	2.0	4.0	rms e^-/pixel
grade 2	–	3.0	6.0	rms e^-/pixel
Maximum readout frequency (see note 7)	–	5.0	–	MHz
Response non-uniformity (std. deviation)	–	3	10	% of mean
Dark signal non-uniformity (std. deviation) (see notes 3 and 8)	–	1000	2000	e^-/pixel/s

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (measured at mid-clock level)

	Min	Typical	Max	
S∅/S∅ interphase	–	3.5	–	nF
I∅/I∅ interphase	–	3.5	–	nF
I∅/SS and S∅/SS	–	4.5	–	nF
R∅/R∅ interphase	–	40	–	pF
R∅/(SS + DG + OD)	–	60	–	pF
∅R/SS	–	10	–	pF
Output impedance (at typ. operating condition)	–	300	–	Ω

NOTES

1. Signal level at which resolution begins to degrade.
2. Measured between 233 and 253 K and V_{SS} +9.0 V. Dark signal at any temperature T (kelvin) may be estimated from:
   $$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$
   where Q_{d0} is the dark signal at T = 293 K (20 °C).
3. Test carried out at e2v technologies on all sensors.
4. Dynamic range is the ratio of readout noise to full well capacity measured at 243 K and 20 kHz readout speed.
5. CCD characterisation measurements made using charge generated by X-ray photons of known energy.
6. Measured using a dual-slope integrator technique (i.e. correlated double sampling) with a 20 µs integration period.
7. Readout at speeds in excess of 5 MHz into a 15 pF load can be achieved but performance to the parameters given cannot be guaranteed.
8. Measured between 233 and 253 K, excluding white defects.

BLEMISH SPECIFICATION

Traps Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^- at 243 K.

Slipped columns Are counted if they have an amplitude greater than 200 e^-.

Black spots Are counted when they have a signal level of less than 90% of the local mean at a signal level of approximately half full-well.

White spots Are counted when they have a generation rate 25 times the specified maximum dark signal generation rate (measured between 233 and 253 K). The amplitude of white spots will vary in the same manner as dark current, i.e.:
$$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$

White column A column which contains at least 21 white defects.

Black column A column which contains at least 21 black defects.

GRADE	0	1	2
Column defects:			
black or slipped	0	2	6
white	0	0	0
Black spots	15	25	100
Traps >200 e^-	1	2	5
White spots	20	30	50

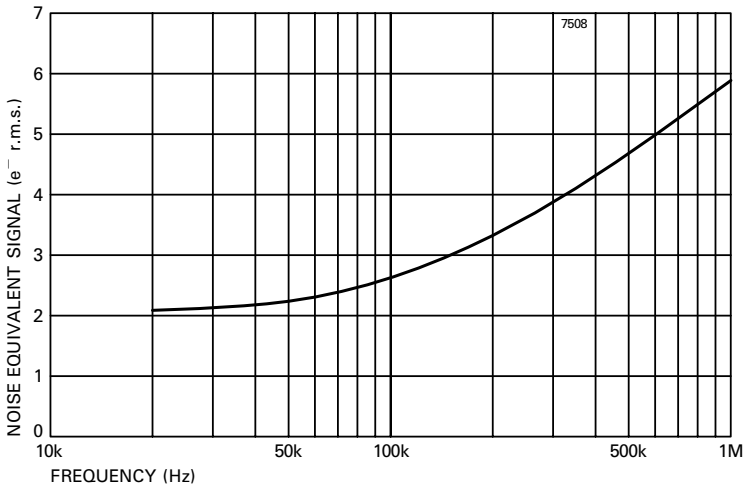
Grade 5 Devices which are fully functioning, with image quality below that of grade 2, and which may not meet all other performance parameters.

Minimum separation between adjacent black columns . . . . . 50 pixels

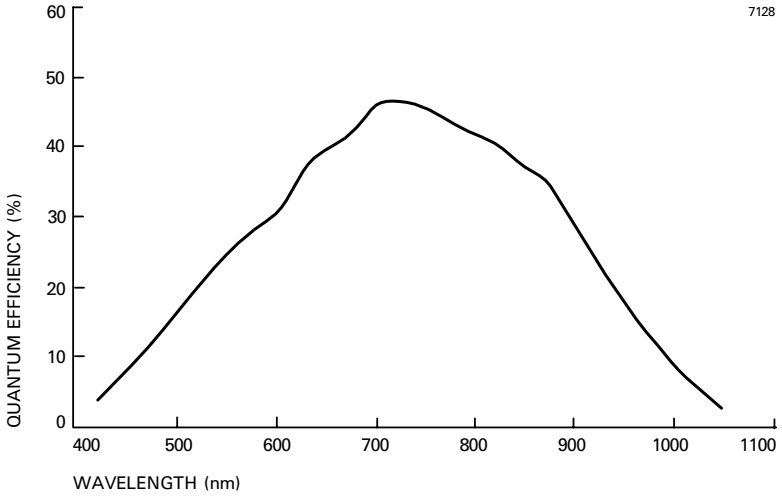
Note The effect of temperature on defects is that traps will be observed less at higher temperatures but more may appear below 233 K. The amplitude of white spots and columns will decrease rapidly with temperature.

TYPICAL OUTPUT CIRCUIT NOISE
(Measured using clamp and sample)

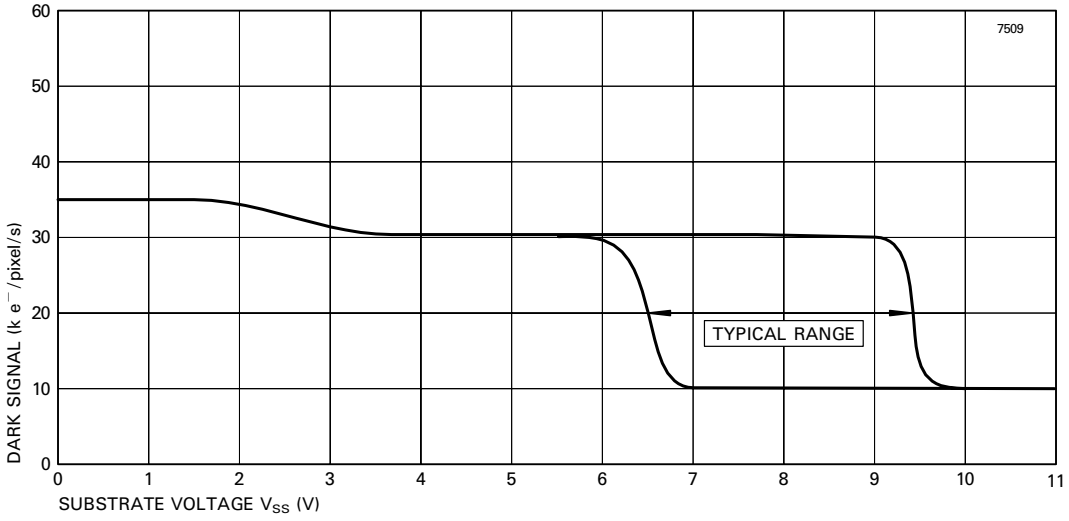
V_{SS} = 9 V V_{RD} = 18 V V_{OD} = 29 V



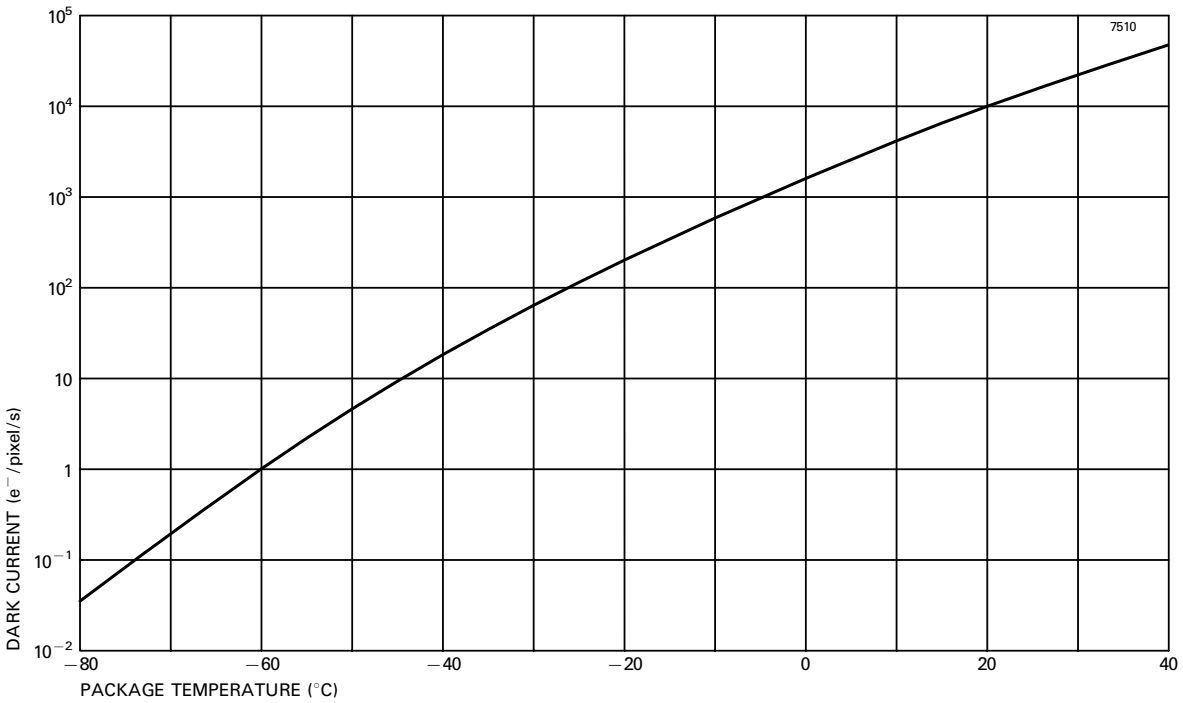
TYPICAL SPECTRAL RESPONSE
(No window)



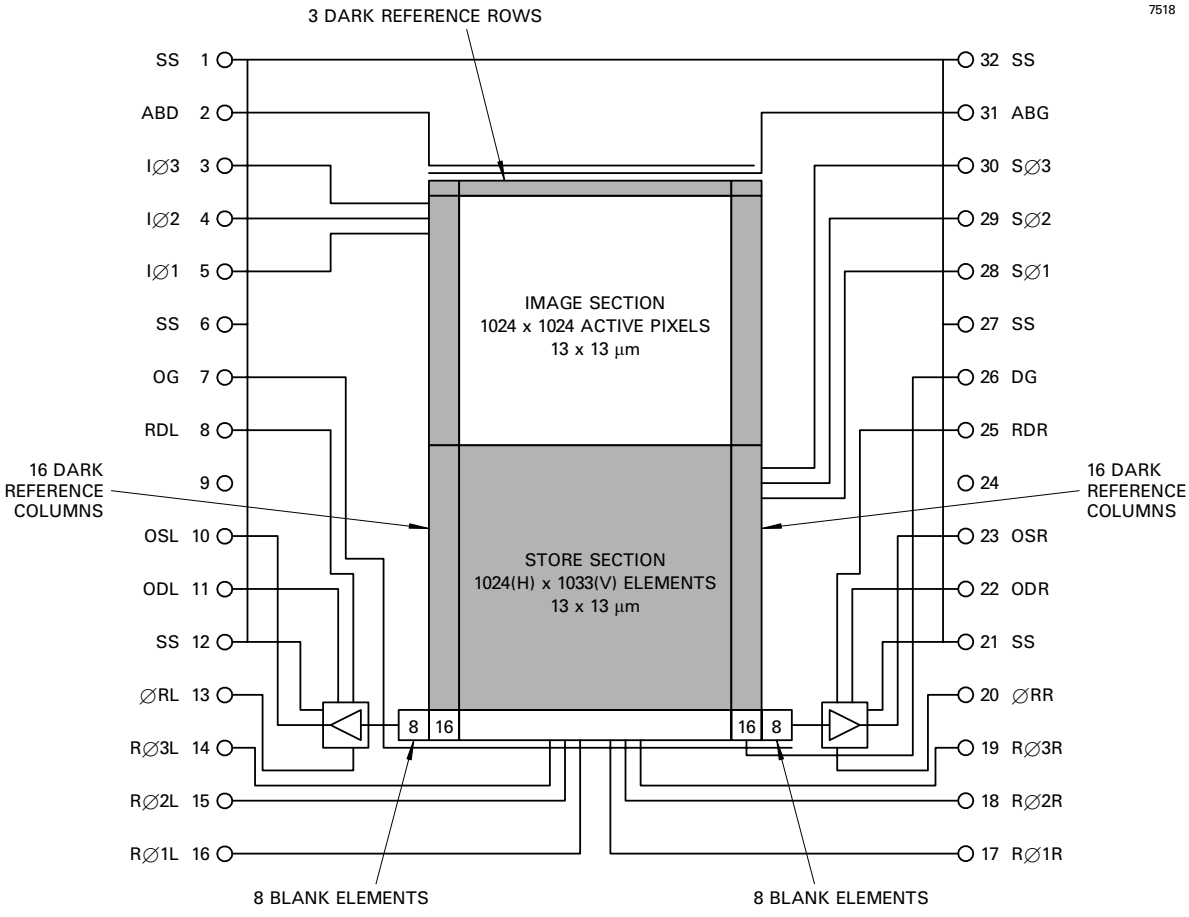
TYPICAL VARIATION OF DARK SIGNAL WITH SUBSTRATE VOLTAGE
(Two I∅ phases held low)



TYPICAL VARIATION OF DARK CURRENT WITH TEMPERATURE



DEVICE SCHEMATIC



CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

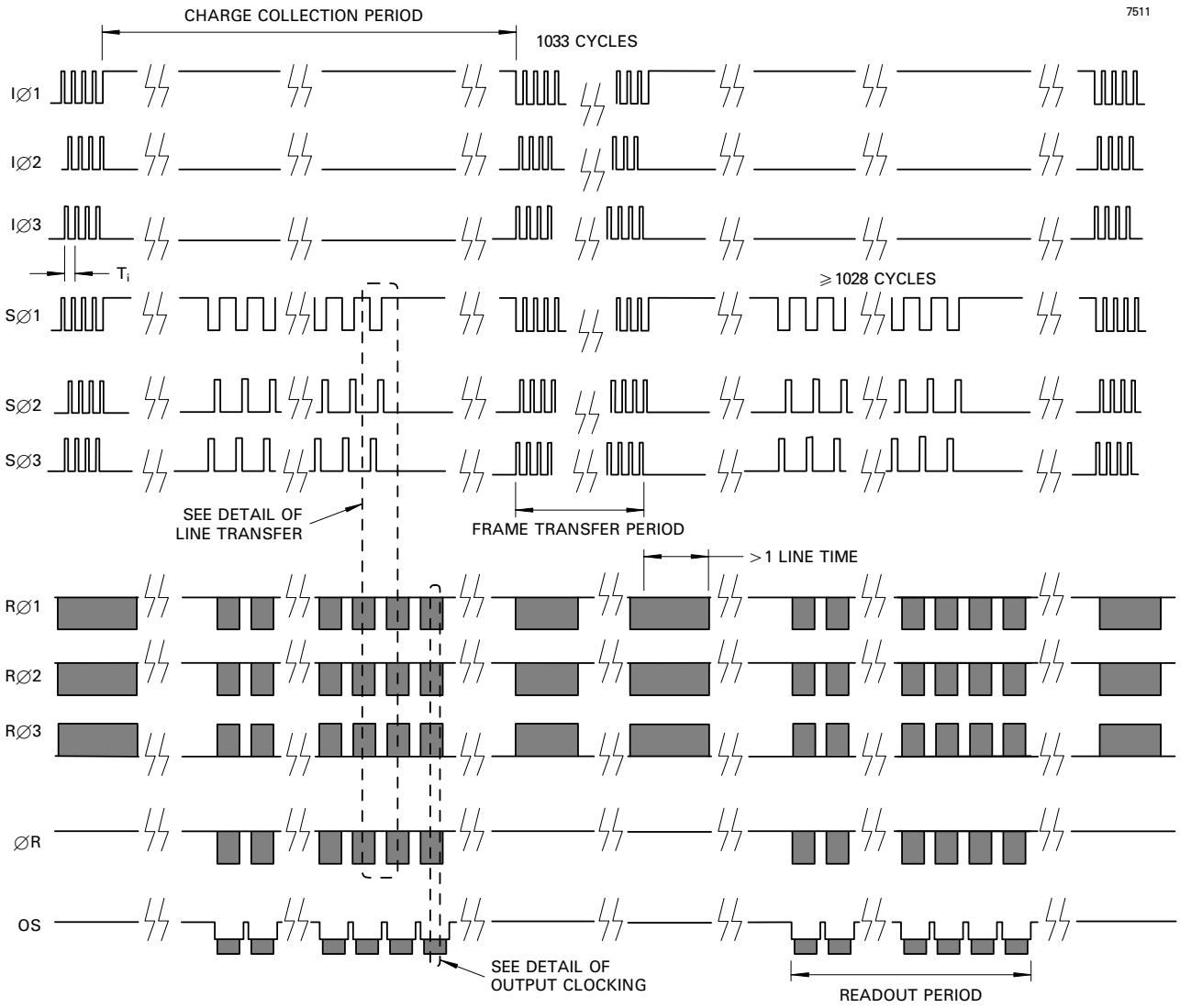
PIN	REF	DESCRIPTION	PULSE AMPLITUDE OR DC LEVEL (V) (See note 9)			MAXIMUM RATINGS with respect to V_{SS}
			Min	Typical	Max	
1	SS	Substrate	0	9	10	-
2	ABD	Anti-blooming drain (see note 10)		V_{OD}		−0.3 to +25 V
3	I∅3	Image area clock	8	12	15	±20 V
4	I∅2	Image area clock	8	12	15	±20 V
5	I∅1	Image area clock	8	12	15	±20 V
6	SS	Substrate	0	9	10	-
7	OG	Output gate	1	3	5	±20 V
8	RDL	Reset transistor drain (left amplifier)	15	17	19	−0.3 to +25 V
9	-	No connection		-		-
10	OSL	Output transistor source (left amplifier)		see note 11		−0.3 to +25 V
11	ODL	Output transistor drain (left amplifier)	27	29	31	−0.3 to +35 V
12	SS	Substrate	0	9	10	-
13	∅RL	Output reset pulse (left amplifier)	8	12	15	±20 V
14	R∅3L	Output register clock (left section)	8	10	15	±20 V
15	R∅2L	Output register clock (left section)	8	10	15	±20 V
16	R∅1L	Output register clock (left section)	8	10	15	±20 V
17	R∅1R	Output register clock (right section)	8	10	15	±20 V
18	R∅2R	Output register clock (right section)	8	10	15	±20 V
19	R∅3R	Output register clock (right section)	8	10	15	±20 V
20	∅RR	Output reset pulse (right amplifier)	8	12	15	±20 V
21	SS	Substrate	0	9	10	-
22	ODR	Output transistor drain (right amplifier)	27	29	31	−0.3 to +35 V
23	OSR	Output transistor source (right amplifier)		see note 11		−0.3 to +25 V
24	-	No connection		-		-
25	RDR	Reset transistor drain (right amplifier)	15	17	19	−0.3 to +25 V
26	DG	Dump gate (see note 12)	-	0	-	±20 V
27	SS	Substrate	0	9	10	-
28	S∅1	Storage area clock	8	12	15	±20 V
29	S∅2	Storage area clock	8	12	15	±20 V
30	S∅3	Storage area clock	8	12	15	±20 V
31	ABG	Anti-blooming gate	0	0	5	±20 V
32	SS	Substrate	0	9	10	-

Maximum voltages between pairs of pins:
pin 10 (OSL) to pin 11 (ODL) . . . . . ±15 V
pin 22 (ODR) to pin 23 (OSR) . . . . . ±15 V
Maximum output transistor current . . . . . 10 mA

NOTES

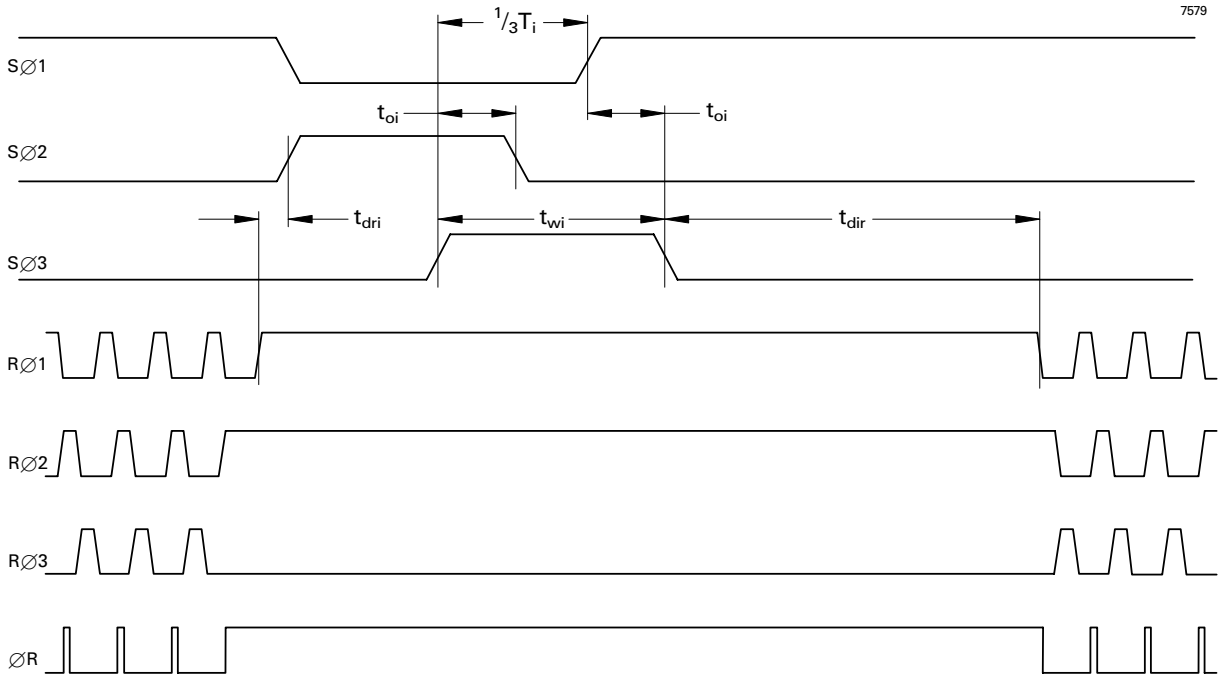
9. Readout register clock pulse low levels +1 V; other clock low levels 0±0.5 V.
10. Drain not incorporated, but bias is still necessary.
11. 3 to 5 V below OD. Connect to ground using a 2 to 5 mA current source or appropriate load resistor (typically 5 to 10 kΩ).
12. Non-charge dumping level shown. For operation in charge dumping mode, DG should be pulsed to 12 ± 2 V.
13. All devices will operate at the typical values given. However, some adjustment within the minimum to maximum range may be required for to optimise performance for critical applications. It should be noted that conditions for optimum performance may differ from device to device.
14. With the R∅ connections shown, the device will operate through the left-hand output only. In order to operate from both outputs R∅1(R) and R∅2(R) should be reversed.

FRAME TRANSFER TIMING DIAGRAM

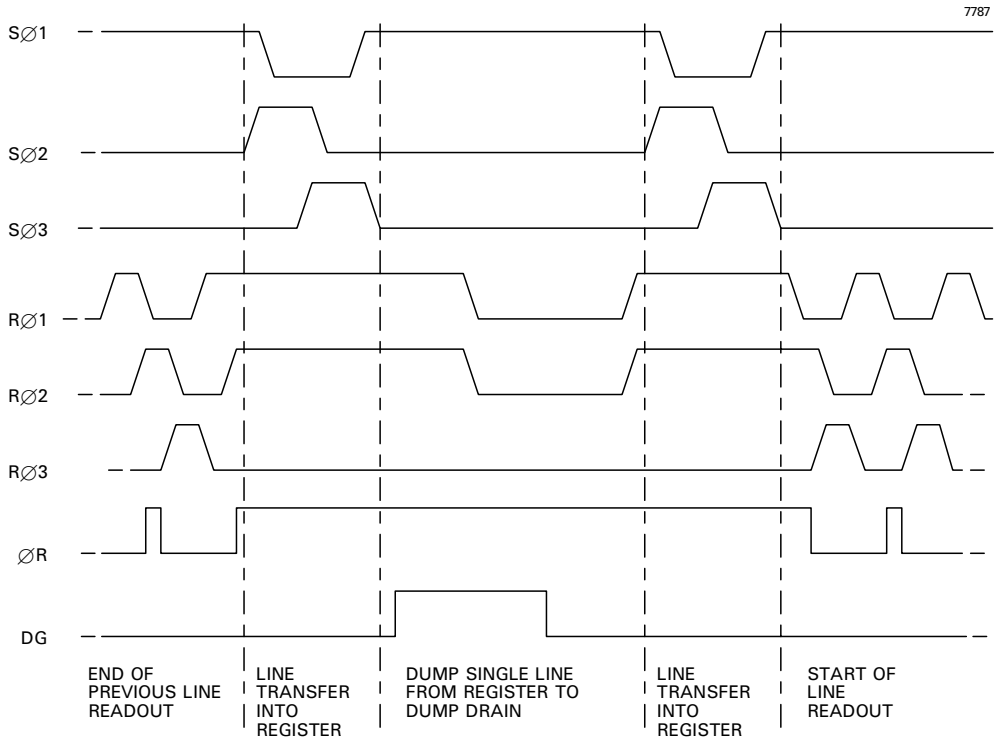


DETAIL OF LINE TRANSFER

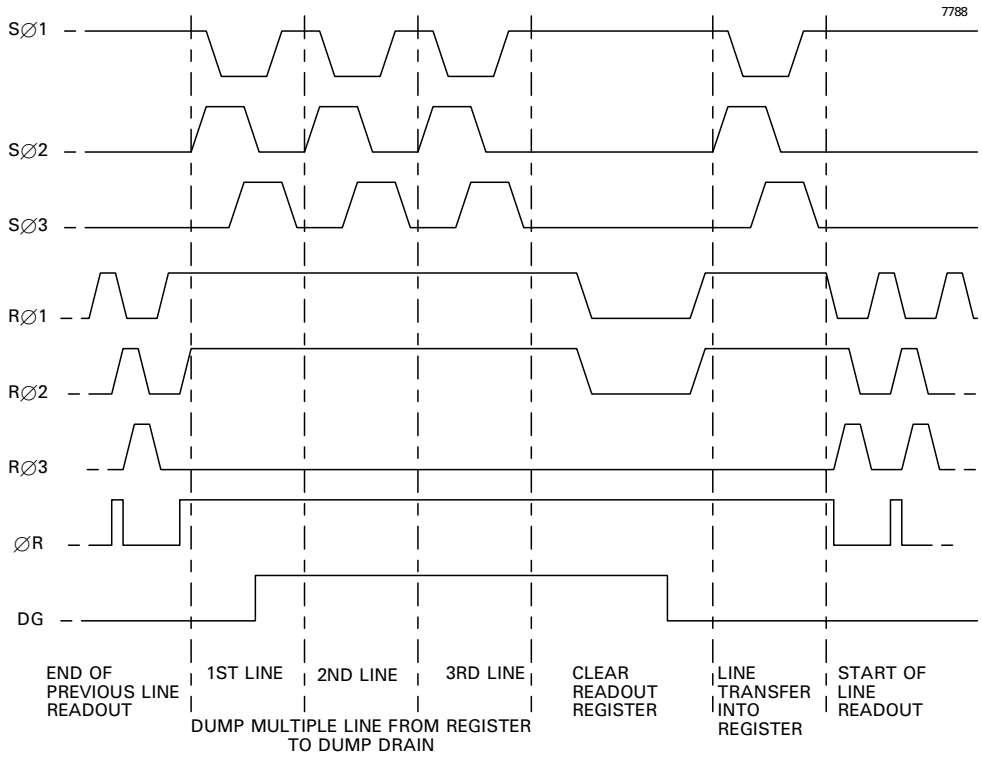
(For output from a single amplifier)



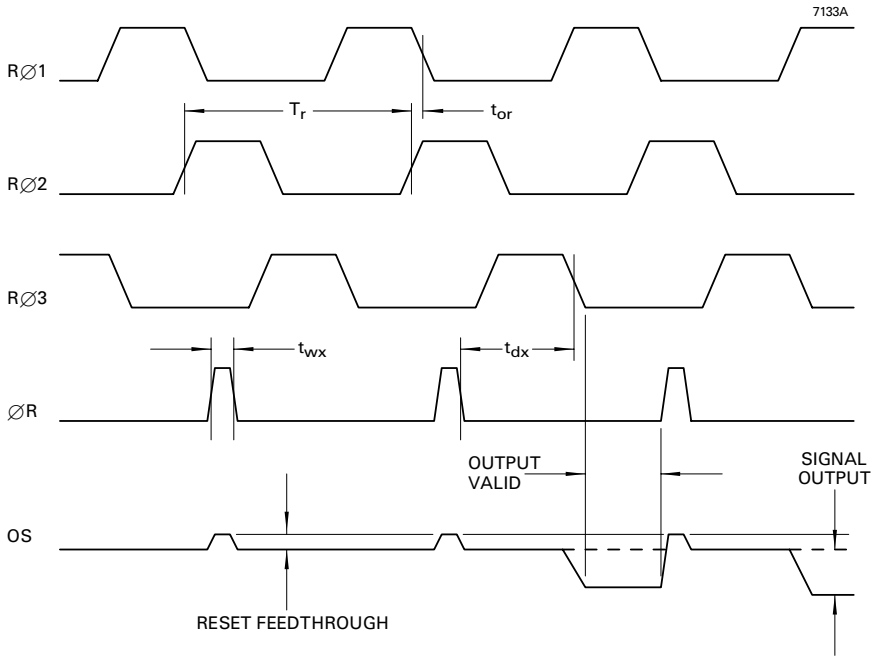
DETAIL OF VERTICAL LINE TRANSFER (Single line dump)



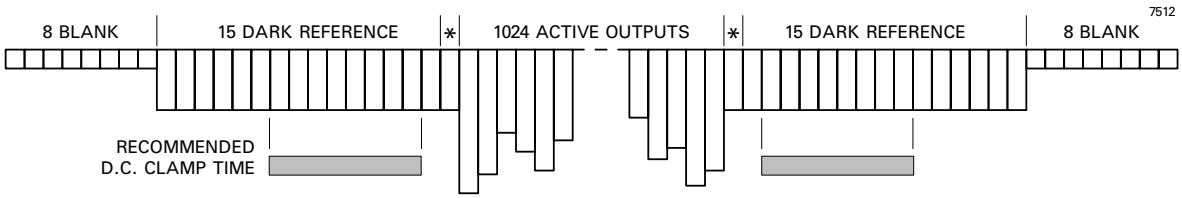
DETAIL OF VERTICAL LINE TRANSFER (Multiple line dump)



DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



* = Partially shielded transition elements

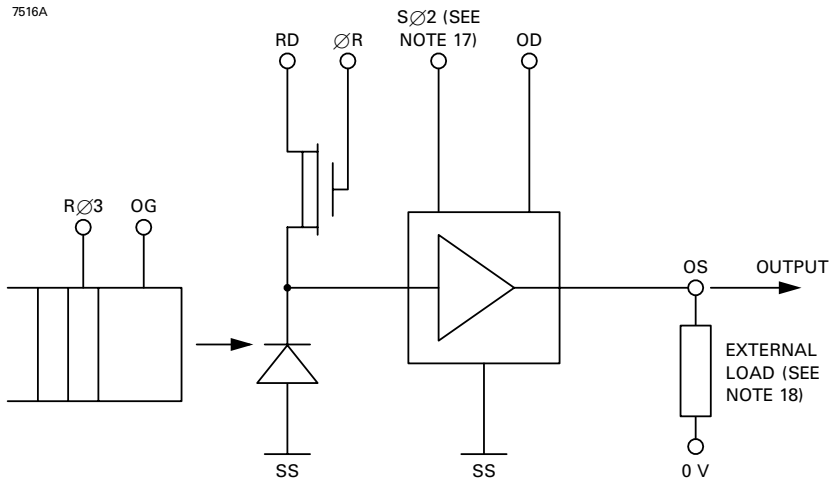
CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typical	Max	
T_i	Image clock period	2	5	see note 15	µs
t_{wi}	Image clock pulse width	1	2.5	see note 15	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	0.1	0.5	$0.2T_i$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	0.5	$0.2T_i$	µs
t_{oi}	Image clock pulse overlap	$(t_{ri}+t_{fi})/2$	0.5	$0.2T_i$	µs
t_{dir}	Delay time, SØ stop to RØ start	1	2	see note 15	µs
t_{dri}	Delay time, RØ stop to SØ start	1	1	see note 15	µs
T_r	Output register clock cycle period	200	1000	see note 15	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.3T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	$0.2t_{wx}$	$0.5t_{rr}$	$0.1T_r$	ns
t_{dx}	Delay time, ØR low to RØ3 low	30	$0.5T_r$	$0.8T_r$	ns

NOTES

15. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.
16. To minimise dark current, two of the IØ clocks should be held low during integration. IØ timing requirements are identical to SØ (as shown above).

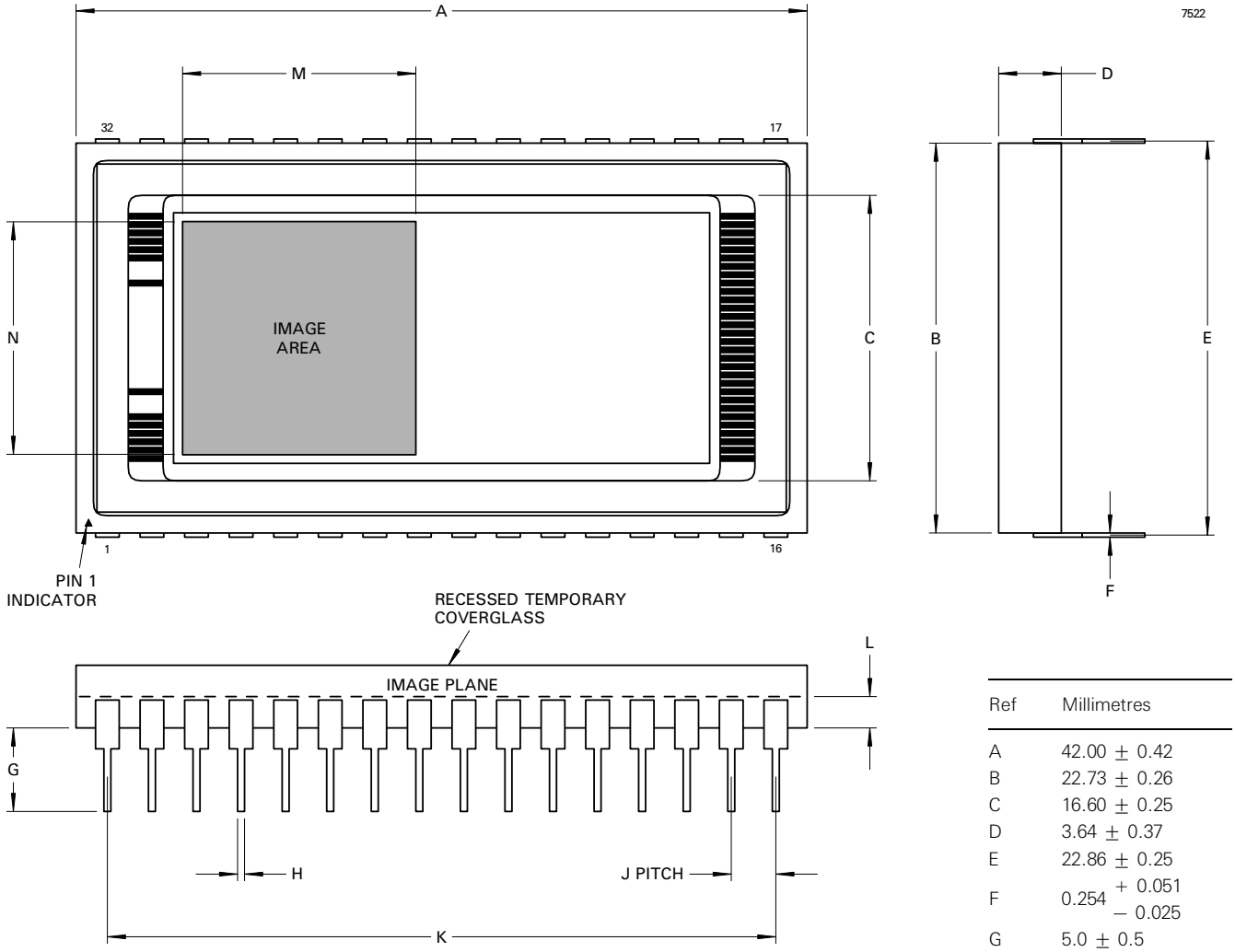
OUTPUT CIRCUIT



NOTES

17. The amplifier has a DC restoration circuit which is internally activated whenever S∅2 is high.
18. Not critical; can be a 2 to 5 mA constant current supply or an appropriate load resistor.

OUTLINE
(All dimensions without limits are nominal)



Ref	Millimetres
A	42.00 ± 0.42
B	22.73 ± 0.26
C	16.60 ± 0.25
D	3.64 ± 0.37
E	22.86 ± 0.25
F	$0.254^{+\ 0.051}_{-\ 0.025}$
G	5.0 ± 0.5
H	0.457 ± 0.051
J	2.54 ± 0.13
K	38.1
L	1.65 ± 0.50
M	13.3
N	13.3

ORDERING INFORMATION

Options include:

- Temporary Quartz Window
- Permanent Quartz Window
- Temporary Glass Window
- Permanent Glass Window
- Fibre-optic Coupling
- UV Coating
- X-ray Phosphor Coating

For further information on the performance of these and other options, please contact e2v technologies.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:-

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (pins 3, 4, 5, 7, 13, 14, 15, 16, 17, 18, 19, 20, 26, 28, 29, 30, 31) but not to the other pins.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising dose of greater than 10^4 rads.

Certain characterisation data are held at e2v technologies. Users planning to use CCDs in a high radiation environment are advised to contact e2v technologies.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	73	–	373	K
Operating	73	243	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling . . . . 5 K/min