CD-RW Laser Diode Current Driver

Features

- **Single +5V supply**
- **Laser diode read current driver**
- **Laser diode write current driver**
- **Laser diode Erase current driver**
- **Deltap circuit to control write current**
- **FSA circuit to integrate photo diode current**
- **Cagain circuit to convert V_{cagain} into current**
- **Dalpha circuit to perform voltage subtraction and limiting**
- **3-wire interface to control internal DAC**
- **A build-in OP-AMP**
- **48-pin SSOP package**

Applications

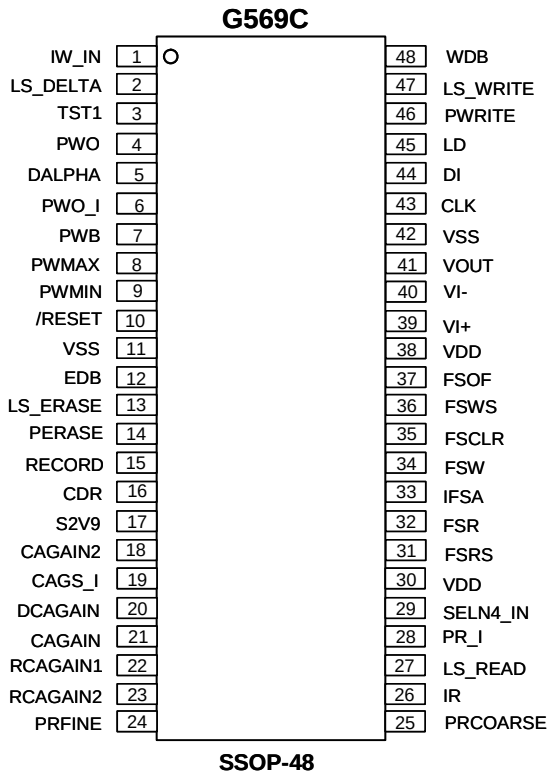
- **CD-RW Drive**

General Description

The G569C is a single chip solution for the various functions relating to laser diode operation in a CD-RW drive. The G569C integrates nine functional blocks in one chip. It has five voltage-to-current converters, one current-to-voltage converters which is called FSA, one OP-AMP, one eight-channels D/A converter, and one voltage subtracter with output clamping capability called Dalpha.

Three of the five V-to-I converters provide the laser diode currents for Read, Write, and Erase operations, respectively; another one of the V-I converters provides the Cagain current; and the other one provides Deltap current which can selectively shunt a certain amount of laser diode current for write operation. For the Write and Erase operations, the voltage to current conversion ratio can be adjusted using an external or internal DAC resistor array. The FSA circuit performs integration on the output current of an external photo diode, and sample-and-hold the peak voltage. It is used to monitor the laser diode power. The internal eight-channel D/A converter is used to provide the input voltage for above functional blocks. The G569C is available in a 48-pin SSOP surface-mount package.

Pin configuration



SSOP-48

Ordering Information

ORDER NUMBER	ORDER NUMBER (Pb free)	TEMP. RANGE	PACKAGE
G569CS8U	G569CS8Uf	0°C to 85°C	SSOP-48

Note: S8: SSOP-48
U: Tape & Reel

Absolute Maximum Ratings

V_{CC} to GND……..-0.3V to +6V
Dalpha to GND……...-3V to +6V
All other pin to GND……-0.3V to +6V
ESD protetion (human body model)……2000V
Continuous power dissipation (T_A=70°C), derate .7mW/°C about 70°C)…… 695mW
Operating Temperature…….-10°C to +100°C
Junction Temperature……..……+150°C
Storage temperature Range……-65°C to +165°C
Reflow Temperature (soldering, 10sec)……..+260°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply voltage	V_{DD}	4.75	5	5.5	V
High-level input voltage	V_{IH}	2			V
Low-level input voltage	V_{IL}			0.8	V
Operating free-air temperature	T_A	0		70	°C

Electrical Characteristics (V_{CC} = 5V, T_A = 0°C to +70°C, unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltage range		4.75	5.0	5.5	V
PWO output voltage		0		V_{S2V9}	V
Dalpha input voltage		-3.0		3.5	V
PWO_I input voltage		0		1.5	V
PWB output voltage		0		V_{S2V9}	V
PWMAX output voltage		0		V_{S2V9}	V
PWMIN output voltage		0		V_{S2V9}	V
IE output current		0		130	mA
S2V9 input voltage	V_{S2V9}		2.9		V
Cagain output current		0		1.2	mA
PRFine output voltage		0		V_{S2V9}	V
PRCoarse output voltage		0		V_{S2V9}	V
IR output current		0		160	mA
PR_I input voltage		0		2.16	V
FSR output voltage		0		3.0	V
FSW output voltage		0		3.0	V
VI- input voltage		0		3.5	V
VI+ input voltage		0		3.5	V
IW output current		0		160	mA
Operation current			41		mA

Pin Description

PIN NO.	PIN NAME	I/O	PIN FUNCTION
1	IW_IN	I	A diode of type BAS216 should be connected between this pin and node IW. This pin provides the path for sinking IW current.
2	LS_DELTA	O	Connect a 10Ω resistor from this pin to VSS
3	TST1	I	Test pin. Connect to ground for normal operation.
4	PWO	O	DAC output, connect to PWO_I through a resistor divider
5	DALPHA	I	Control voltage input
6	PWO_I	I	Control voltage input
7	PWB	O	Voltage output
8	PWMAX	O	Voltage output
9	PWMIN	O	Voltage output
10	/RESET	I	Logic input. A Low on this pin reset all DAC latches to 0.
11,42	VSS	I	Ground pin
12	EDB	O	Connect to the base node of external PNP BJT (Type BC808).
13	LS_ERASE	I	Connect a 6.8Ω (1206 type) resistor from this pin to V_{DD}
14	PERASE	O	Connect a DAC resistor array from this pin to VSS
15	RECORD	I	Logic input, a high indicates in recording mode.
16	CDR	I	Logic input, a high indicates in CD-R mode.
17	S2V9	I	Voltage input. Contribute to current output on CAGAIN pin and provides internal DAC reference voltage.
18	CAGAIN2	O	Tristate output. Connect 62KΩ to pin CAGAIN.
19	CAGS_I	I	Logic input, 0~2V swing.
20	DCAGAIN	O	An optional resistor may be added to modify the output current on CAGAIN
21	CAGAIN	O	Current output
22	RCAGAIN1	O	A 16.2KΩ resistor should be connected from this pin to VSS
23	RCAGAIN2	O	A 3.9KΩ resistor should be connected from this pin to VSS
24	PRFINE	O	DAC output, connect to PR_I through a resistor divider
25	PRCOARSE	O	DAC output, connect to PR_I through a resistor divider
26	IR	O	Read current output for laser diode
27	LS_READ	I	Connect two 22Ω (1206 type) resistors from this pin to V_{DD}
28	PR_I	I	Voltage input which controls the current on IR pin
29	SELN4_IN	I	Logic input. This pin can be shorted to pin CDR or be connected to the voltage divider formed by CDR and SELN4.
30,38	VDD	I	Supply voltage input. Each V_{DD} pin should have a 0.1µF bypass capacitor to VSS.
31	FSRS	I	Logic input, when FSRS=1, the voltage on pin FSCLR is sampled onto pin FSR, else FSR is in hold mode.
32	FSR	O	Sampled voltage output, controlled by FSRS
33	IFSA	I	If internal integration control circuitry is used, connect a photo diode from this pin to +30V. connect it to VDD otherwise
34	FSW	O	Sampled voltage output, controlled by FSWS
35	FSCLR	O	Sampling capacitors and resistor are connected to this pin.
36	FSWS	I	Logic input, when FSWS=1, the voltage on pin FSCLR is sampled onto pin FSW, else FSW is in hold mode.
37	FSOF	I	If internal integration control circuitry is used, connect the control signal to this pin. A logic low enable the current charging on the capacitors on pin FSCLR with the current from IFSA. Connect this pin to VDD if internal integration control circuitry is not used.
39	V_{I+}	I	Non-inverting input of Op Amp
40	V_{I-}	I	Inverting input of Op Amp
41	VOUT	O	Op Amp output
43	CLK	I	Clock input of I^2S bus
44	DI	I	Data input of I^2S bus
45	LD	I	Latch data input of I^2S bus
46	PWRITE	O	Connect a DAC resistor network from this pin to VSS
47	LS_WRITE	I	Connect a 6.8Ω (1206type) from this pin to V_{DD}
48	WDB	O	Connect to the base node of external PNP BJT. (Type BC807-40)

Detail Description

The typical application circuit of G569C is shown in Fig. 1. The block diagram of G569C is shown in Fig. 2. It contains nine circuit blocks. The operation of these blocks is described below.

READ Block

This block is equivalent to an operational transconductance amplifier (OTA). The voltage on PR_I pin is the input voltage, V_{PR_I}; the output current, IR, is delivered on pin IR. The relationship between V_{PR_I} and IR is given by:

$IR = 820 \times V_{PR\_I} / (R232 \parallel R233)$

where IR is in mA, V_{PR_I} is in volt, and R is in Ω. The recommended values for R232 and R233 are 22Ω, the maximum V_{PR_I} is 2.16 V, thus the maximum IR is 160mA. Since IR must flow through the two external 22Ω resistors connected between VDD and LS_READ pin, type 1206 SMD resistors must be used to handle the power dissipation.

ERASE Block

This block is also equivalent to an operational transconductance amplifier (OTA). The voltage on PWD node is the input voltage, V_{PWD}; the output voltage, V_{EDB}, can be used to drive an external PNP BJT to provides desired IE current. The relationship between V_{PWD} and IE is given by:

$$I_E = \frac{1800}{R_{235}} \times V_{PWD} / R_{PERASE},$$

where IE is in mA, V_{PWD} is in volt, and R_{PERASE}, in KΩ, is the total resistance from pin PEARSE to ground. Typically, a digital-to-analog converter (DAC) resistor array is connected at PERASE pin to allow digital programming of the OTA's transconductance. The maximum RPERASE is 7.5KΩ. An internal DAC can be enabled through I^2S bus to replace the external DAC resistor array. The maximum IE is 130 mA. Since IE must flow through the external 6.8Ω resistors connected between VDD and LS_ERASE pin, type 1206 SMD resistors must be used to handle the power dissipation.

WRITE Block

This block is also an operational transconductance amplifier (OTA). The voltage on PWD node is the input voltage, V_{PWD}; the output voltage, V_{WDB}, can be used to drive an external PNP BJT to provides desired IW current. The relationship between V_{PWD} and IW is given by:

$$I_W = \frac{1800}{R_{234}} \times V_{PWD} / R_{PWRITE},$$

where IW is in mA, V_{PWD} is in volt, and R_{PWRITE}, in KΩ is the total resistance from pin PWRITE to ground. Typically, a digital-to-analog converter (DAC) resistor array is connected at PWRITE pin to allow digital programming of the OTA's transconductance. An internal DAC can be enabled through I^2S bus to replace the external DAC resistor array. The maximum RPWRITE is 7.5KΩ. The maximum IW is 130 mA. Since IW must flow through the external 6.8Ω resistors connected between VDD and LS_WRITE pin, type 1206 SMD resistors must be used to handle the power dissipation.

DELTAP Block

This block is a current sink used to selectively sink the IW current. When DP4 is low, the current sink reduces the output current on IW by the amount of the magnitude of the current sink. The magnitude of the current sink, Is, is given by:

$$Is = \frac{3}{20} \times V_{DELTAP} / R_{LS\_DELTA},$$

where Is is in mA; V_{DELTAP}, in volt, is an internal DAC output; and R_{LS_DELTA}, in KΩ, is the resistance from pin LS_DELTA to ground. Type 1206 SMD resistors must be used for R_{LS_DELTA} to handle the power dissipation. When DP4 is high, the current output on IW current is not affected.

DALPHA Block

The function of this block is a voltage subtracter. The voltage on pin PWB, V_{PWB}, is given by:

$V_{PWB} = 2 \times V_{PWO\_I} - V_{DALPHA},$

where V_{PWO_I} and V_{DALPHA} are the voltages on pins PWO_I and DALPHA, respectively. In addition, the magnitude of the output voltage V_{PWB} is limited by V_{PWMAX} and V_{PWMIN}, which are the voltages on pins PWMAX and PWMIN.

When $2xV_{PWO\_I} - V_{DALPHA} < V_{PWMIN}$, then $V_{PWB} = V_{PWMIN}$.

When $2xV_{PWO\_I} - V_{DALPHA}, > V_{PWMAX}$, then $V_{PWB} = V_{PWMAX}$.

The input voltage ranges of V_{PWMAX} and V_{PWMIN} are 0 to V_{S2V9} which is the voltage input at S2V9 pin, and the condition $V_{PWMAX} > V_{PWMIN}$ must hold. Note that the input voltage range of V_{DALPHA} is -3V to +3.5V.

CAGAIN Block

This block is also an operational transconductance amplifier (OTA). The voltage on VCAGAIN pin is the input voltage, $V_{VCAGAIN}$; the output current, I_{CAGAIN}, is delivered on pin CAGAIN. Let the voltages on pins CDR, CAGS, CAGAIN and S2V9 be denoted as V_{CDR}, V_{CAGS}, V_{CAGAIN}, V_{S2V9}, respectively. The relationship between $V_{VCAGAIN}$ and I_{CAGAIN} is given by:

When $V_{CDR} = 5V$, $V_{CAGS} = 5V$
$I_{CAGAIN} = 1.2 \times V_{CAGAIN} / (R108 \parallel R109) + (V_{S2V9} - V_{CAGAIN}) / R195,$

When $V_{CDR} = 5V$, $V_{CAGS} = 0V$
$I_{CAGAIN} = (V_{S2V9} - V_{CAGAIN}) / R195$

When V_{CDR} = 0V, V_{CAGS} = 5V, V_{RECORD} = 0V
I_{CAGAIN} = 1.2 x V_{CAGAIN} / R108 + (V_{S2V9} - V_{CAGAIN}) / R195,

When V_{CDR} = 0V, V_{CAGS} = 5V, V_{RECORD} = 5V
I_{CAGAIN} = 1.2 x V_{CAGAIN} / R108

When V_{CDR} = 0V, V_{CAGS} = 0V, V_{RECORD} = 0V
I_{CAGAIN} = (V_{S2V9} - V_{CAGAIN}) / R195,

When V_{CDR} = 0V, V_{CAGS} = 0V, V_{RECORD} = 5V
I_{CAGAIN} = 0 mA,

Where I_{CAGAIN} is in mA; all voltages are in volt, and all resistance are in KΩ.

FSA Block

The FSOF/FSON control the integration of the photodiode current, I_{FSA}, on the capacitors connected on pin FSCLR to obtain a voltage. The voltage on FSCLR pin is connected to two sample-and-hold circuit. The voltages sampled by the control voltage on FSWS and FSRS pins are output on FSW and FSR pins, respectively. Namely,

When V_{FSWS} = 5V, V_{FSW} = V_{FSCLR},

When V_{FSWS} = 0V, V_{FSW} = the previously sampled value;

When V_{FSRS} = 5V, V_{FSR} = V_{FSCLR},

When V_{FSRS} = 0V, V_{FSR} = the previously sampled value.

The charging of FSCLR node is controlled by signals V_{FSOF} and V_{FSON}.

When V_{FSOF} = 0V, the FSCLR pin is charged by I_{FSA}.

When V_{FSOF} = 5V, the FSCLR pin is not charged by I_{FSA}.

The FSCLR, RDGAIN1, RDGAIN2, and RDGAIN3 pins are driven by an open-drain buffer, i.e., the voltages on these pins are either 0V or Hi-Z. The capacitance values of the three capacitors connecting to the FSCLR may need to be changed if loader other than CDL4800 is used.

When V_{FSCLR} = 0V, the charges on the capacitors are discharged to 0V.

When V_{FSCLR} = Hi-Z, the charging of FSCLR node is allowed.

When $V_{RDGAIN1}$ = 0V, the V_{FSCLR} is given by:
V_{FSCLR} = I_{FSA} x R187.

When $V_{RDGAIN1}$ = Hi-Z, the charging of FSCLR node is allowed.

When $V_{RDGAIN2}$ = 0V, the capacitor C_{123} is in parallel with C_{116}.

When $V_{RDGAIN2}$ = Hi-Z, the capacitor C_{123} has no effect.

When $V_{RDGAIN3}$ = 0V, the capacitor C_{117} is in parallel with C_{116}.

When $V_{RDGAIN3}$ = Hi-Z, the capacitor C_{117} has no effect.

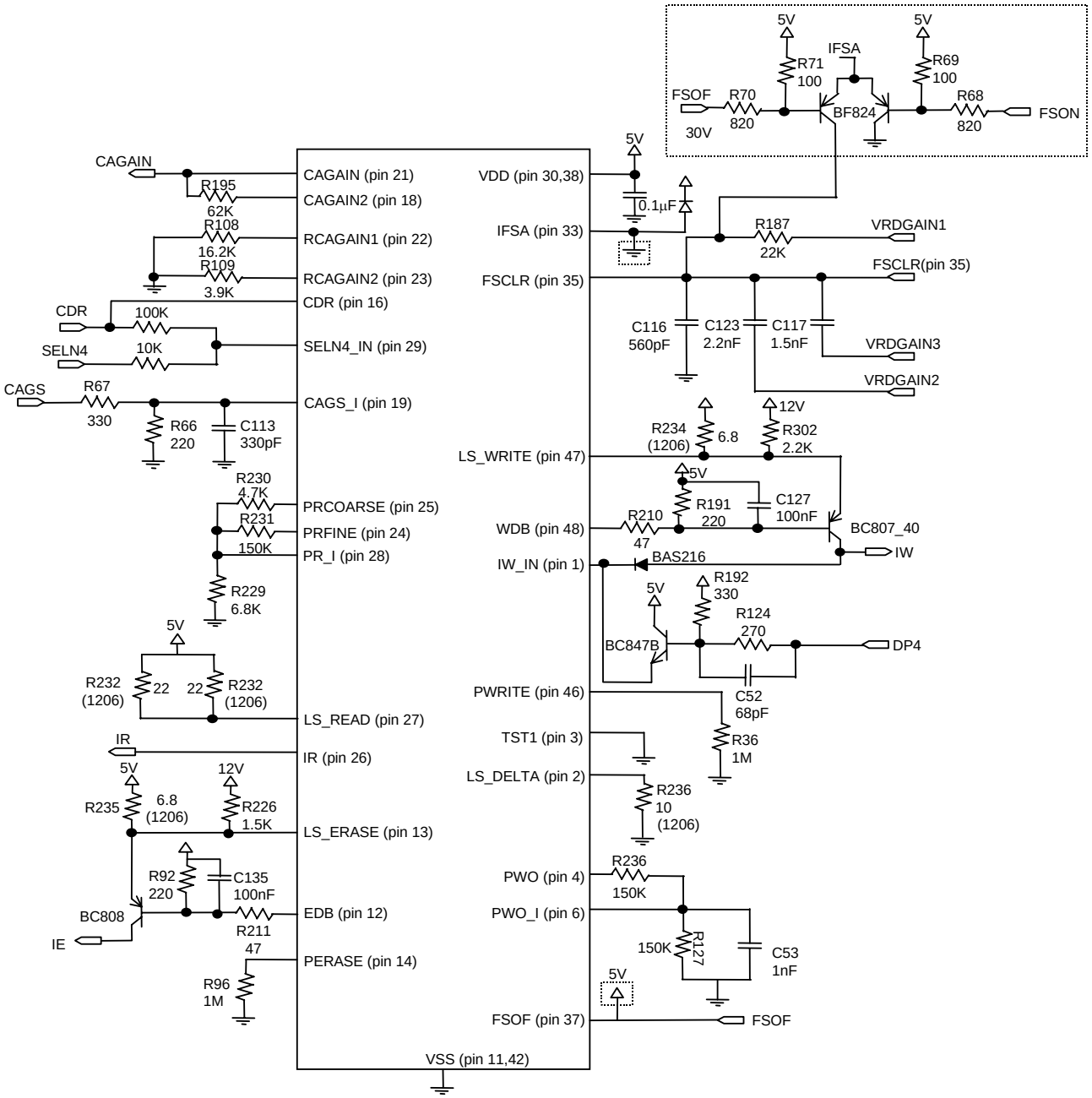


Fig 1. Typical application circuit

Note: The circuits in the dotted-line are the suggested circuit when internal integration circuit is not used. Please refer to pin description for details.

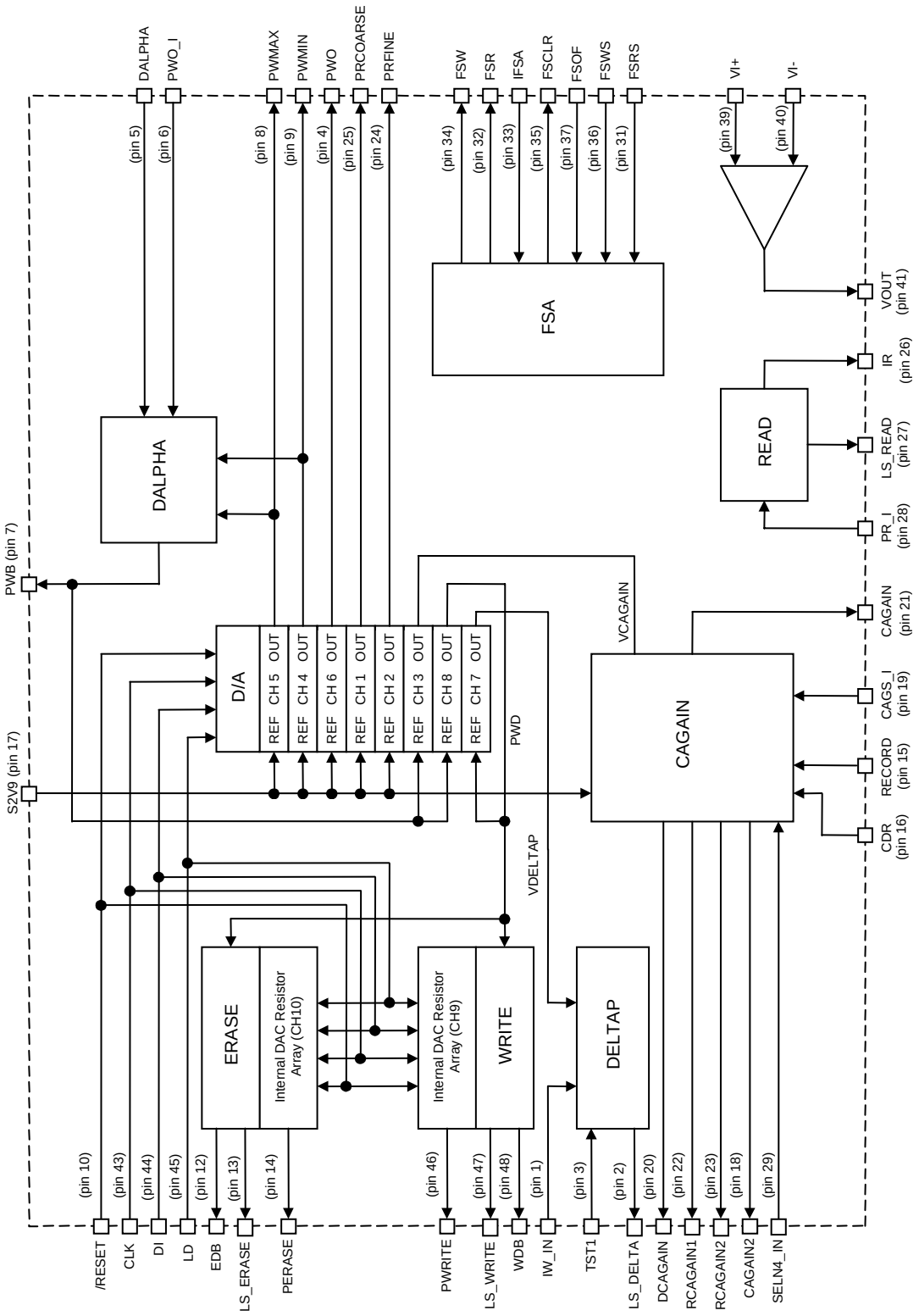
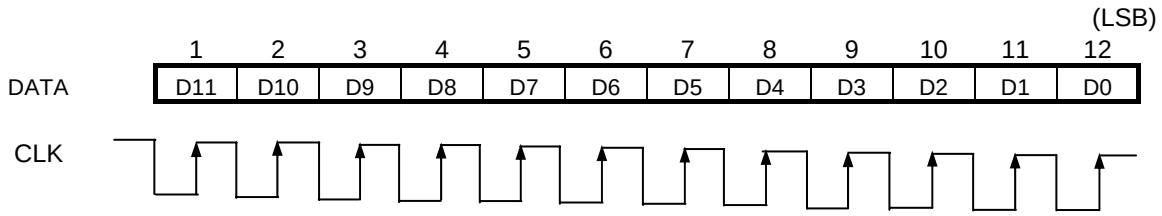


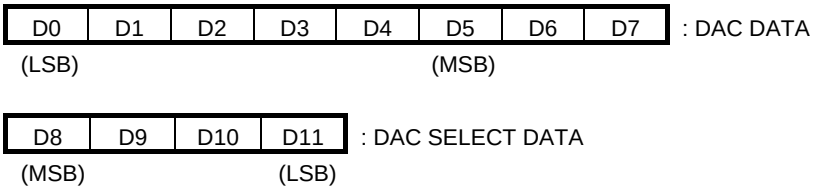
Fig 2. Block Diagram of G569C

Internal DAC Digital Format

12BIT SERIAL DATA



Data Assignment



DAC Select Data

D8	D9	D10	D11	DAC Selection
0	0	0	0	Don't Care
0	0	0	1	PRCOARSE Selection
0	0	1	0	PRFINE Selection
0	0	1	1	VCAGAIN Selection
0	1	0	0	PWMIN Selection
0	1	0	1	PWMAX Selection
0	1	1	0	PWO Selection
0	1	1	1	DELTAP Selection
1	0	0	0	PWD Selection
1	0	0	1	WRITE Selection
1	0	1	0	ERASE Selection
1	0	1	1	Don't Care
1	1	0	0	Don't Care
1	1	0	1	Don't Care
1	1	1	0	Don't Care
1	1	1	1	Don't Care

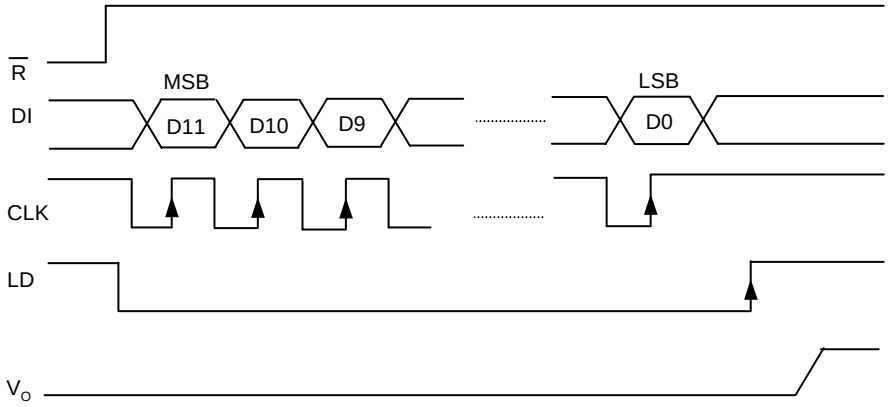
Digital Data Format for Internal DAC

D0	D1	D2	D3	D4	D5	D6	D7	DAC Output
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	V_{IN} / 256 × 1
0	1	0	0	0	0	0	0	V_{IN} / 256 × 2
1	1	0	0	0	0	0	0	V_{IN} / 256 × 3
¦	¦	¦	¦	¦	¦	¦	¦	¦
1	1	1	1	1	1	1	1	V_{IN} / 256 × 255

Digital Data Format for WRITE and ERASE

D0	D1	D2	D3	D4	D5	D6	D7	Comments
0	×	×	×	×	×	×	×	Disable Internal R2R Network
1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	Enable Internal R2R Network D1 is LSB , D7 is MSB

Timing Chart

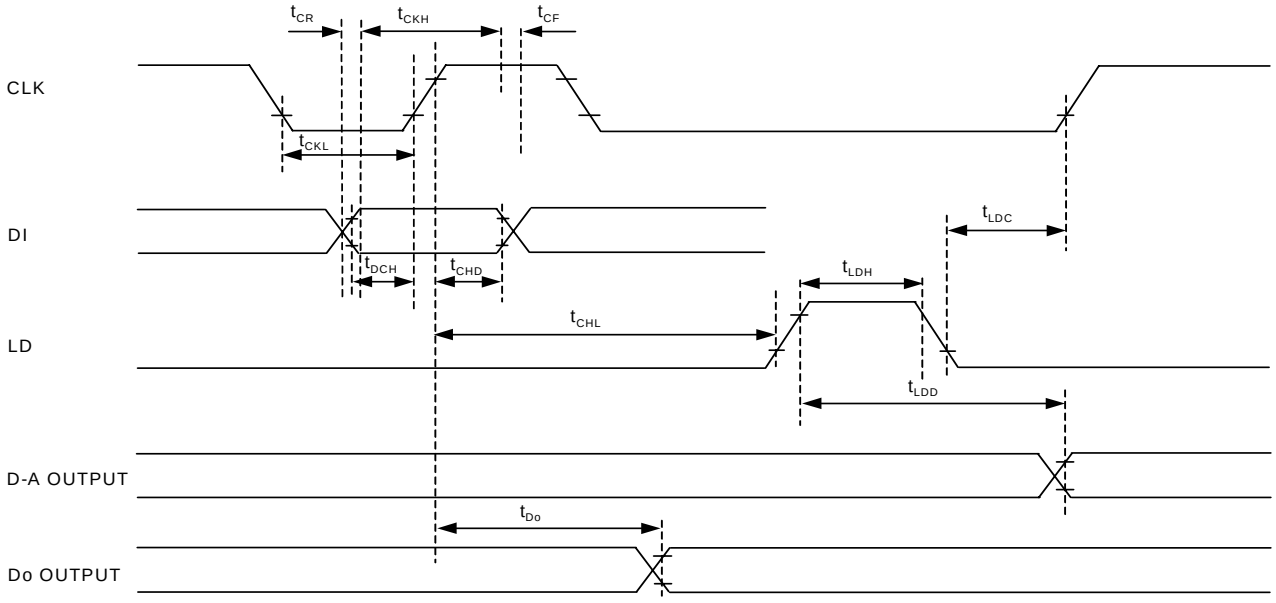


*Input data carried out LD signal Low besides CLK signal positive edge. CLK, LD is keep generally HIGH level.

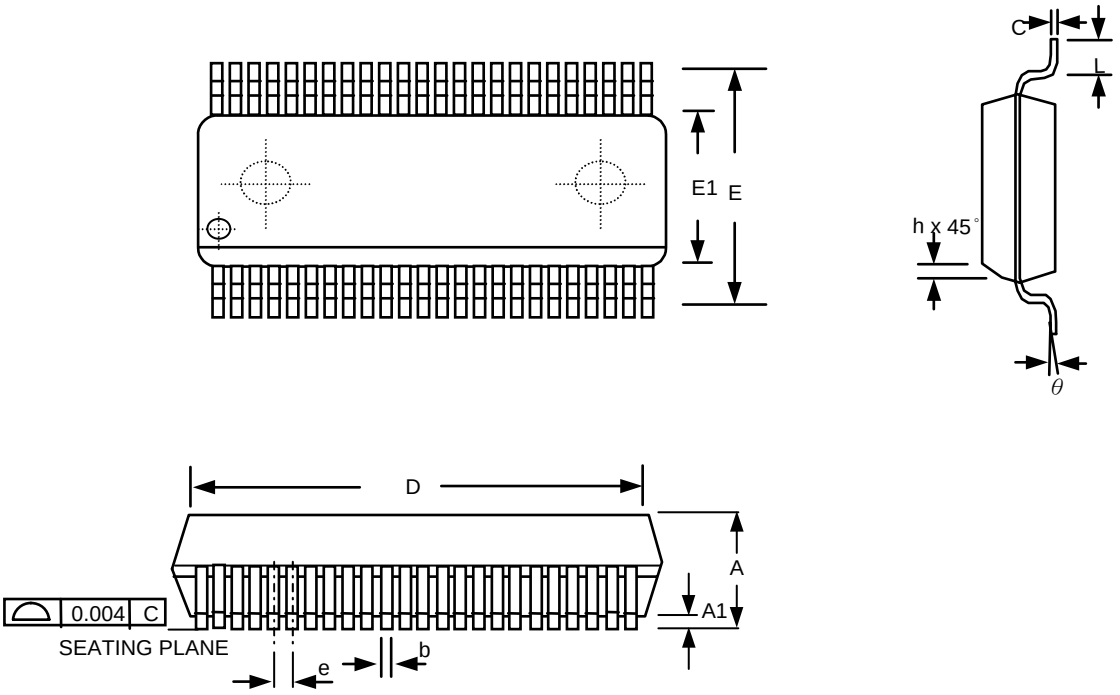
AC Characteristics

Symbol	Parameter	Measurement Condition	Limit			Unit
t_{CKL}	Clock "L" Pulse Width		200			nS
t_{CKH}	Clock "H" Pulse Width		200			nS
t_{CR}	Clock Rise Time				200	nS
t_{CF}	Clock Fall Time					
t_{DCH}	Data Set Up Time		60			nS
t_{CHD}	Data Hold Time		100			nS
t_{CHL}	LD Set Up Time		200			nS
t_{LDC}	LD Hold Time		100			nS
t_{LDH}	LD "H" Pulse Duration Time		100			nS
t_{Do}	Data Output Delay Time	C_L=100pF	70		350	nS
t_{LDD}	D-A Output Setting Time	$C_L \leq$ 100pF,V_{AO}:0.1< = > 2.6V This Time Until The Output Becomes The final Value Of 1/2 LSB			300	µS

Timing Chart



Package Information



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.413	2.591	2.794	0.095	0.102	0.110
A1	0.203	0.305	0.406	0.008	0.012	0.016
b	0.203		0.343	0.008		0.0135
c	0.127		0.254	0.005		0.010
D	15.75	15.88	16.00	0.620	0.625	0.630
e	0.635 BASIC			0.025 BASIC		
E	10.033		10.668	0.395		0.420
E1	7.391	7.493	7.595	0.291	0.295	0.289
h	0.381		0.635	0.015		0.025
L	0.508		1.016	1.020		0.040
θ	0		θ	0		θ

Package Description: SSOP-48

Quantity /Reel : 1000 / Reel
Reel Diameter : 13”
Carrier Tape (Width) : 32mm
Carrier Tape (Pitch) : 16mm

Mechanical Polarization

Top View Shown With Cover Tape Removed

EIA-JEDEC SO Package Outline Style