

165-Bump BGA  
Commercial Temp  
Industrial Temp

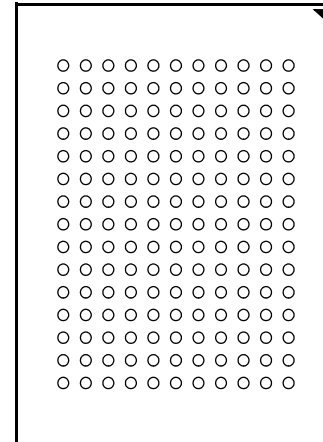


## 72Mb SigmaQuad-II Burst of 4 SRAM

333 MHz–167 MHz  
1.8 V V<sub>DD</sub>  
1.8 V and 1.5 V I/O

### Features

- Simultaneous Read and Write SigmaQuad™ Interface
- JEDEC-standard pinout and package
- Dual Double Data Rate interface
- Byte Write controls sampled at data-in time
- Burst of 4 Read and Write
- 1.8 V +100/-100 mV core power supply
- 1.5 V or 1.8 V HSTL Interface
- Pipelined read operation
- Fully coherent read and write pipelines
- ZQ pin for programmable output drive strength
- IEEE 1149.1 JTAG-compliant Boundary Scan
- Pin-compatible with present 9Mb, 18Mb, and 36Mb and future 144Mb devices
- 165-bump, 15 mm x 17 mm, 1 mm bump pitch BGA package
- RoHS-compliant 165-bump BGA package available



**Bottom View**  
**165-Bump, 15 mm x 17 mm BGA**  
**1 mm Bump Pitch, 11 x 15 Bump Array**

### SigmaQuad™ Family Overview

The GS8662D08/09/18/36E are built in compliance with the SigmaQuad-II SRAM pinout standard for Separate I/O synchronous SRAMs. They are 75,497,472-bit (72Mb) SRAMs. The GS8662D08/18/36E SigmaQuad SRAMs are just one element in a family of low power, low voltage HSTL I/O SRAMs designed to operate at the speeds needed to implement economical high performance networking systems.

### Clocking and Addressing Schemes

The GS8662D08/09/18/36E SigmaQuad-II SRAMs are synchronous devices. They employ two input register clock inputs, K and  $\bar{K}$ . K and  $\bar{K}$  are independent single-ended clock inputs, not differential inputs to a single differential clock input buffer. The device also allows the user to manipulate the output register clock inputs quasi independently with the C and

$\bar{C}$  clock inputs. C and  $\bar{C}$  are also independent single-ended clock inputs, not differential inputs. If the C clocks are tied high, the K clocks are routed internally to fire the output registers instead.

Because Separate I/O SigmaQuad-II B4 RAMs always transfer data in four packets, A0 and A1 are internally set to 0 for the first read or write transfer, and automatically incremented by 1 for the next transfers. Because the LSBs are tied off internally, the address field of a SigmaQuad-II B4 RAM is always two address pins less than the advertised index depth (e.g., the 4M x 18 has a 1024K addressable index).

### Parameter Synopsis

	- 333	-300	-250	-200	-167
tKHKH	3.0 ns	3.3 ns	4.0 ns	5.0 ns	6.0 ns
tKHQV	0.45 ns	0.45 ns	0.45 ns	0.45 ns	0.50 ns

**2M x 36 SigmaQuad-II SRAM—Top View**

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	MCL/SA (288Mb)	SA	$\overline{\text{W}}$	$\overline{\text{BW2}}$	$\overline{\text{K}}$	$\overline{\text{BW1}}$	$\overline{\text{R}}$	SA	MCL/SA (144Mb)	CQ
B	Q27	Q18	D18	SA	$\overline{\text{BW3}}$	K	$\overline{\text{BW0}}$	SA	D17	Q17	Q8
C	D27	Q28	D19	V <sub>SS</sub>	SA	NC	SA	V <sub>SS</sub>	D16	Q7	D8
D	D28	D20	Q19	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	Q16	D15	D7
E	Q29	D29	Q20	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	Q15	D6	Q6
F	Q30	Q21	D21	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	D14	Q14	Q5
G	D30	D22	Q22	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	Q13	D13	D5
H	$\overline{\text{Doff}}$	V <sub>REF</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>REF</sub>	ZQ
J	D31	Q31	D23	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	D12	Q4	D4
K	Q32	D32	Q23	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	Q12	D3	Q3
L	Q33	Q24	D24	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	D11	Q11	Q2
M	D33	Q34	D25	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	D10	Q1	D2
N	D34	D26	Q25	V <sub>SS</sub>	SA	SA	SA	V <sub>SS</sub>	Q10	D9	D1
P	Q35	D35	Q26	SA	SA	C	SA	SA	Q9	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{\text{C}}$	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—15 x 17 mm<sup>2</sup> Body—1 mm Bump Pitch

**Notes:**

1.  $\overline{\text{BW0}}$  controls writes to D0:D8;  $\overline{\text{BW1}}$  controls writes to D9:D17;  $\overline{\text{BW2}}$  controls writes to D18:D26;  $\overline{\text{BW3}}$  controls writes to D27:D35
2. MCL = Must Connect Low

**4M x 18 SigmaQuad-II SRAM—Top View**

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	MCL/SA (144Mb)	SA	$\overline{\text{W}}$	$\overline{\text{BW1}}$	$\overline{\text{K}}$	NC	$\overline{\text{R}}$	SA	SA	CQ
B	NC	Q9	D9	SA	NC	K	$\overline{\text{BW0}}$	SA	NC	NC	Q8
C	NC	NC	D10	$V_{SS}$	SA	NC	SA	$V_{SS}$	NC	Q7	D8
D	NC	D11	Q10	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	NC	NC	D7
E	NC	NC	Q11	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	NC	D6	Q6
F	NC	Q12	D12	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	Q5
G	NC	D13	Q13	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	NC	D5
H	$\overline{\text{Doff}}$	$V_{REF}$	$V_{DDQ}$	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	$V_{DDQ}$	$V_{REF}$	ZQ
J	NC	NC	D14	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	Q4	D4
K	NC	NC	Q14	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	D3	Q3
L	NC	Q15	D15	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	NC	NC	Q2
M	NC	NC	D16	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	NC	Q1	D2
N	NC	D17	Q16	$V_{SS}$	SA	SA	SA	$V_{SS}$	NC	NC	D1
P	NC	NC	Q17	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{\text{C}}$	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—15 x 17 mm<sup>2</sup> Body—1 mm Bump Pitch

**Notes:**

1.  $\overline{\text{BW0}}$  controls writes to D0:D8.  $\overline{\text{BW1}}$  controls writes to D9:D17.
2. MCL = Must Connect Low

**8M x 9 SigmaQuad-II SRAM—Top View**

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	SA	SA	$\overline{\text{W}}$	NC	$\overline{\text{K}}$	NC	$\overline{\text{R}}$	SA	SA	CQ
B	NC	NC	NC	SA	NC	K	$\overline{\text{BW0}}$	SA	NC	NC	Q4
C	NC	NC	NC	V <sub>SS</sub>	SA	NC	SA	V <sub>SS</sub>	NC	NC	D4
D	NC	D5	NC	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	NC	NC
E	NC	NC	Q5	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	D3	Q3
F	NC	NC	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	NC
G	NC	D6	Q6	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	NC
H	$\overline{\text{D}}_{\text{off}}$	V <sub>REF</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>REF</sub>	ZQ
J	NC	NC	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	Q2	D2
K	NC	NC	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	NC
L	NC	Q7	D7	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	NC	Q1
M	NC	NC	NC	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	NC	D1
N	NC	D8	NC	V <sub>SS</sub>	SA	SA	SA	V <sub>SS</sub>	NC	NC	NC
P	NC	NC	Q8	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{\text{C}}$	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—13 x 15 mm<sup>2</sup> Body—1 mm Bump Pitch

**Notes:**

1. BW0 controls writes to D0:D8.
2. MCL = Must Connect Low

### 8M x 8 SigmaQuad-II SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	SA	SA	$\overline{\text{W}}$	$\overline{\text{NW1}}$	$\overline{\text{K}}$	NC	$\overline{\text{R}}$	SA	SA	CQ
B	NC	NC	NC	SA	NC	K	$\overline{\text{NW0}}$	SA	NC	NC	Q3
C	NC	NC	NC	V <sub>SS</sub>	SA	NC	SA	V <sub>SS</sub>	NC	NC	D3
D	NC	D4	NC	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	NC	NC
E	NC	NC	Q4	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	D2	Q2
F	NC	NC	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	NC
G	NC	D5	Q5	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	NC
H	$\overline{\text{Doff}}$	V <sub>REF</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>REF</sub>	ZQ
J	NC	NC	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	Q1	D1
K	NC	NC	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	NC
L	NC	Q6	D6	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	NC	Q0
M	NC	NC	NC	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	NC	D0
N	NC	D7	NC	V <sub>SS</sub>	SA	SA	SA	V <sub>SS</sub>	NC	NC	NC
P	NC	NC	Q7	SA	SA	C	SA	SA	NC	NC	NC
R	TDO	TCK	SA	SA	SA	$\overline{\text{C}}$	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—15 x 17 mm<sup>2</sup> Body—1 mm Bump Pitch

**Notes:**

1.  $\overline{\text{NW0}}$  controls writes to D0:D3.  $\overline{\text{NW1}}$  controls writes to D4:D7.
2. MCL = Must Connect Low

### Pin Description Table

Symbol	Description	Type	Comments
SA	Synchronous Address Inputs	Input	—
NC	No Connect	—	—
$\overline{R}$	Synchronous Read	Input	Active Low
$\overline{W}$	Synchronous Write	Input	Active Low
$\overline{BW0} - \overline{BW3}$	Synchronous Byte Writes	Input	Active Low x9/x18/x36 only
$\overline{NW0} - \overline{NW1}$	Nybble Write Control Pin	Input	Active Low x8 only
K	Input Clock	Input	Active High
$\overline{K}$	Input Clock	Input	Active Low
C	Output Clock	Input	Active High
$\overline{C}$	Output Clock	Input	Active Low
TMS	Test Mode Select	Input	—
TDI	Test Data Input	Input	—
TCK	Test Clock Input	Input	—
TDO	Test Data Output	Output	—
V <sub>REF</sub>	HSTL Input Reference Voltage	Input	—
ZQ	Output Impedance Matching Input	Input	—
Qn	Synchronous Data Outputs	Output	
Dn	Synchronous Data Inputs	Input	
$\overline{D}_{off}$	Disable DLL when low	Input	Active Low
CQ	Output Echo Clock	Output	—
$\overline{CQ}$	Output Echo Clock	Output	—
V <sub>DD</sub>	Power Supply	Supply	1.8 V Nominal
V <sub>DDQ</sub>	Isolated Output Buffer Supply	Supply	1.5 or 1.8 V Nominal
V <sub>SS</sub>	Power Supply: Ground	Supply	—

**Note:**

NC = Not Connected to die or any other pin

## Background

Separate I/O SRAMs, from a system architecture point of view, are attractive in applications where alternating reads and writes are needed. Therefore, the SigmaQuad-II SRAM interface and truth table are optimized for alternating reads and writes. Separate I/O SRAMs are unpopular in applications where multiple reads or multiple writes are needed because burst read or write transfers from Separate I/O SRAMs can cut the RAM's bandwidth in half.

## Alternating Read-Write Operations

SigmaQuad-II SRAMs follow a few simple rules of operation.

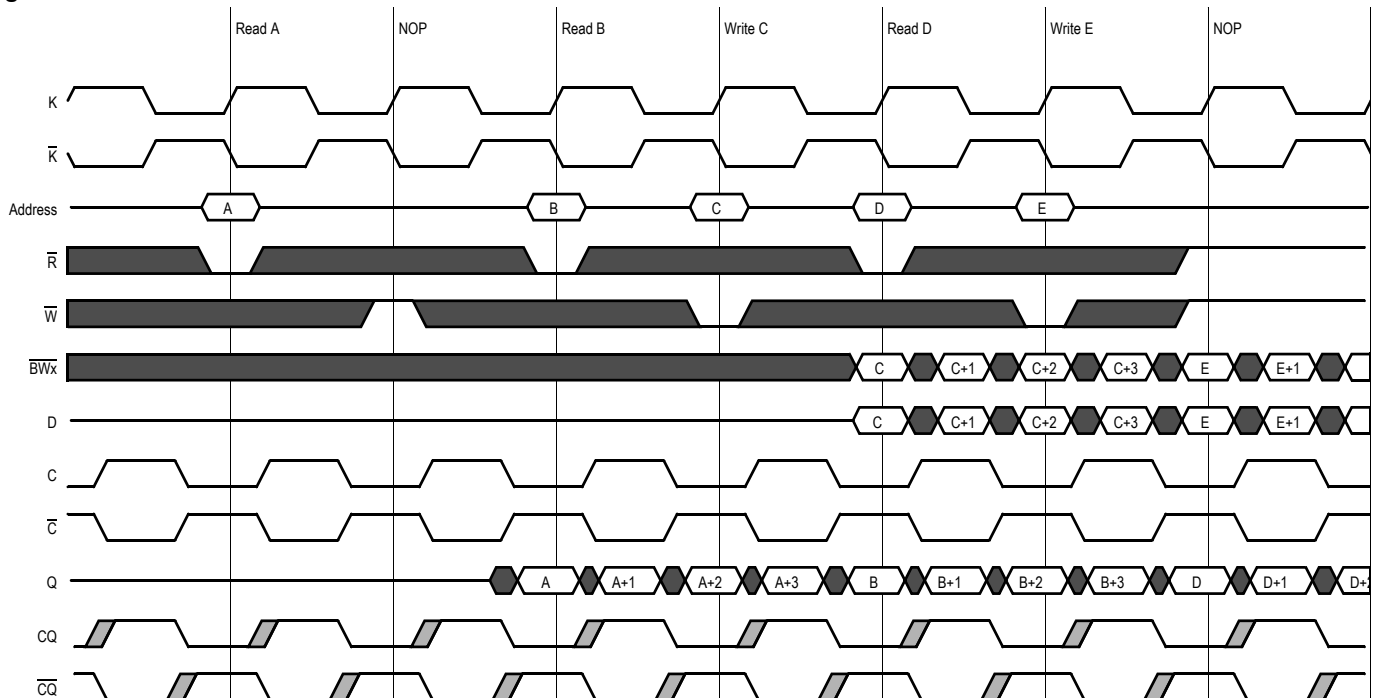
- Read or Write commands issued on one port are never allowed to interrupt an operation in progress on the other port.
- Read or Write data transfers in progress may not be interrupted and re-started.
- $\overline{R}$  and  $\overline{W}$  high always deselected the RAM.
- All address, data, and control inputs are sampled on clock edges.

In order to enforce these rules, each RAM combines present state information with command inputs. See the Truth Table for details.

### SigmaQuad-II B4 SRAM DDR Read

The status of the Address Input,  $\overline{W}$ , and  $\overline{R}$  pins are sampled by the rising edges of K.  $\overline{W}$  and  $\overline{R}$  high causes chip disable. A low on the Read Enable-bar pin,  $\overline{R}$ , begins a read cycle.  $\overline{R}$  is always ignored if the previous command loaded was a read command. Data can be clocked out after the next rising edge of K with a rising edge of  $\overline{C}$  (or by  $\overline{K}$  if C and  $\overline{C}$  are tied high), after the following rising edge of  $\overline{K}$  with a rising edge of C (or by K if C and  $\overline{C}$  are tied high), after the next rising edge of K with a rising edge of  $\overline{C}$ , and after the following rising edge of  $\overline{K}$  with a rising edge of C. Clocking in a high on the Read Enable-bar pin,  $\overline{R}$ , begins a read port deselect cycle.

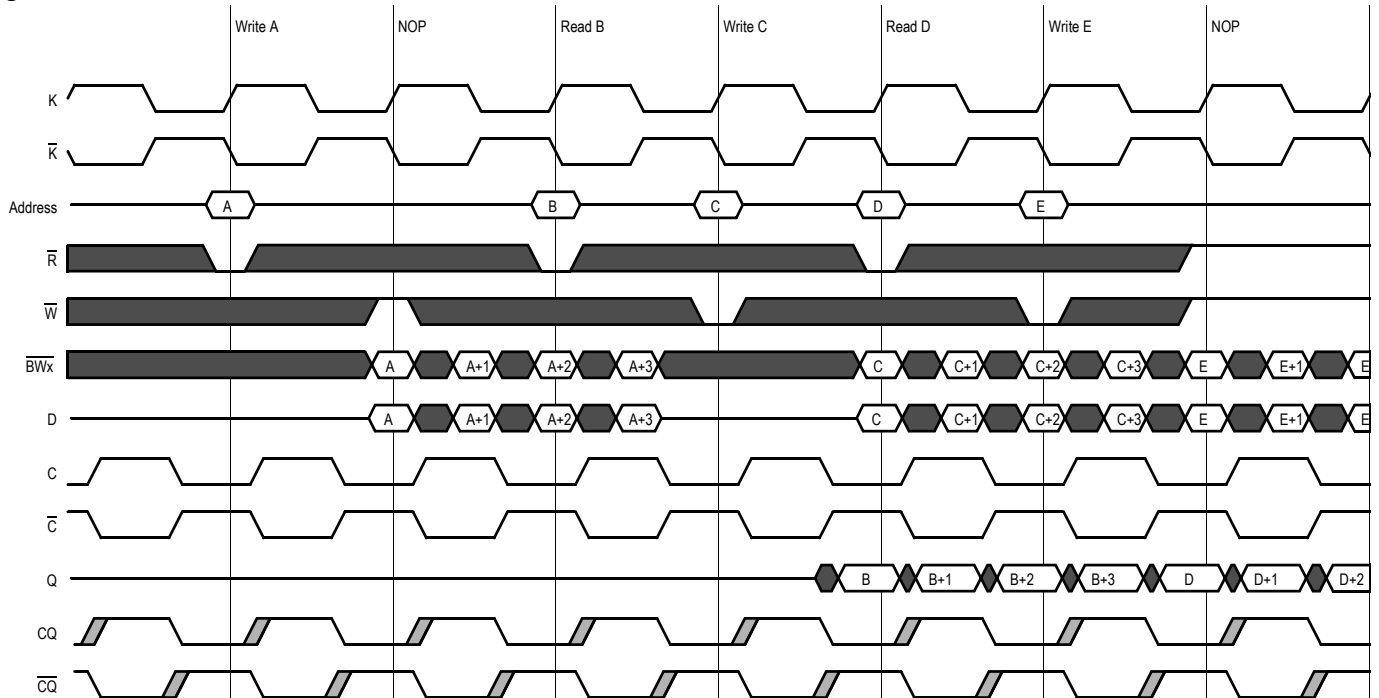
### SigmaQuad-II B4 Double Data Rate SRAM Read First



### SigmaQuad-II B4 SRAM DDR Write

The status of the Address Input,  $\overline{W}$ , and  $\overline{R}$  pins are sampled by the rising edges of K.  $\overline{W}$  and  $\overline{R}$  high causes chip disable. A low on the Write Enable-bar pin,  $\overline{W}$ , and a high on the Read Enable-bar pin,  $\overline{R}$ , begins a write cycle.  $\overline{W}$  is always ignored if the previous command was a write command. Data is clocked in by the next rising edge of K, the rising edge of  $\overline{K}$  after that, the next rising edge of K, and finally by the next rising edge of  $\overline{K}$ . and by the rising edge of the K that follows.

### SigmaQuad-II B4 Double Data Rate SRAM Write First





### Power-Up Sequence for SigmaQuad-II SRAMs

SigmaQuad-II SRAMs must be powered-up in a specific sequence in order to avoid undefined operations.

#### Power-Up Sequence

1. Power-up and maintain  $\overline{\text{Doff}}$  at low state.
  - 1a. Apply  $V_{DD}$ .
  - 1b. Apply  $V_{DDQ}$ .
  - 1c. Apply  $V_{REF}$  (may also be applied at the same time as  $V_{DDQ}$ ).
2. After power is achieved and clocks ( $K$ ,  $\overline{K}$ ,  $C$ ,  $\overline{C}$ ) are stabilized, change  $\overline{\text{Doff}}$  to high.
3. An additional 1024 clock cycles are required to lock the DLL after it has been enabled.

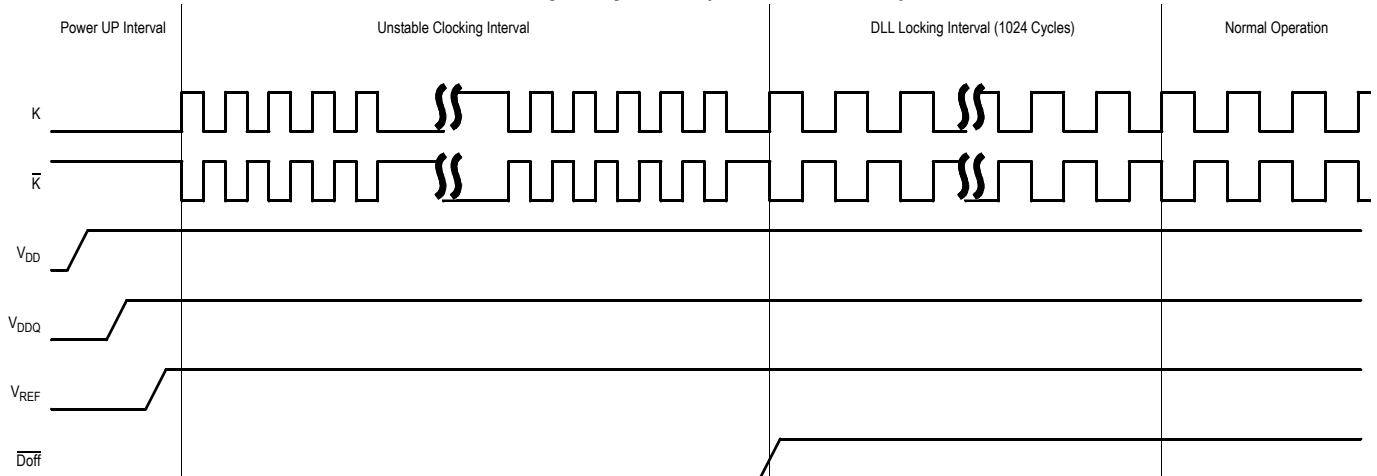
#### Note:

If you want to tie  $\overline{\text{Doff}}$  high with an unstable clock, you must stop the clock for a minimum of 30 seconds to reset the DLL after the clocks become stabilized.

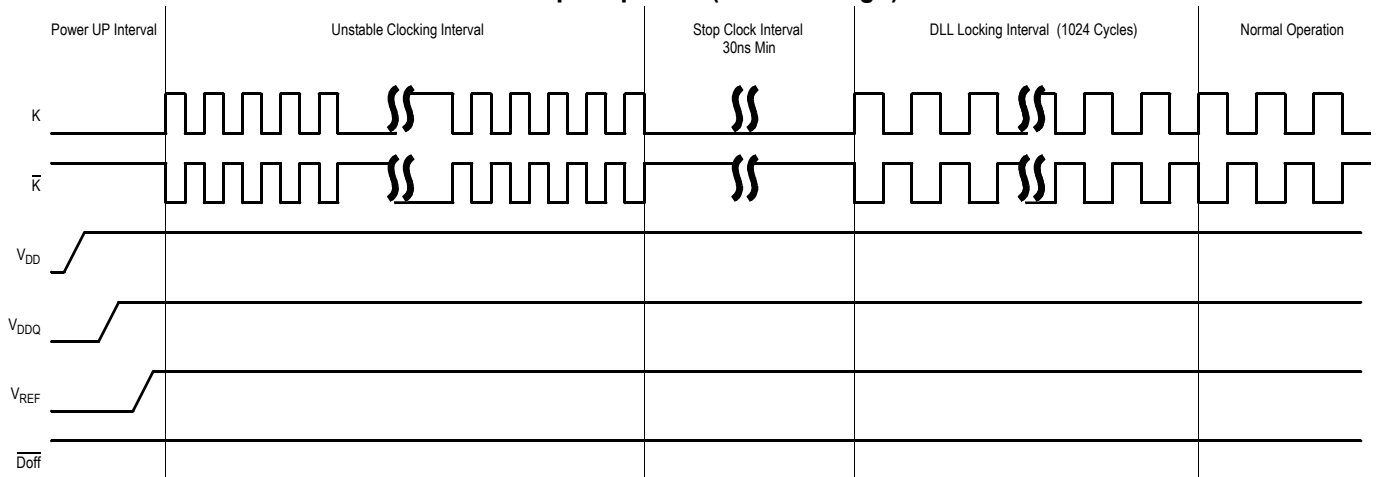
#### DLL Constraints

- The DLL synchronizes to either K or C clock. These clocks should have low phase jitter ( $t_{KCVar}$  on page 21).
- The DLL cannot operate at a frequency lower than 119 MHz.
- If the incoming clock is not stabilized when DLL is enabled, the DLL may lock on the wrong frequency and cause undefined errors or failures during the initial stage.

#### Power-Up Sequence ( $\overline{\text{Doff}}$ controlled)



#### Power-Up Sequence ( $\overline{\text{Doff}}$ tied High)



#### Note:

If the frequency is changed, DLL reset is required. After reset, a minimum of 1024 cycles is required for DLL lock.

## Special Functions

### Byte Write and Nybble Write Control

Byte Write Enable pins are sampled at the same time that Data In is sampled. A high on the Byte Write Enable pin associated with a particular byte (e.g.,  $\overline{BW0}$  controls D0–D8 inputs) will inhibit the storage of that particular byte, leaving whatever data may be stored at the current address at that byte location undisturbed. Any or all of the Byte Write Enable pins may be driven high or low during the data in sample times in a write sequence.

Each write enable command and write address loaded into the RAM provides the base address for a 4 beat data transfer. The x18 version of the RAM, for example, may write 72 bits in association with each address loaded. Any 9-bit byte may be masked in any write sequence.

Nybble Write (4-bit) control is implemented on the 8-bit-wide version of the device. For the x8 version of the device, “Nybble Write Enable” and “ $\overline{NBx}$ ” may be substituted in all the discussion above.

### Example x18 RAM Write Sequence using Byte Write Enables

Data In Sample Time	$\overline{BW0}$	$\overline{BW1}$	D0–D8	D9–D17
Beat 1	0	1	Data In	Don't Care
Beat 2	1	0	Don't Care	Data In
Beat 3	0	0	Data In	Data In
Beat 4	1	0	Don't Care	Data In

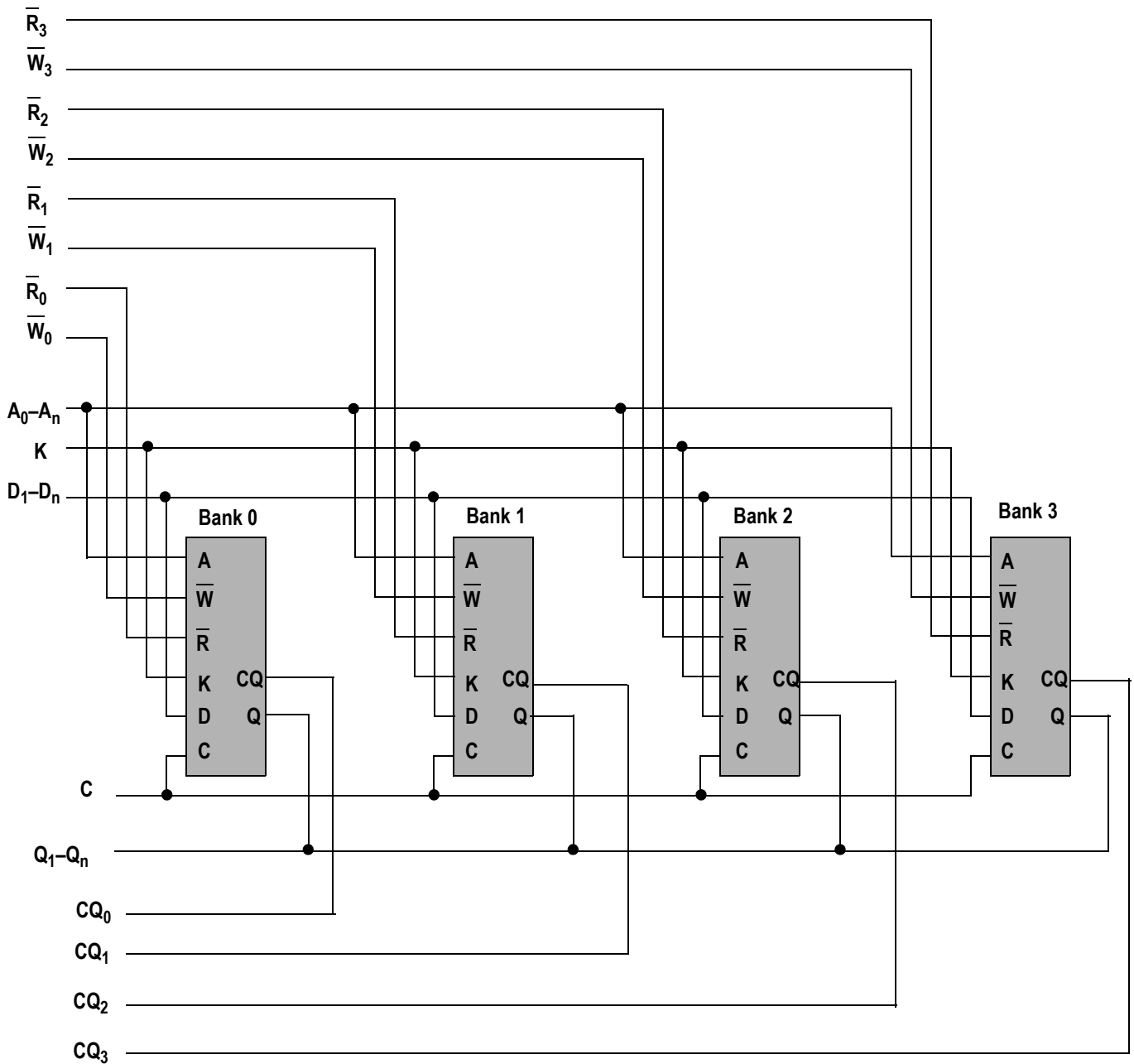
### Resulting Write Operation

Byte 1 D0–D8	Byte 2 D9–D17	Byte 1 D0–D8	Byte 2 D9–D17	Byte 1 D0–D8	Byte 2 D9–D17	Byte 1 D0–D8	Byte 2 D9–D17
Written	Unchanged	Unchanged	Written	Written	Written	Unchanged	Written
Beat 1		Beat 2		Beat 3		Beat 4	

### Output Register Control

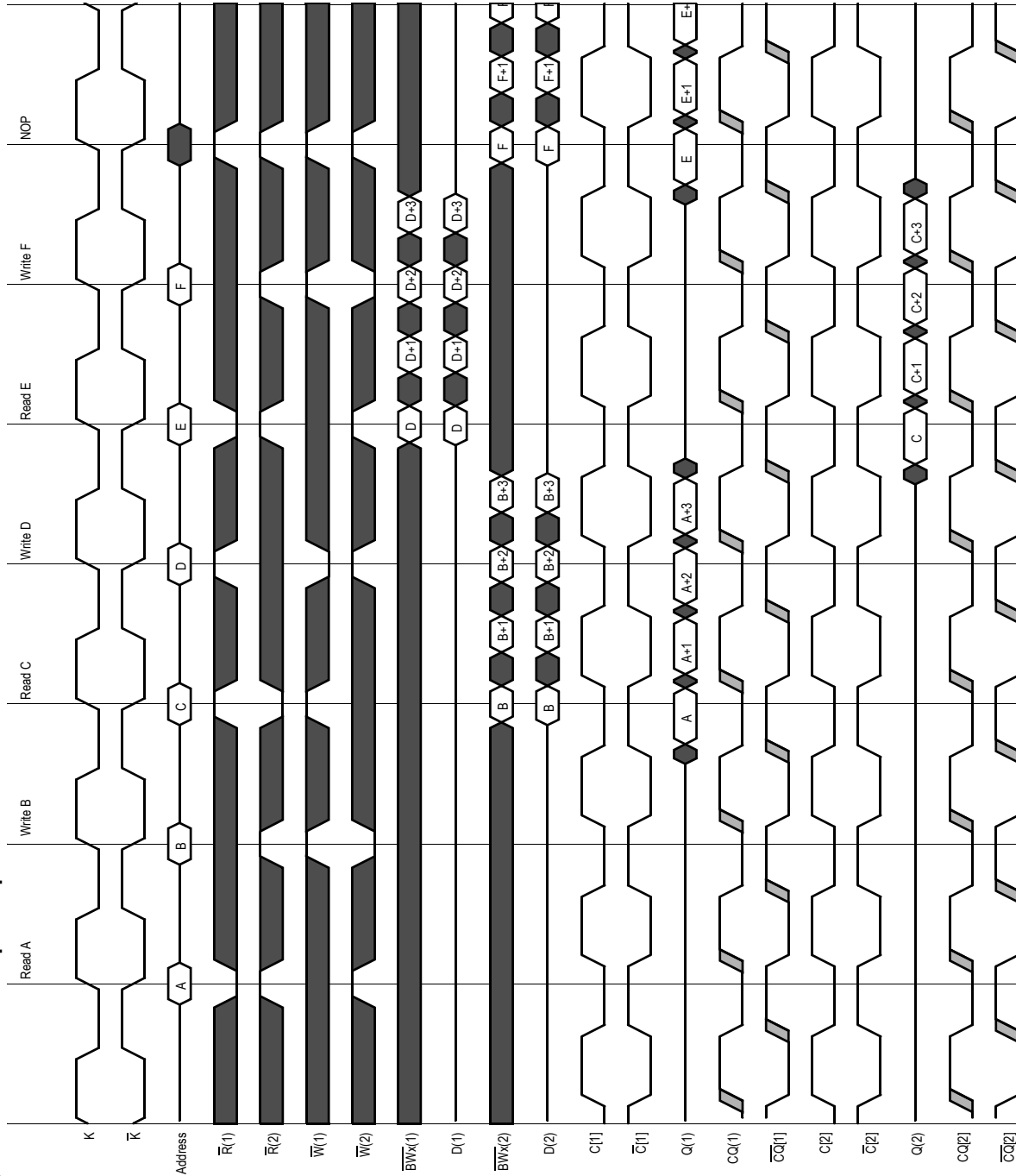
SigmaQuad-II SRAMs offer two mechanisms for controlling the output data registers. Typically, control is handled by the Output Register Clock inputs, C and  $\overline{C}$ . The Output Register Clock inputs can be used to make small phase adjustments in the firing of the output registers by allowing the user to delay driving data out as much as a few nanoseconds beyond the next rising edges of the K and  $\overline{K}$  clocks. If the C and  $\overline{C}$  clock inputs are tied high, the RAM reverts to K and  $\overline{K}$  control of the outputs, allowing the RAM to function as a conventional pipelined read SRAM.

### Example Four Bank Depth Expansion Schematic



**Note:**  
For simplicity  $\overline{BW}_n, \overline{NW}_n, \overline{K}$ , and  $\overline{C}$  are not shown.

**Σ2x2B4 SigmaQuad-II SRAM Depth Expansion**



### FLXDrive-II Output Driver Impedance Control

HSTL I/O SigmaQuad-II SRAMs are supplied with programmable impedance output drivers. The ZQ pin must be connected to  $V_{SS}$  via an external resistor,  $R_Q$ , to allow the SRAM to monitor and adjust its output driver impedance. The value of  $R_Q$  must be 5X the value of the desired RAM output impedance. The allowable range of  $R_Q$  to guarantee impedance matching continuously is between  $150\Omega$  and  $300\Omega$ . Periodic readjustment of the output driver impedance is necessary as the impedance is affected by drifts in supply voltage and temperature. The SRAM's output impedance circuitry compensates for drifts in supply voltage and temperature. A clock cycle counter periodically triggers an impedance evaluation, resets and counts again. Each impedance evaluation may move the output driver impedance level one step at a time towards the optimum level. The output driver is implemented with discrete binary weighted impedance steps. Updates of pull-down drive impedance occur whenever a driver is producing a "1" or is High-Z. Pull-up drive impedance is updated when a driver is producing a "0" or is High-Z.

### Separate I/O SigmaQuad-II B4 SRAM Truth Table

Previous Operation	A	$\bar{R}$	$\bar{W}$	Current Operation	D	D	D	D	Q	Q	Q	Q
$K \uparrow$ ( $t_{n-1}$ )	$K \uparrow$ ( $t_n$ )	$K \uparrow$ ( $t_n$ )	$K \uparrow$ ( $t_n$ )	$K \uparrow$ ( $t_n$ )	$K \uparrow$ ( $t_{n+1}$ )	$\bar{K} \uparrow$ ( $t_{n+1/2}$ )	$K \uparrow$ ( $t_{n+2}$ )	$\bar{K} \uparrow$ ( $t_{n+2/2}$ )	$K \uparrow$ ( $t_{n+1}$ )	$\bar{K} \uparrow$ ( $t_{n+1/2}$ )	$K \uparrow$ ( $t_{n+2}$ )	$\bar{K} \uparrow$ ( $t_{n+2/2}$ )
Deselect	X	1	1	Deselect	X	X	—	—	Hi-Z	Hi-Z	—	—
Write	X	1	X	Deselect	D2	D3	—	—	Hi-Z	Hi-Z	—	—
Read	X	X	1	Deselect	X	X	—	—	Q2	Q3	—	—
Deselect	V	1	0	Write	D0	D1	D2	D3	Hi-Z	Hi-Z	—	—
Deselect	V	0	X	Read	X	X	—	—	Q0	Q1	Q2	Q3
Read	V	X	0	Write	D0	D1	D2	D3	Q2	Q3	—	—
Write	V	0	X	Read	D2	D3	—	—	Q0	Q1	Q2	Q3

#### Notes:

1. "1" = input "high"; "0" = input "low"; "V" = input "valid"; "X" = input "don't care"
2. "—" indicates that the input requirement or output state is determined by the next operation.
3. Q0, Q1, Q2, and Q3 indicate the first, second, third, and fourth pieces of output data transferred during Read operations.
4. D0, D1, D2, and D3 indicate the first, second, third, and fourth pieces of input data transferred during Write operations.
5. Qs are tristated for one cycle in response to Deselect and Write commands, one cycle after the command is sampled, except when preceded by a Read command.
6. Users should not clock in metastable addresses.

### Byte Write Clock Truth Table

$\overline{BW}$	$\overline{BW}$	$\overline{BW}$	$\overline{BW}$	Current Operation	D	D	D	D
$K \uparrow$ ( $t_{n+1}$ )	$\overline{K} \uparrow$ ( $t_{n+1\frac{1}{2}}$ )	$K \uparrow$ ( $t_{n+2}$ )	$\overline{K} \uparrow$ ( $t_{n+2\frac{1}{2}}$ )	$K \uparrow$ ( $t_n$ )	$K \uparrow$ ( $t_{n+1}$ )	$\overline{K} \uparrow$ ( $t_{n+1\frac{1}{2}}$ )	$K \uparrow$ ( $t_{n+2}$ )	$\overline{K} \uparrow$ ( $t_{n+2\frac{1}{2}}$ )
T	T	T	T	Write Dx stored if $\overline{BWn} = 0$ in all four data transfers	D0	D2	D3	D4
T	F	F	F	Write Dx stored if $\overline{BWn} = 0$ in 1st data transfer only	D0	X	X	X
F	T	F	F	Write Dx stored if $\overline{BWn} = 0$ in 2nd data transfer only	X	D1	X	X
F	F	T	F	Write Dx stored if $\overline{BWn} = 0$ in 3rd data transfer only	X	X	D2	X
F	F	F	T	Write Dx stored if $\overline{BWn} = 0$ in 4th data transfer only	X	X	X	D3
F	F	F	F	Write Abort No Dx stored in any of the four data transfers	X	X	X	X

**Notes:**

1. "1" = input "high"; "0" = input "low"; "X" = input "don't care"; "T" = input "true"; "F" = input "false".
2. If one or more  $\overline{BWn} = 0$ , then  $BW = "T"$ , else  $BW = "F"$ .

**x36 Byte Write Enable ( $\overline{BWn}$ ) Truth Table**

$\overline{BW0}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	D0–D8	D9–D17	D18–D26	D27–D35
1	1	1	1	Don't Care	Don't Care	Don't Care	Don't Care
0	1	1	1	Data In	Don't Care	Don't Care	Don't Care
1	0	1	1	Don't Care	Data In	Don't Care	Don't Care
0	0	1	1	Data In	Data In	Don't Care	Don't Care
1	1	0	1	Don't Care	Don't Care	Data In	Don't Care
0	1	0	1	Data In	Don't Care	Data In	Don't Care
1	0	0	1	Don't Care	Data In	Data In	Don't Care
0	0	0	1	Data In	Data In	Data In	Don't Care
1	1	1	0	Don't Care	Don't Care	Don't Care	Data In
0	1	1	0	Data In	Don't Care	Don't Care	Data In
1	0	1	0	Don't Care	Data In	Don't Care	Data In
0	0	1	0	Data In	Data In	Don't Care	Data In
1	1	0	0	Don't Care	Don't Care	Data In	Data In
0	1	0	0	Data In	Don't Care	Data In	Data In
1	0	0	0	Don't Care	Data In	Data In	Data In
0	0	0	0	Data In	Data In	Data In	Data In

**x18 Byte Write Enable ( $\overline{BWn}$ ) Truth Table**

$\overline{BW0}$	$\overline{BW1}$	D0–D8	D9–D17
1	1	Don't Care	Don't Care
0	1	Data In	Don't Care
1	0	Don't Care	Data In
0	0	Data In	Data In

**x09 Byte Write Enable ( $\overline{BWn}$ ) Truth Table**

$\overline{BW0}$	D0–D8
1	Don't Care
0	Data In
1	Don't Care
0	Data In

### Nybble Write Clock Truth Table

$\overline{NW}$	$\overline{NW}$	$\overline{NW}$	$\overline{NW}$	Current Operation	D	D	D	D
$K \uparrow$ ( $t_{n+1}$ )	$\overline{K} \uparrow$ ( $t_{n+1\frac{1}{2}}$ )	$K \uparrow$ ( $t_{n+2}$ )	$\overline{K} \uparrow$ ( $t_{n+2\frac{1}{2}}$ )	$K \uparrow$ ( $t_n$ )	$K \uparrow$ ( $t_{n+1}$ )	$\overline{K} \uparrow$ ( $t_{n+1\frac{1}{2}}$ )	$K \uparrow$ ( $t_{n+2}$ )	$\overline{K} \uparrow$ ( $t_{n+2\frac{1}{2}}$ )
T	T	T	T	Write Dx stored if $\overline{NWn} = 0$ in all four data transfers	D0	D2	D3	D4
T	F	F	F	Write Dx stored if $\overline{NWn} = 0$ in 1st data transfer only	D0	X	X	X
F	T	F	F	Write Dx stored if $\overline{NWn} = 0$ in 2nd data transfer only	X	D1	X	X
F	F	T	F	Write Dx stored if $\overline{NWn} = 0$ in 3rd data transfer only	X	X	D2	X
F	F	F	T	Write Dx stored if $\overline{NWn} = 0$ in 4th data transfer only	X	X	X	D3
F	F	F	F	Write Abort No Dx stored in any of the four data transfers	X	X	X	X

**Notes:**

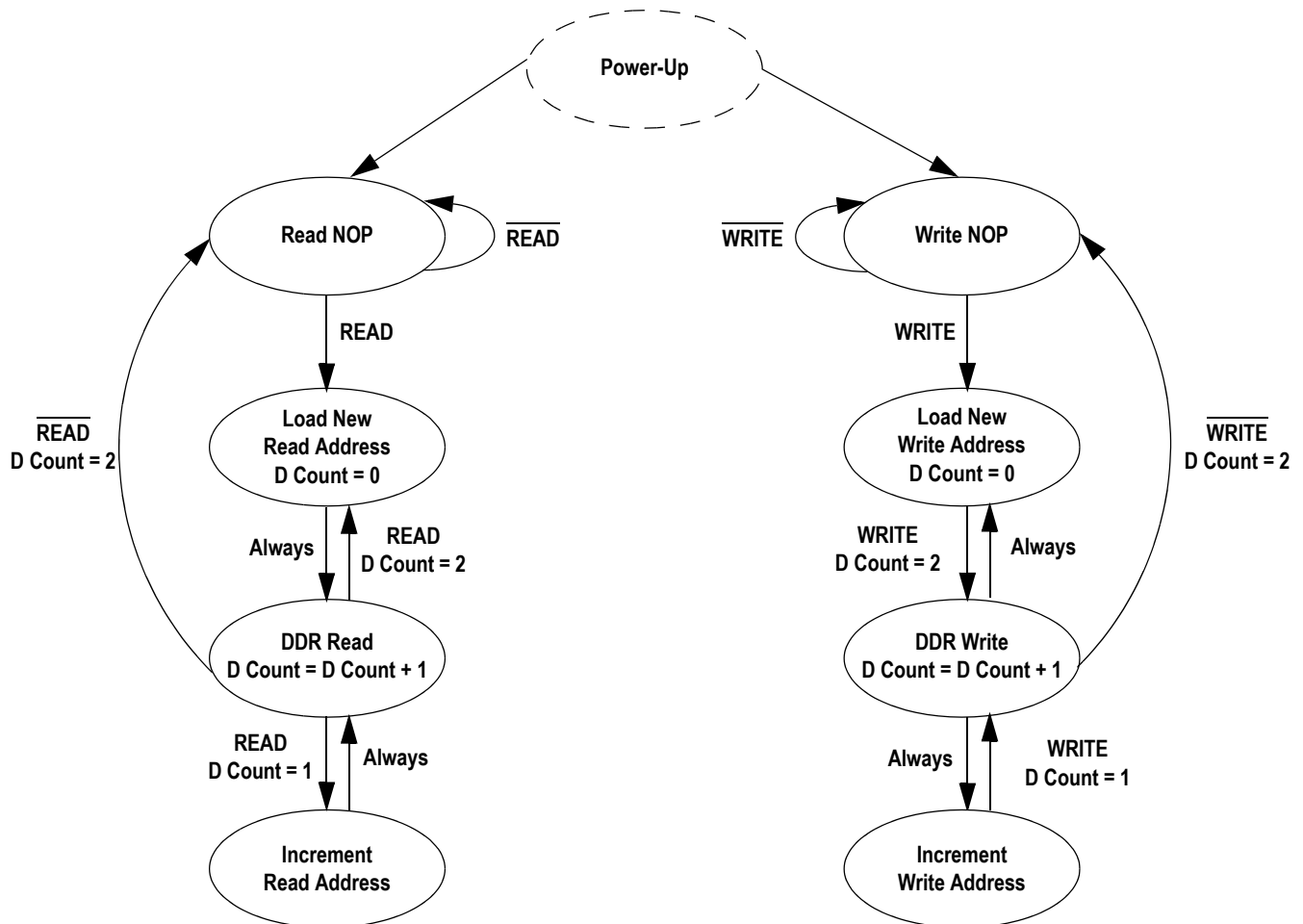
- “1” = input “high”; “0” = input “low”; “X” = input “don’t care”; “T” = input “true”; “F” = input “false”.
- If one or more  $\overline{NWn} = 0$ , then  $\overline{NW} = \text{“T”}$ , else  $\overline{NW} = \text{“F”}$ .

### x8 Nybble Write Enable ( $\overline{NWn}$ ) Truth Table

$\overline{NW0}$	$\overline{NW1}$	D0–D3	D4–D7
1	1	Don't Care	Don't Care
0	1	Data In	Don't Care
1	0	Don't Care	Data In
0	0	Data In	Data In



### State Diagram



**Notes:**

1. Internal burst counter is fixed as 2-bit linear (i.e., when first address is A0+0, next internal burst address is A0+1).
2. "READ" refers to read active status with  $\overline{R}$  = Low, " $\overline{READ}$ " refers to read inactive status with  $\overline{R}$  = High. The same is true for "WRITE" and " $\overline{WRITE}$ ".
3. Read and write state machine can be active simultaneously.
4. State machine control timing sequence is controlled by K.

### Absolute Maximum Ratings

(All voltages reference to  $V_{SS}$ )

Symbol	Description	Value	Unit
$V_{DD}$	Voltage on $V_{DD}$ Pins	-0.5 to 2.9	V
$V_{DDQ}$	Voltage in $V_{DDQ}$ Pins	-0.5 to $V_{DD}$	V
$V_{REF}$	Voltage in $V_{REF}$ Pins	-0.5 to $V_{DDQ}$	V
$V_{I/O}$	Voltage on I/O Pins	-0.5 to $V_{DDQ} + 0.5$ ( $\leq 2.9$ V max.)	V
$V_{IN}$	Voltage on Other Input Pins	-0.5 to $V_{DDQ} + 0.5$ ( $\leq 2.9$ V max.)	V
$I_{IN}$	Input Current on Any Pin	+/-100	mA dc
$I_{OUT}$	Output Current on Any I/O Pin	+/-100	mA dc
$T_J$	Maximum Junction Temperature	125	$^{\circ}$ C
$T_{STG}$	Storage Temperature	-55 to 125	$^{\circ}$ C

**Note:**

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

### Recommended Operating Conditions

#### Power Supplies

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	$V_{DD}$	1.7	1.8	1.9	V
I/O Supply Voltage	$V_{DDQ}$	1.4	1.5	$V_{DD}$	V
Reference Voltage	$V_{REF}$	0.68	—	0.95	V

**Notes:**

- The power supplies need to be powered up simultaneously or in the following sequence:  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{REF}$ , followed by signal inputs. The power down sequence must be the reverse.  $V_{DDQ}$  must not exceed  $V_{DD}$ .
- Most speed grades and configurations of this device are offered in both Commercial and Industrial Temperature ranges. The part number of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

#### Operating Temperature

Parameter	Symbol	Min.	Typ.	Max.	Unit
Ambient Temperature (Commercial Range Versions)	$T_A$	0	25	70	$^{\circ}$ C
Ambient Temperature (Industrial Range Versions)	$T_A$	-40	25	85	$^{\circ}$ C

### HSTL I/O DC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
DC Input Logic High	$V_{IH} (dc)$	$V_{REF} + 0.1$	$V_{DD} + 0.3$	V	1
DC Input Logic Low	$V_{IL} (dc)$	-0.3	$V_{REF} - 0.1$	V	1

**Notes:**

- Compatible with both 1.8 V and 1.5 V I/O drivers
- These are DC test criteria. DC design criteria is  $V_{REF} \pm 50$  mV. The AC  $V_{IH}/V_{IL}$  levels are defined separately for measuring timing parameters.
- $V_{IL} (Min)DC = -0.3$  V,  $V_{IL} (Min)AC = -1.5$  V (pulse width  $\leq 3$  ns).
- $V_{IH} (Max)DC = V_{DDQ} + 0.3$  V,  $V_{IH} (Max)AC = V_{DDQ} + 0.85$  V (pulse width  $\leq 3$  ns).

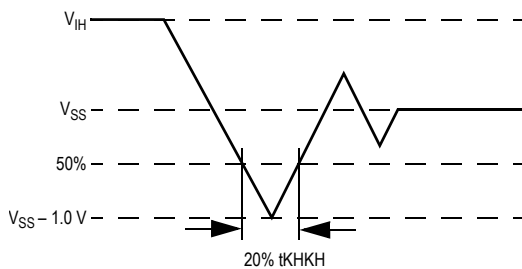
### HSTL I/O AC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
AC Input Logic High	$V_{IH} (ac)$	$V_{REF} + 200$	—	mV	3,4
AC Input Logic Low	$V_{IL} (ac)$	—	$V_{REF} - 200$	mV	3,4
$V_{REF}$ Peak to Peak AC Voltage	$V_{REF} (ac)$	—	5% $V_{REF} (DC)$	mV	1

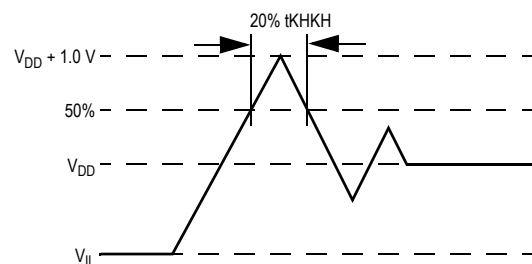
**Notes:**

- The peak to peak AC component superimposed on  $V_{REF}$  may not exceed 5% of the DC component of  $V_{REF}$ .
- To guarantee AC characteristics,  $V_{IH}, V_{IL}, Trise,$  and  $Tfall$  of inputs and clocks must be within 10% of each other.
- For devices supplied with HSTL I/O input buffers. Compatible with both 1.8 V and 1.5 V I/O drivers.

#### Undershoot Measurement and Timing



#### Overshoot Measurement and Timing



### Capacitance

( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{DD} = 1.8\text{ V}$ )

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	$C_{IN}$	$V_{IN} = 0\text{ V}$	4	5	pF
Output Capacitance	$C_{OUT}$	$V_{OUT} = 0\text{ V}$	6	7	pF
Clock Capacitance	$C_{CLK}$	$V_{IN} = 0\text{ V}$	5	6	pF

**Note:**

This parameter is sample tested.

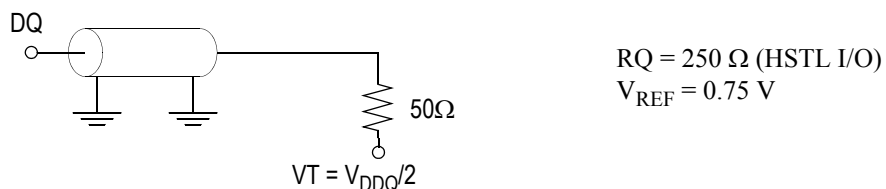
### AC Test Conditions

Parameter	Conditions
Input high level	1.25 V
Input low level	0.25 V
Max. input slew rate	2 V/ns
Input reference level	0.75 V
Output reference level	$V_{DDQ}/2$

**Note:**

Test conditions as specified with output loading as shown unless otherwise noted.

### AC Test Load Diagram



### Input and Output Leakage Characteristics

Parameter	Symbol	Test Conditions	Min.	Max	Notes
Input Leakage Current (except mode pins)	$I_{IL}$	$V_{IN} = 0\text{ to }V_{DD}$	-2 $\mu\text{A}$	2 $\mu\text{A}$	
$\overline{\text{Doff}}$	$I_{INDOFF}$	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0\text{ V} \leq V_{IN} \leq V_{IL}$	-2 $\mu\text{A}$ -2 $\mu\text{A}$	2 $\mu\text{A}$ 2 $\mu\text{A}$	
Output Leakage Current	$I_{OL}$	Output Disable, $V_{OUT} = 0\text{ to }V_{DDQ}$	-2 $\mu\text{A}$	2 $\mu\text{A}$	

### Programmable Impedance HSTL Output Driver DC Electrical Characteristics

Parameter	Symbol	Min.	Max.	Units	Notes
Output High Voltage	$V_{OH1}$	$V_{DDQ}/2 - 0.12$	$V_{DDQ}/2 + 0.12$	V	1, 3
Output Low Voltage	$V_{OL1}$	$V_{DDQ}/2 - 0.12$	$V_{DDQ}/2 + 0.12$	V	2, 3
Output High Voltage	$V_{OH2}$	$V_{DDQ} - 0.2$	$V_{DDQ}$	V	4, 5
Output Low Voltage	$V_{OL2}$	$V_{SS}$	0.2	V	4, 6

**Notes:**

- $I_{OH} = (V_{DDQ}/2) / (RQ/5) \pm 15\%$  @  $V_{OH} = V_{DDQ}/2$  (for:  $175\Omega \leq RQ \leq 350\Omega$ ).
- $I_{OL} = (V_{DDQ}/2) / (RQ/5) \pm 15\%$  @  $V_{OL} = V_{DDQ}/2$  (for:  $175\Omega \leq RQ \leq 350\Omega$ ).
- Parameter tested with  $RQ = 250\Omega$  and  $V_{DDQ} = 1.5$  V or 1.8 V
- Minimum Impedance mode,  $ZQ = V_{SS}$
- $I_{OH} = -1.0$  mA
- $I_{OL} = 1.0$  mA

### Operating Currents

Parameter	Symbol	Test Conditions	-333		-300		-250		-200		-167		Notes
			0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	
Operating Current (x36): DDR	$I_{DD}$	$V_{DD} = \text{Max}, I_{OUT} = 0$ mA Cycle Time $\geq t_{KHKH}$ Min	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	2, 3
Operating Current (x18): DDR	$I_{DD}$	$V_{DD} = \text{Max}, I_{OUT} = 0$ mA Cycle Time $\geq t_{KHKH}$ Min	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	2, 3
Operating Current (x9): DDR	$I_{DD}$	$V_{DD} = \text{Max}, I_{OUT} = 0$ mA Cycle Time $\geq t_{KHKH}$ Min	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	2, 3
Operating Current (x8): DDR	$I_{DD}$	$V_{DD} = \text{Max}, I_{OUT} = 0$ mA Cycle Time $\geq t_{KHKH}$ Min	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	2, 3
Standby Current (NOP): DDR	$I_{SB1}$	Device deselected, $I_{OUT} = 0$ mA, $f = \text{Max}$ , All Inputs $\leq 0.2$ V or $\geq V_{DD} - 0.2$ V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	2, 4

**Notes:**

- Power measured with output pins floating.
- Minimum cycle,  $I_{OUT} = 0$  mA
- Operating current is calculated with 50% read cycles and 50% write cycles.
- Standby Current is only after all pending read and write burst operations are completed.

### AC Electrical Characteristics

Parameter	Symbol	-333		-300		-250		-200		-167		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
<b>Clock</b>													
K, $\overline{K}$ Clock Cycle Time C, C Clock Cycle Time	$t_{KHKH}$ $t_{CHCH}$	3.0	3.5	3.3	4.2	4.0	6.3	5.0	7.88	6.0	8.4	ns	
t <sub>KC</sub> Variable	$t_{KCVar}$	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	ns	5
K, $\overline{K}$ Clock High Pulse Width C, C Clock High Pulse Width	$t_{KHKL}$ $t_{CHCL}$	1.2	—	1.32	—	1.6	—	2.0	—	2.4	—	ns	
K, $\overline{K}$ Clock Low Pulse Width C, C Clock Low Pulse Width	$t_{KLKH}$ $t_{CLCH}$	1.2	—	1.32	—	1.6	—	2.0	—	2.4	—	ns	
K to $\overline{K}$ High C to C High	$t_{KHKH}$	1.35	—	1.49	—	1.8	—	2.2	—	2.7	—	ns	
K, $\overline{K}$ Clock High to C, $\overline{C}$ Clock High	$t_{KHCH}$	0	1.30	0	1.45	0	1.8	0	2.3	0	2.8	ns	
DLL Lock Time	$t_{KCLock}$	1024	—	1024	—	1024	—	1024	—	1024	—	cycle	6
K Static to DLL reset	$t_{KReset}$	30	—	30	—	30	—	30	—	30	—	ns	
<b>Output Times</b>													
K, $\overline{K}$ Clock High to Data Output Valid C, C Clock High to Data Output Valid	$t_{KHQV}$ $t_{CHQV}$	—	0.45	—	0.45	—	0.45	—	0.45	—	0.5	ns	3
K, $\overline{K}$ Clock High to Data Output Hold C, C Clock High to Data Output Hold	$t_{KHQX}$ $t_{CHQX}$	-0.45	—	-0.45	—	-0.45	—	-0.45	—	-0.5	—	ns	3
K, $\overline{K}$ Clock High to Echo Clock Valid C, C Clock High to Echo Clock Valid	$t_{KHCQV}$ $t_{CHCQV}$	—	0.45	—	0.45	—	0.45	—	0.45	—	0.5	ns	
K, $\overline{K}$ Clock High to Echo Clock Hold C, C Clock High to Echo Clock Hold	$t_{KHCQX}$ $t_{CHCQX}$	-0.45	—	-0.45	—	-0.45	—	-0.45	—	-0.5	—	ns	
CQ, $\overline{CQ}$ High Output Valid	$t_{CQHqV}$	—	0.25	—	0.27	—	0.30	—	0.35	—	0.40	ns	7
CQ, $\overline{CQ}$ High Output Hold	$t_{CQHqX}$	-0.25	—	-0.27	—	-0.30	—	-0.35	—	-0.40	—	ns	7
K Clock High to Data Output High-Z C Clock High to Data Output High-Z	$t_{KHQZ}$ $t_{CHQZ}$	—	0.45	—	0.45	—	0.45	—	0.45	—	0.5	ns	3
K Clock High to Data Output Low-Z C Clock High to Data Output Low-Z	$t_{KHQX1}$ $t_{CHQX1}$	-0.45	—	-0.45	—	-0.45	—	-0.45	—	-0.5	—	ns	3
<b>Setup Times</b>													
Address Input Setup Time	$t_{AVKH}$	0.4	—	0.4	—	0.5	—	0.6	—	0.7	—	ns	
Control Input Setup Time	$t_{IVKH}$	0.4	—	0.4	—	0.5	—	0.6	—	0.7	—	ns	2
Data Input Setup Time	$t_{DVKH}$	0.28	—	0.3	—	0.35	—	0.4	—	0.5	—	ns	

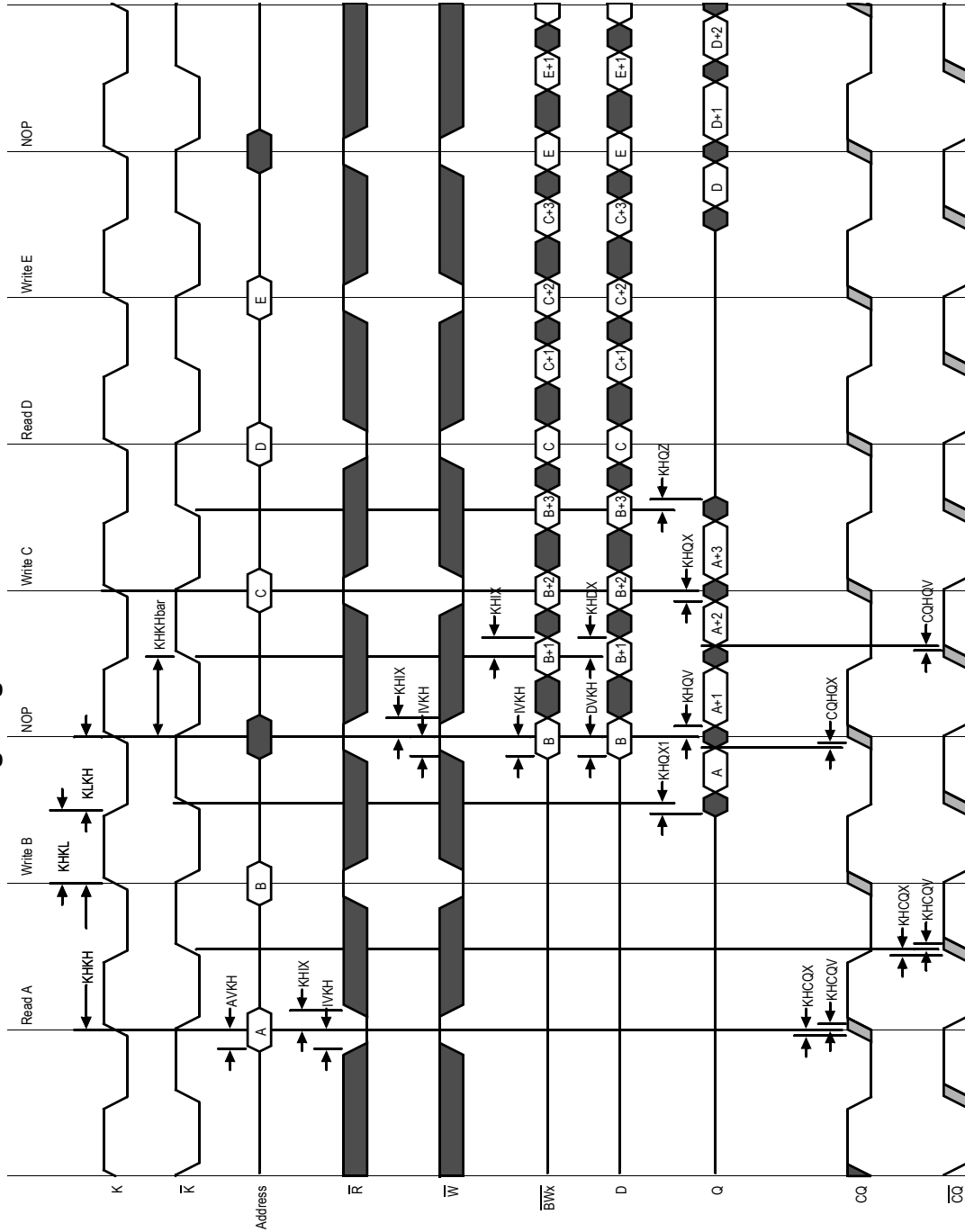
### AC Electrical Characteristics (Continued)

Parameter	Symbol	-333		-300		-250		-200		-167		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
<b>Hold Times</b>													
Address Input Hold Time	$t_{KHAX}$	0.4	—	0.4	—	0.5	—	0.6	—	0.7	—	ns	
Control Input Hold Time	$t_{KHIX}$	0.4	—	0.4	—	0.5	—	0.6	—	0.7	—	ns	
Data Input Hold Time	$t_{KHDX}$	0.28	—	0.3	—	0.35	—	0.4	—	0.5	—	ns	

**Notes:**

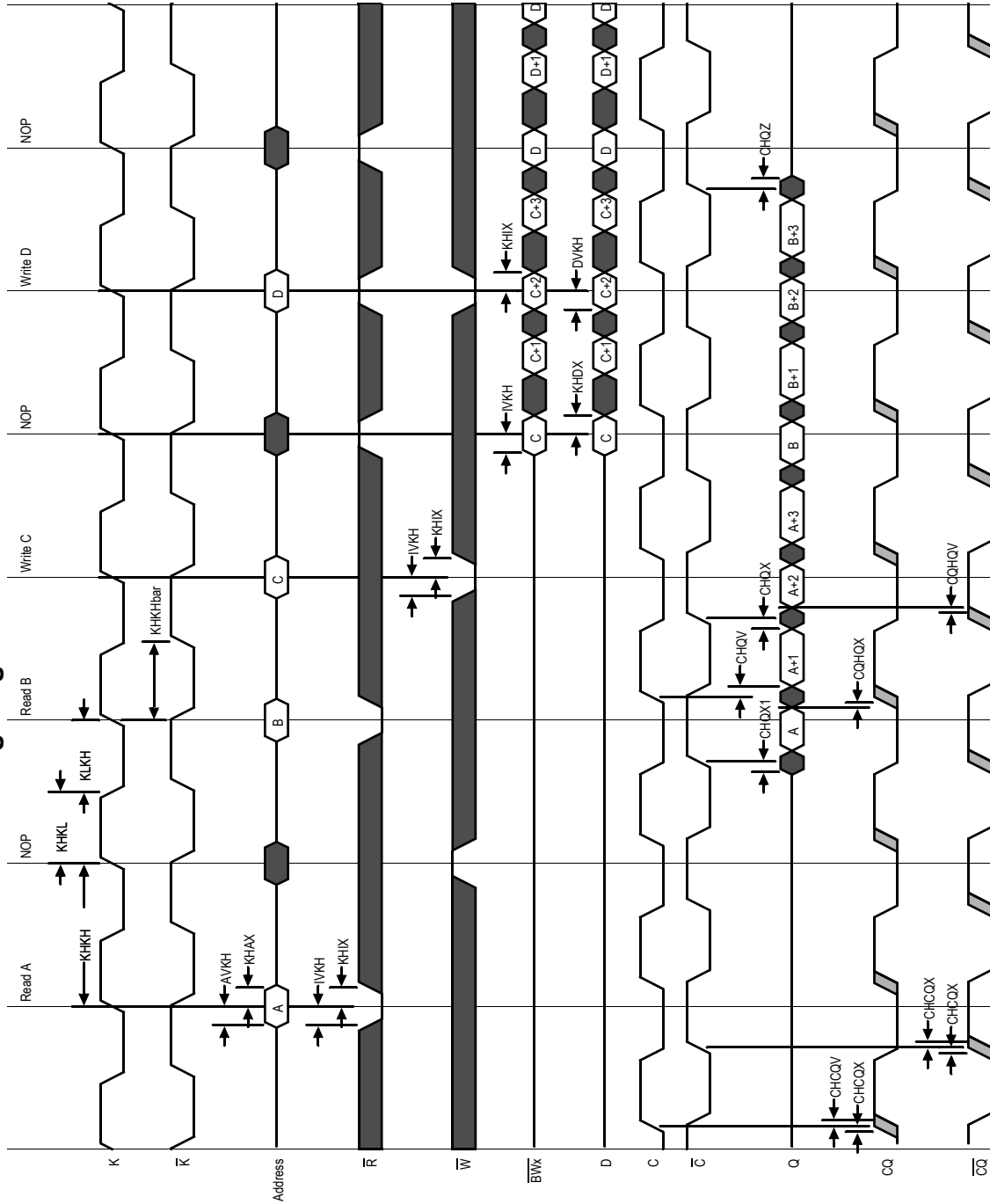
1. All Address inputs must meet the specified setup and hold times for all latching clock edges.
2. Control singles are  $\overline{R}$ ,  $\overline{W}$ ,  $\overline{BW0}$ ,  $\overline{BW1}$ , and ( $\overline{NW0}$ ,  $\overline{NW1}$  for x8) and ( $\overline{BW2}$ ,  $\overline{BW3}$  for x36).
3. If  $\overline{C}$ ,  $\overline{C}$  are tied high, K, K become the references for C,  $\overline{C}$  timing parameters
4. To avoid bus contention, at a given voltage and temperature  $t_{CHQX1}$  is bigger than  $t_{CHQZ}$ . The specs as shown do not imply bus contention because  $t_{CHQX1}$  is a MIN parameter that is worst case at totally different test conditions (0°C, 1.9 V) than  $t_{CHQZ}$ , which is a MAX parameter (worst case at 70°C, 1.7 V). It is not possible for two SRAMs on the same board to be at such different voltages and temperatures.
5. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
6.  $V_{DD}$  slew rate must be less than 0.1 V DC per 50 ns for DLL lock retention. DLL lock time begins once  $V_{DD}$  and input clock are stable.
7. Echo clock is very tightly controlled to data valid/data hold. By design, there is a  $\pm 0.1$  ns variation from echo clock to data. The datasheet parameters reflect tester guard bands and test setup variations.

### K and $\bar{K}$ Controlled Read-Write-Read Timing Diagram





### C and $\bar{C}$ Controlled Read-Write-Read Timing Diagram





### Ordering Information—GSI SigmaQuad-II SRAM

Org	Part Number <sup>1</sup>	Type	Package	Speed (MHz)	T <sub>A</sub> <sup>3</sup>
8M x 8	GS8662D08E-333	SigmaQuad-II SRAM	165-bump BGA	333	C
8M x 8	GS8662D08E-300	SigmaQuad-II SRAM	165-bump BGA	300	C
8M x 8	GS8662D08E-250	SigmaQuad-II SRAM	165-bump BGA	250	C
8M x 8	GS8662D08E-200	SigmaQuad-II SRAM	165-bump BGA	200	C
8M x 8	GS8662D08E-167	SigmaQuad-II SRAM	165-bump BGA	167	C
8M x 8	GS8662D08E-333I	SigmaQuad-II SRAM	165-bump BGA	333	I
8M x 8	GS8662D08E-300I	SigmaQuad-II SRAM	165-bump BGA	300	I
8M x 8	GS8662D08E-250I	SigmaQuad-II SRAM	165-bump BGA	250	I
8M x 8	GS8662D08E-200I	SigmaQuad-II SRAM	165-bump BGA	200	I
8M x 8	GS8662D08E-167I	SigmaQuad-II SRAM	165-bump BGA	167	I
8M x 9	GS8662D09E-333	SigmaQuad-II SRAM	165-bump BGA	333	C
8M x 9	GS8662D09E-300	SigmaQuad-II SRAM	165-bump BGA	300	C
8M x 9	GS8662D09E-250	SigmaQuad-II SRAM	165-bump BGA	250	C
8M x 9	GS8662D09E-200	SigmaQuad-II SRAM	165-bump BGA	200	C
8M x 9	GS8662D09E-167	SigmaQuad-II SRAM	165-bump BGA	167	C
8M x 9	GS8662D09E-333I	SigmaQuad-II SRAM	165-bump BGA	333	I
8M x 9	GS8662D09E-300I	SigmaQuad-II SRAM	165-bump BGA	300	I
8M x 9	GS8662D09E-250I	SigmaQuad-II SRAM	165-bump BGA	250	I
8M x 9	GS8662D09E-200I	SigmaQuad-II SRAM	165-bump BGA	200	I
8M x 9	GS8662D09E-167I	SigmaQuad-II SRAM	165-bump BGA	167	I
4M x 18	GS8662D18E-333	SigmaQuad-II SRAM	165-bump BGA	333	C
4M x 18	GS8662D18E-300	SigmaQuad-II SRAM	165-bump BGA	300	C
4M x 18	GS8662D18E-250	SigmaQuad-II SRAM	165-bump BGA	250	C
4M x 18	GS8662D18E-200	SigmaQuad-II SRAM	165-bump BGA	200	C
4M x 18	GS8662D18E-167	SigmaQuad-II SRAM	165-bump BGA	167	C
4M x 18	GS8662D18E-333I	SigmaQuad-II SRAM	165-bump BGA	333	I
4M x 18	GS8662D18E-300I	SigmaQuad-II SRAM	165-bump BGA	300	I
4M x 18	GS8662D18E-250I	SigmaQuad-II SRAM	165-bump BGA	250	I
4M x 18	GS8662D18E-200I	SigmaQuad-II SRAM	165-bump BGA	200	I
4M x 18	GS8662D18E-167I	SigmaQuad-II SRAM	165-bump BGA	167	I

**Notes:**

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- T<sub>A</sub> = C = Commercial Temperature Range. T<sub>A</sub> = I = Industrial Temperature Range.

### Ordering Information—GSI SigmaQuad-II SRAM

Org	Part Number <sup>1</sup>	Type	Package	Speed (MHz)	T <sub>A</sub> <sup>3</sup>
2M x 36	GS8662D36E-333	SigmaQuad-II SRAM	165-bump BGA	333	C
2M x 36	GS8662D36E-300	SigmaQuad-II SRAM	165-bump BGA	300	C
2M x 36	GS8662D36E-250	SigmaQuad-II SRAM	165-bump BGA	250	C
2M x 36	GS8662D36E-200	SigmaQuad-II SRAM	165-bump BGA	200	C
2M x 36	GS8662D36E-167	SigmaQuad-II SRAM	165-bump BGA	167	C
2M x 36	GS8662D36E-333I	SigmaQuad-II SRAM	165-bump BGA	333	I
2M x 36	GS8662D36E-300I	SigmaQuad-II SRAM	165-bump BGA	300	I
2M x 36	GS8662D36E-250I	SigmaQuad-II SRAM	165-bump BGA	250	I
2M x 36	GS8662D36E-200I	SigmaQuad-II SRAM	165-bump BGA	200	I
2M x 36	GS8662D36E-167I	SigmaQuad-II SRAM	165-bump BGA	167	I
8M x 8	GS8662D08E-333	SigmaQuad-II SRAM	165-bump BGA	333	C
8M x 8	GS8662D08GE-300	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	300	C
8M x 8	GS8662D08GE-250	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	250	C
8M x 8	GS8662D08GE-200	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	200	C
8M x 8	GS8662D08GE-167	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	167	C
8M x 8	GS8662D08GE-333I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	333	I
8M x 8	GS8662D08GE-300I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	300	I
8M x 8	GS8662D08GE-250I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	250	I
8M x 8	GS8662D08GE-200I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	200	I
8M x 8	GS8662D08GE-167I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	167	I
8M x 9	GS8662D09GE-333	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	333	C
8M x 9	GS8662D09GE-300	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	300	C
8M x 9	GS8662D09GE-250	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	250	C
8M x 9	GS8662D09GE-200	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	200	C
8M x 9	GS8662D09GE-167	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	167	C
8M x 9	GS8662D09GE-333I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	333	I
8M x 9	GS8662D09GE-300I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	300	I
8M x 9	GS8662D09GE-250I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	250	I
8M x 9	GS8662D09GE-200I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	200	I
8M x 9	GS8662D09GE-167I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	167	I

**Notes:**

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### Ordering Information—GSI SigmaQuad-II SRAM

Org	Part Number <sup>1</sup>	Type	Package	Speed (MHz)	T <sub>A</sub> <sup>3</sup>
4M x 18	GS8662D18GE-333	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	333	C
4M x 18	GS8662D18GE-300	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	300	C
4M x 18	GS8662D18GE-250	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	250	C
4M x 18	GS8662D18GE-200	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	200	C
4M x 18	GS8662D18GE-167	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	167	C
4M x 18	GS8662D18GE-333I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	333	I
4M x 18	GS8662D18GE-300I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	300	I
4M x 18	GS8662D18GE-250I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	250	I
4M x 18	GS8662D18GE-200I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	200	I
4M x 18	GS8662D18GE-167I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	167	I
2M x 36	GS8662D36GE-333	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	333	C
2M x 36	GS8662D36GE-300	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	300	C
2M x 36	GS8662D36GE-250	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	250	C
2M x 36	GS8662D36GE-200	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	200	C
2M x 36	GS8662D36GE-167	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	167	C
2M x 36	GS8662D36GE-333I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	333	I
2M x 36	GS8662D36GE-300I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	300	I
2M x 36	GS8662D36GE-250I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	250	I
2M x 36	GS8662D36GE-200I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	200	I
2M x 36	GS8662D36GE-167I	SigmaQuad-II SRAM	RoHS-compliant 165-bump BGA	167	I

**Notes:**

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