HMC376LP3 / 376LP3E

v00.1005

GaAs PHEMT MMIC LOW NOISE AMPLIFIER, 700 - 1000 MHz

Typical Applications

The HMC376LP3 / HMC376LP3E is ideal for:

- Cellular/3G Infrastructure
- Base Stations & Repeaters
- CDMA, W-CDMA, & TD-SCDMA
- Private Land Mobile Radio
- GSM/GPRS & EDGE
- UHF Reallocation Applications

Features

Noise Figure: 0.7 dB

Output IP3: +36 dBm

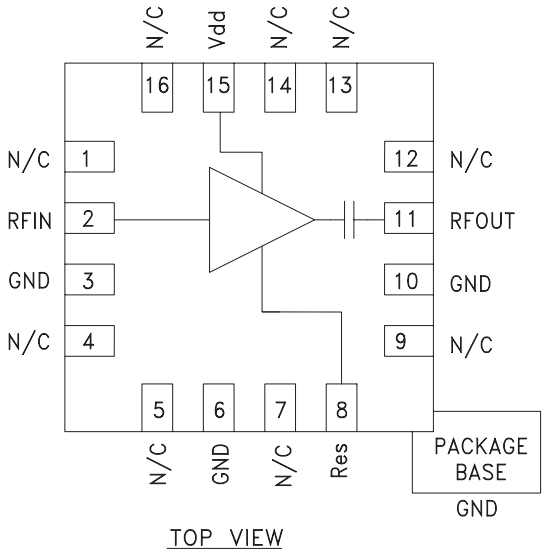
Gain: 15 dB

Externally Adjustable Supply Current

Single Positive Supply: +5.0V

50 Ohm Matched Input/Output

Functional Diagram



TOP VIEW

General Description

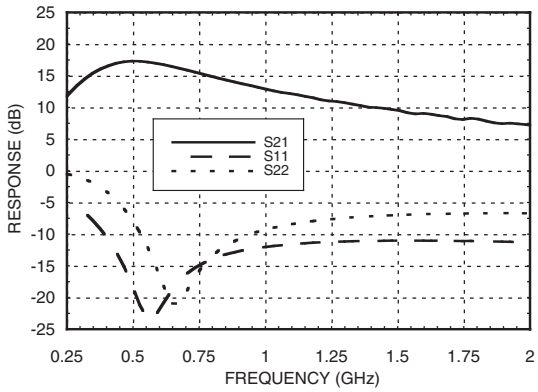
The HMC376LP3 & HMC376LP3E are GaAs PHEMT MMIC Low Noise Amplifiers that are ideal for GSM & CDMA cellular basestation front-end receivers operating between 700 and 1000 MHz. The amplifier has been optimized to provide 0.7 dB noise figure, 15 dB gain and +36 dBm output IP3 from a single supply of +5.0V. Input and output return losses are 14 and 12 dB respectively and the LNA requires only one external component to optimize the RF Input match. The HMC376LP3 & HMC376LP3E share the same package and pinout with the HMC382LP3 1.7 - 2.2 GHz LNA. The HMC376LP3 & HMC376LP3E feature an externally adjustable supply current which allows the designer to tailor the linearity performance of the LNA for each application.

Electrical Specifications, T_A = +25° C, Vdd = +5V, Rbias = 10 Ohms*

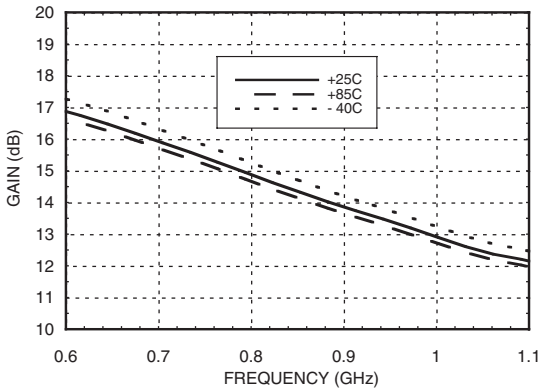
Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		810 - 960			700 - 1000		MHz
Gain	12.5	14.5		11.5	14.5		dB
Gain Variation Over Temperature		0.005	0.01		0.005	0.01	dB / °C
Noise Figure		0.7	1.0		0.7	1.0	dB
Input Return Loss		13			14		dB
Output Return Loss		12			12		dB
Reverse Isolation		20			22		dB
Output Power for 1dB Compression (P1dB)		21.5			21		dBm
Saturated Output Power (Psat)		22			22		dBm
Output Third Order Intercept (IP3) (-20 dBm Input Power per tone, 1 MHz tone spacing)		36			36		dBm
Supply Current (Idd)		73			73		mA

*Rbias resistor value sets current, see application circuit herein.

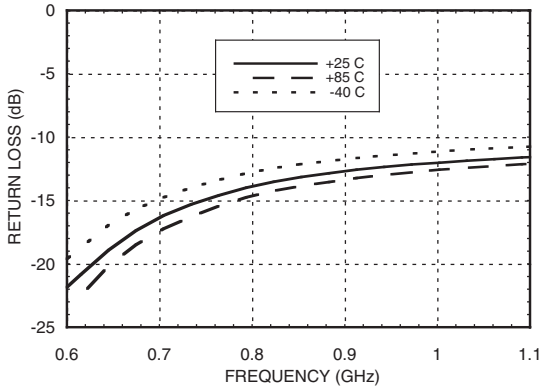
Broadband Gain & Return Loss



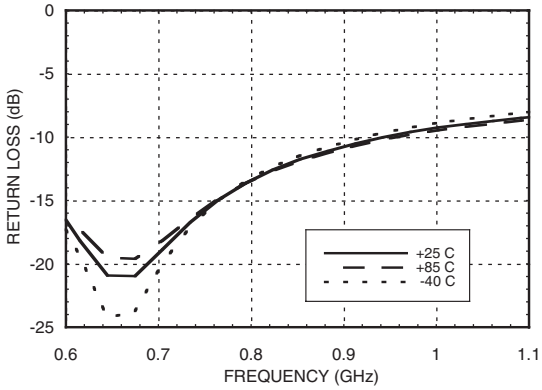
Gain vs. Temperature



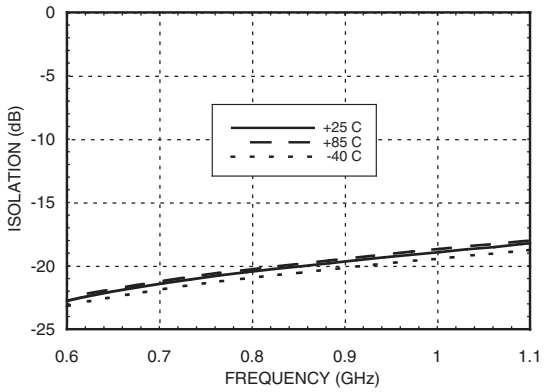
Input Return Loss vs. Temperature



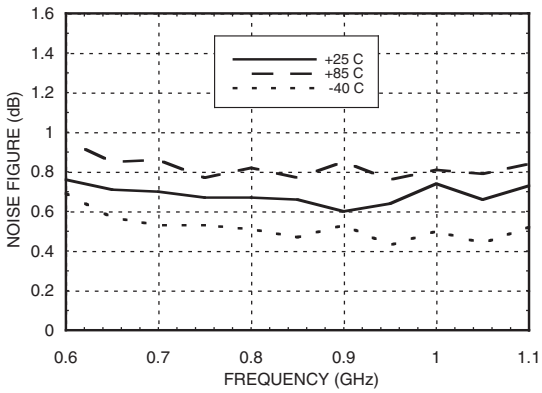
Output Return Loss vs. Temperature



Reverse Isolation vs. Temperature



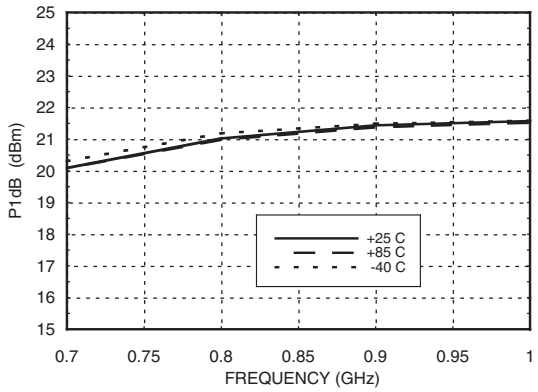
Noise Figure vs. Temperature



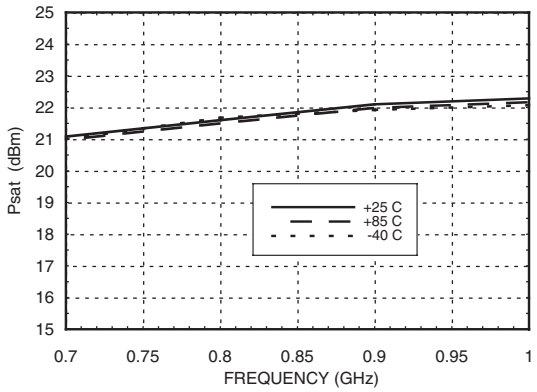
HMC376LP3 / 376LP3E

GaAs PHEMT MMIC LOW NOISE AMPLIFIER, 700 - 1000 MHz

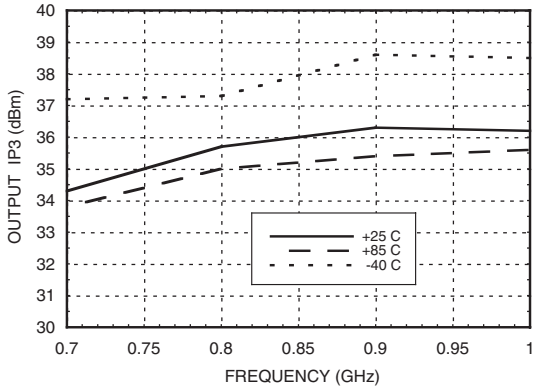
P1dB vs. Temperature @ Idd = 73 mA



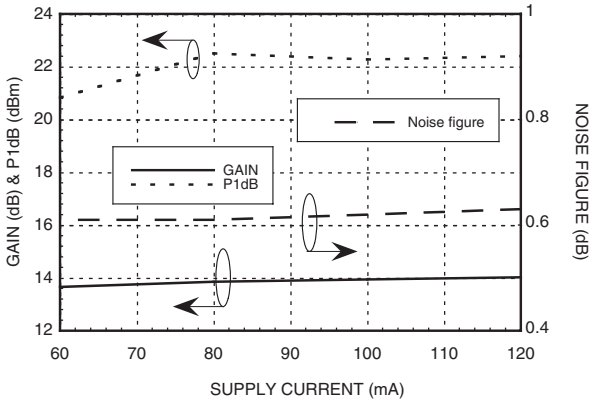
Psat vs. Temperature @ Idd = 73 mA



Output IP3 vs. Temperature @ Idd = 73 mA



Gain, Noise Figure & Power vs. Supply Current @ 900 MHz



Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	+8.0 Vdc
RF Input Power (RFin)(Vs = +5.0 Vdc)	+15 dBm
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 11.83 mW/°C above 85 °C)	0.769 W
Thermal Resistance (channel to ground paddle)	84.5 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

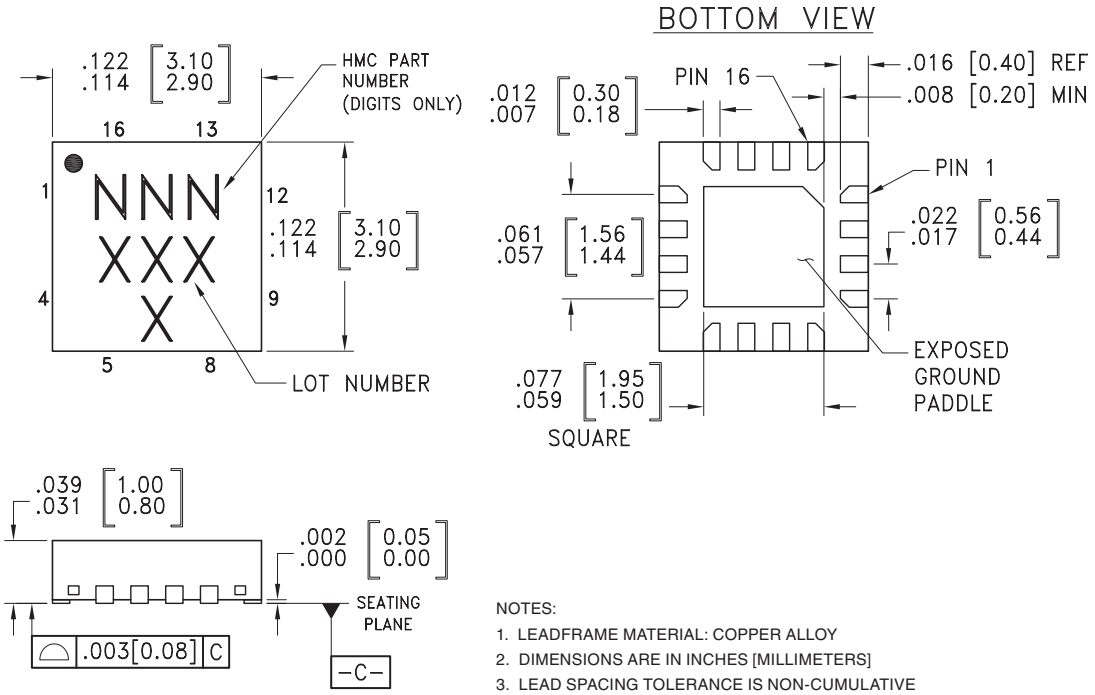
Typical Supply Current vs. Vdd with Rbias = 10 Ohms

Vdd (Vdc)	Idd (mA)
+4.5	73.0
+5.0	73.4
+5.5	73.6

Recommended Bias Resistor Values for Various Idd

Idd (mA)	Rbias (Ohms)
60	12
70	10
80	9.1
100	6.8
120	5.1

Outline Drawing



NOTES:

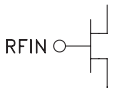
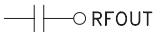
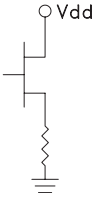
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

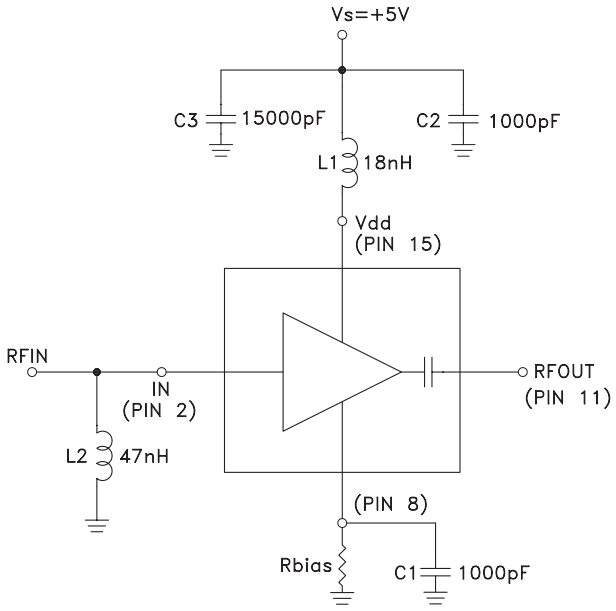
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC376LP3	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H376 XXXX
HMC376LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H376 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Pin Descriptions

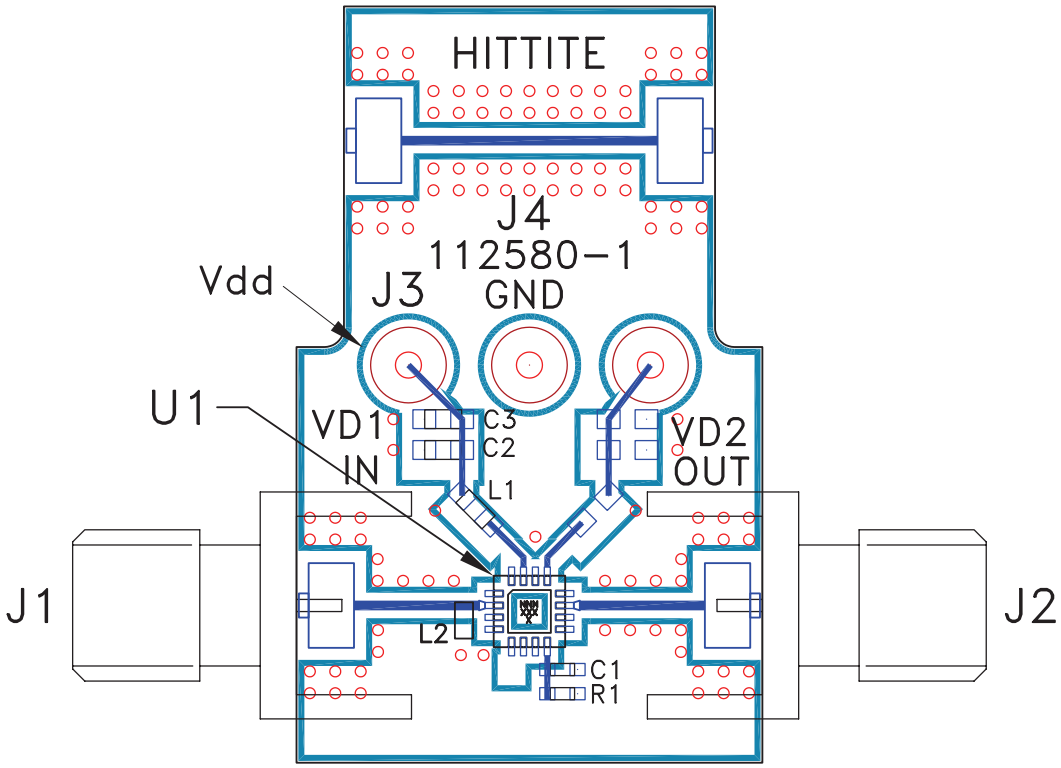
Pin Number	Function	Description	Interface Schematic
1, 4, 5, 7, 9, 12 - 14, 16	N/C	No connection necessary. These pins may be connected to RF/DC ground. Performance will not be affected.	
2	RFIN	This pin is matched to 50 Ohms with a 47 nH inductor to ground. See application circuit.	
3, 6, 10	GND	These pins and package bottom must be connected to RF/DC ground.	
8	Res	This pin is used to set the DC current of the amplifier by selection of external bias resistor. See application circuit.	
11	RFOUT	This pin is AC coupled and matched to 50 Ohms from 0.7 - 1.0 GHz.	
15	Vdd	Power supply voltage. Choke inductor and bypass capacitors are required. See application circuit.	

Application Circuit



Note 1: L1, L2 and C1 should be located as close to the pins as possible.

Evaluation PCB



List of Materials for Evaluation PCB 112585 [1]

Item	Description
J1 - J2	PCB Mount SMA RF Connector
J3 - J4	DC Pin
C1	1000 pF Capacitor, 0402 Pkg.
C2	1000 pF Capacitor, 0603 Pkg.
C3	15000 pF Capacitor, 0603 Pkg.
L1	18 nH Inductor, 0603 Pkg.
L2	47 nH Inductor, 0603 Pkg.
R1	Resistor, 0402 Pkg.
U1	HMC376LP3 / HMC376LP3E Amplifier
PCB [2]	112580 Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.