SRAM MODULE 1MByte (128K x 64 bit), 120-Pin SMM, 3.3V
Part No. HMS12864F8VL

GENERAL DESCRIPTION

The HMS12864F8VL is a high-speed static random access memory (SRAM) module containing 131,072 words organized in a x 64-bit configuration. The module consists of eight 128K x 8 SRAMs mounted on a 120-pin, both-sided, FR4-printed circuit board.

Byte write enable inputs,(/WE0,/WE1,/WE2,/WE3,/WE4,/WE5,/WE6,/WE7) are used to enable the module's 8 bits independently. Output enable(/OE) and write enable(/WE) can set the memory input and output.

Data is written into the SRAM memory when write enable (/WE) and chip enable (/CE) inputs are both LOW. Reading is accomplished when /WE remains HIGH and /CE and output enable (/OE) are LOW.

For reliability, this SRAM module is designed as multiple power and ground pin. All module components may be powered from a single +3.3V DC power supply and all inputs and outputs are fully TTL-compatible.

FEATURES

- Access times : 70 and 100ns
- High-density 1MByte design
- High-reliability, high-speed design
- Single + 3.3V ±0.3V power supply
- Easy memory expansion with /CE and /OE functions
- All inputs and outputs are TTL-compatible
- Industry-standard pin-out
- FR4-PCB design

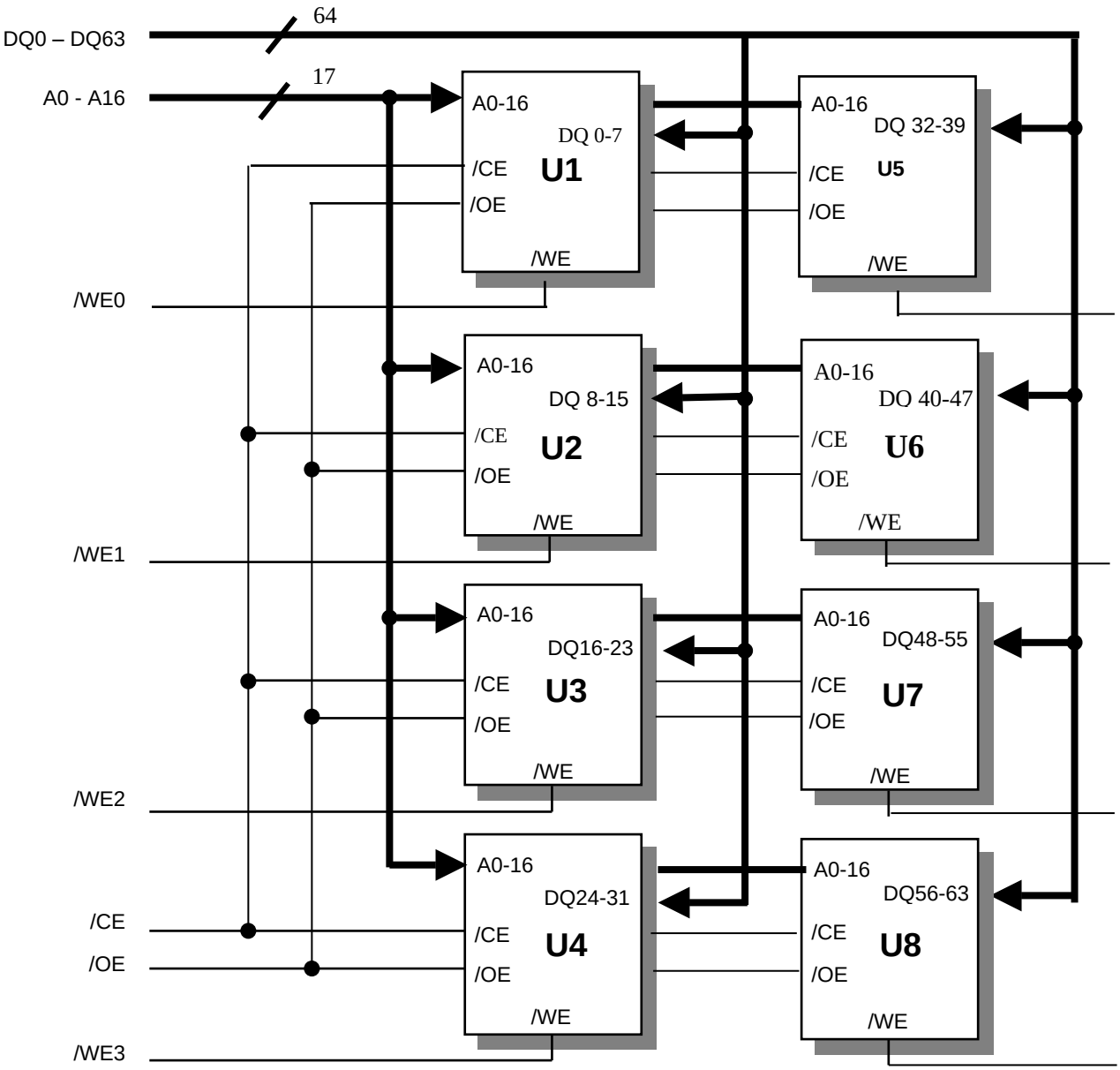
OPTIONS MARKING

- Timing
  - 70ns access - 70
  - 100ns access -100
- Packages
  - 120-pin SMM F

PIN ASSIGNMENT

P1				P2			
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	Vcc	31	Vss	1	Vcc	31	Vss
2	DQ32	32	DQ7	2	DQ24	32	DQ63
3	DQ33	33	DQ6	3	DQ25	33	DQ62
4	DQ34	34	DQ5	4	DQ26	34	DQ61
5	DQ35	35	DQ4	5	DQ27	35	DQ60
6	DQ36	36	DQ3	6	DQ28	36	DQ59
7	DQ37	37	DQ2	7	DQ29	37	DQ58
8	DQ38	38	DQ1	8	DQ30	38	DQ57
9	DQ39	39	DQ0	9	DQ31	39	DQ56
10	Vcc	40	Vss	10	Vcc	40	Vss
11	DQ40	41	DQ15	11	DQ16	41	DQ55
12	DQ41	42	DQ14	12	DQ17	42	DQ54
13	DQ42	43	DQ13	13	DQ18	43	DQ53
14	DQ43	44	DQ12	14	DQ19	44	DQ52
15	DQ44	45	DQ11	15	DQ20	45	DQ51
16	DQ45	46	DQ10	16	DQ21	46	DQ50
17	DQ46	47	DQ9	17	DQ22	47	DQ49
18	DQ47	48	DQ8	18	DQ23	48	DQ48
19	Vcc	49	Vss	19	Vcc	49	Vss
20	/WE0	50	A0	20	A16	50	NC
21	/WE1	51	A1	21	A15	51	NC
22	/WE2	52	A2	22	A14	52	/OE
23	/WE3	53	A3	23	A13	53	NC
24	/WE4	54	A4	24	A12	54	NC
25	Vcc	55	Vss	25	Vcc	55	Vss
26	/WE5	56	A5	26	A11	56	NC
27	/WE6	57	A6	27	A10	57	NC
28	/WE7	58	A7	28	A9	58	NC
29	/CS2	59	/CS1	29	A8	59	NC
30	Vcc	60	Vss	30	Vcc	60	Vss

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-0.5V to Vcc+0.5V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.3V to 4.6V
Power Dissipation	P_D	8.0W
Storage Temperature	T_{STG}	-65°C to +150°C
Operating Temperature	T_A	0°C to +70°C

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 °C)

PARAMETER	SYMBOL	MIN	TYP.	MAX
Supply Voltage	V_{CC}	3.0V	3.3V	3.6V
Ground	V_{SS}	0	0	0
Input High Voltage	V_{IH}	2.2	-	Vcc+0.3V**
Input Low Voltage	V_{IL}	-0.3*	-	0.6V

* V_{IL}(Min.) = -2.0V ac (Pulse Width ≤ 10ns) for I ≤ 20 mA

****** V_{IH}(Min.) = Vcc+2.0V ac (Pulse Width ≤ 10ns) for I ≤ 20 mA

DC AND OPERATING CHARACTERISTICS (1)(0°C ≤ T_A ≤ 70 °C ; Vcc = 3.3V ± 10%)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	VIN=Vss to Vcc	IL_I	-8	8	µA
Output Leakage Current	/CE=$V_{IH\ or\ }$/OE =V_{IH} or /WE=V_{IL} V_{OUT}=Vss to V_{CC}	IL_0	-8	8	µA
Output High Voltage	I_{OH} = -4.0Ma	V_{OH}	2.4		V
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V

* Vcc=3.3V, Temp=25 °C

DC AND OPERATING CHARACTERISTICS (2)

DESCRIPTION	TEST CONDITIONS	SYMBOL	MAX		UNIT
			70	100	
Power Supply Current:Operating	Min. Cycle, 100% Duty /CE=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	I_{CC}	32	32	mA
Power Supply Current:Standby	Min. Cycle, /CE=V_{IH}	I_{SB}	2.4	2.4	mA
	f=0MHZ, /CE≥V_{CC}-0.2V, V_{IN}≥ V_{CC}-0.2V or V_{IN}≤0.2V	I_{SB1}	80	80	uA

CAPACITANCE (T_A =25 ^oC , f= 1.0Mhz)

DESCRIPTION	TEST CONDITIONS	SYMBOL	MAX	UNIT
Input /Output Capacitance	$V_{I/O}$=0V	$C_{I/O}$	80	pF
Input Capacitance	V_{IN}=0V	C_{IN}	64	pF

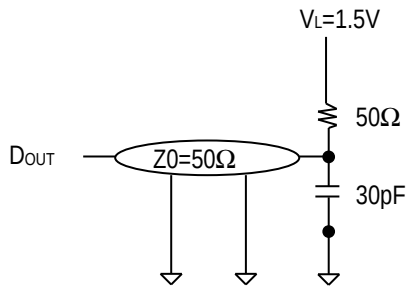
* NOTE : Capacitance is sampled and not 100% tested

AC CHARACTERISTICS ($0^oC \le T_A \le 70\ ^oC$; Vcc = 3.3V ± 0.3V, unless otherwise specified)

Test conditions

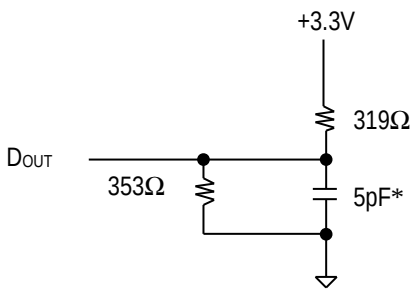
PARAMETER	VALUE
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)

for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ}



READ CYCLE

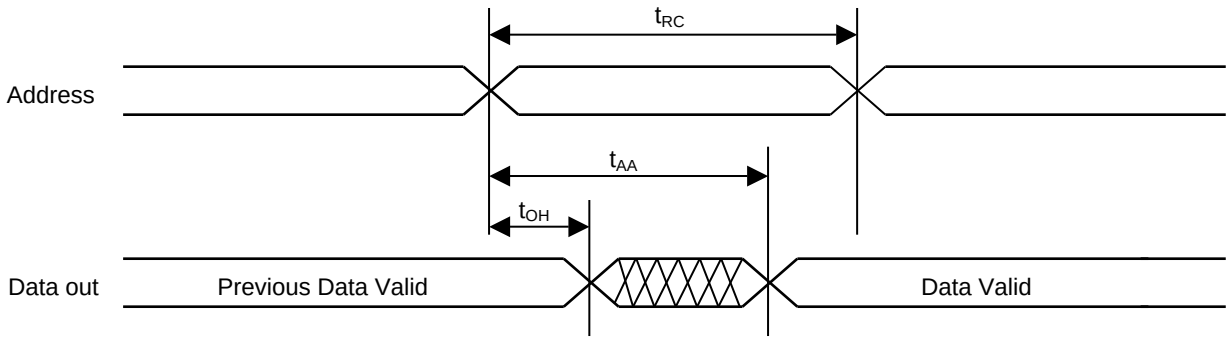
PARAMETER	SYMBOL	70		100		UNIT
		MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	70		100		ns
Address Access Time	t_{AA}		70		100	ns
Chip Select to Output	t_{CO}		70		100	ns
Output Enable to Output	t_{OE}		35		50	ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Chip Enable to Low-Z Output	t_{LZ}	10		10		ns
Output Disable to High-Z Output	t_{OHZ}	0	25	0	30	ns
Chip Disable to High-Z Output	t_{HZ}	0	25	0	30	ns
Output Hold from Address Change	t_{OH}	10		15		ns
Chip Select to Power Up Time	t_{PU}					ns
Chip Select to Power Down Time	t_{PD}					ns

WRITE CYCLE

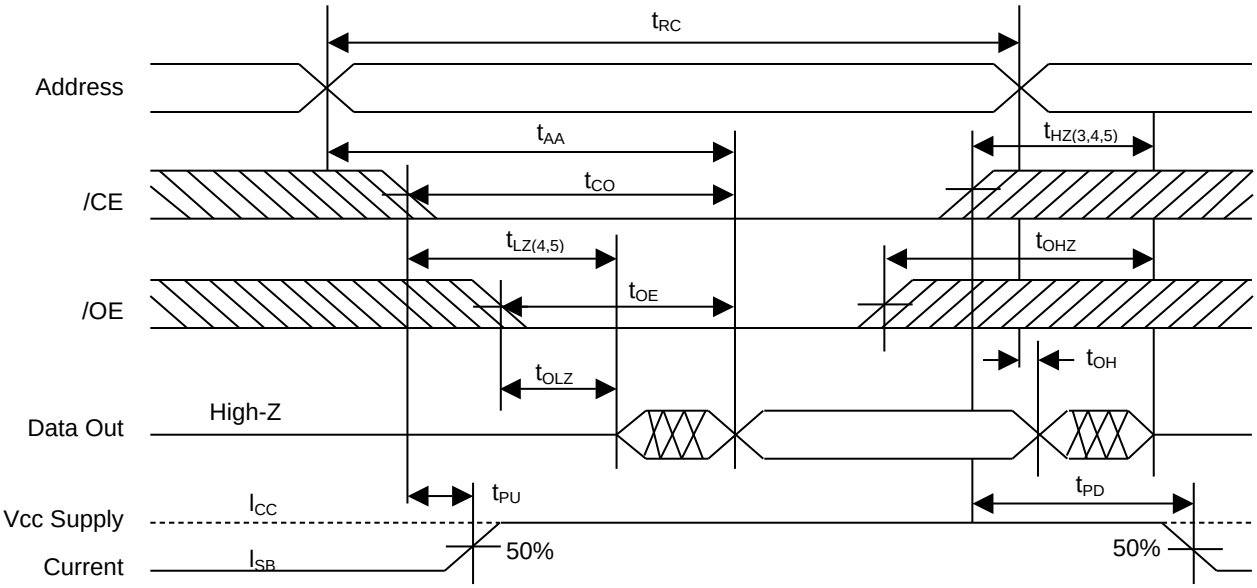
PARAMETER	SYMBOL	70		100		UNIT
		MIN	MAX	MIN	MAX	
Write Cycle Time	t_{WC}	70		100		ns
Chip Select to End of Write	t_{CW}	60		80		ns
Address Set-up Time	t_{AS}	0		0		ns
Address Valid to End of Write	t_{AW}	60		80		ns
Write Pulse Width	t_{WP}	55		70		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to Output High-Z	t_{WHZ}	0	25	0	30	ns
Data to Write Time Overlap	t_{DW}	30		40		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End of Write to Output Low-Z	t_{OW}	5		5		ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(Address Controlled) (/CE =/ OE = V_{IL} , /WE = V_{IH})



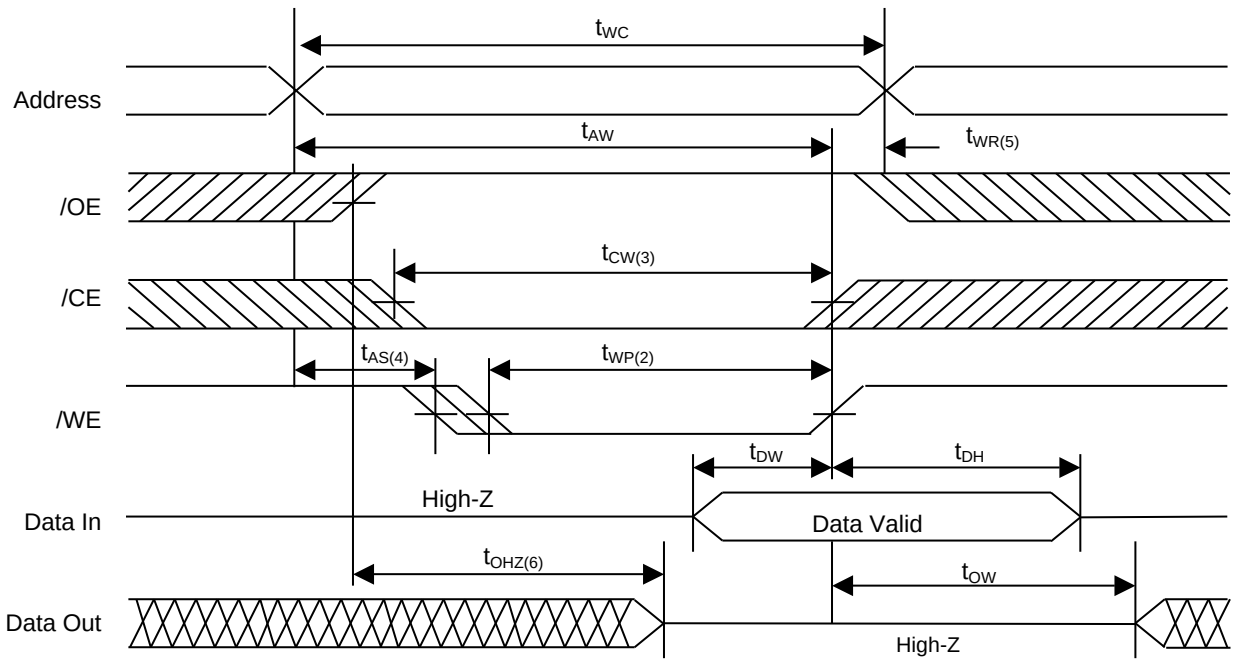
TIMING WAVEFORM OF READ CYCLE (/CE Controlled)



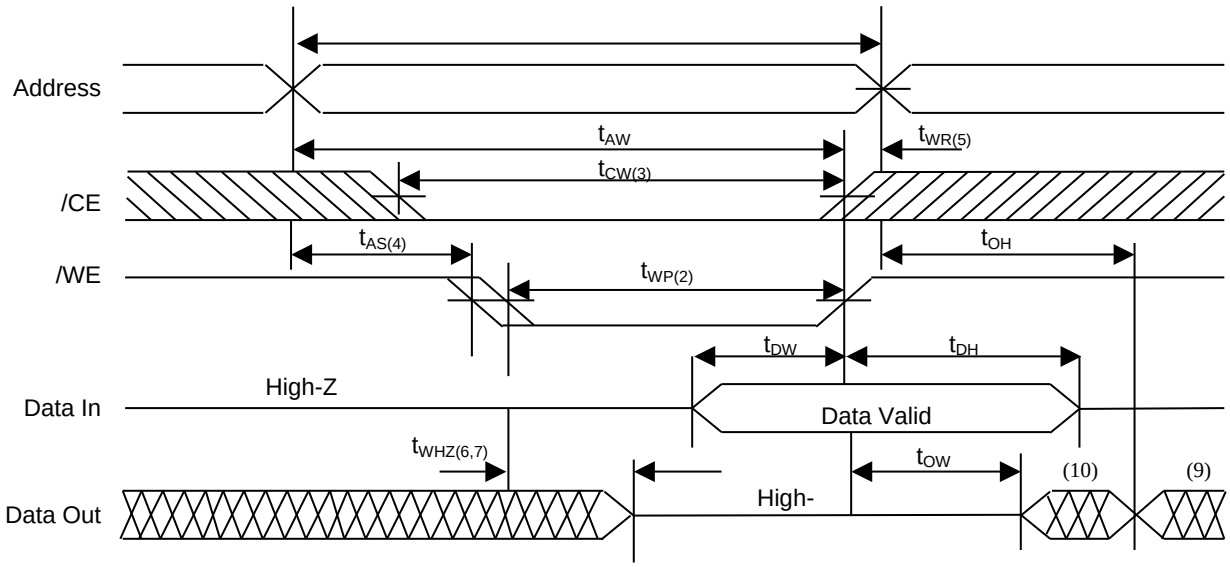
Notes (Read Cycle)

1. /WE is high for read cycle.
2. All read cycle timing is referenced from the last valid address to first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.
5. Transition is measured ± 200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with /CE = V_{IL}.
7. Address valid prior to coincident with /CE transition low.

TIMING WAVEFORM OF WRITE CYCLE (/OE=Clock)



TIMING WAVEFORM OF WRITE CYCLE (/OE Low Fixed)



Notes(Write Cycle)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CE and a low /WE. A write begins at the latest transition among /CE going low and /WE going low: A write ends at the earliest transition among /CE going high and /WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of /CE going low to the end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CE, or /WE going high.
6. If /OE,/CE and /WE are in the read mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CE goes low simultaneously with /WE going low or after /WE going low, the outputs remain high impedance state.
9. D_{OUT} is the read data of the new address.
10. When /CE is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

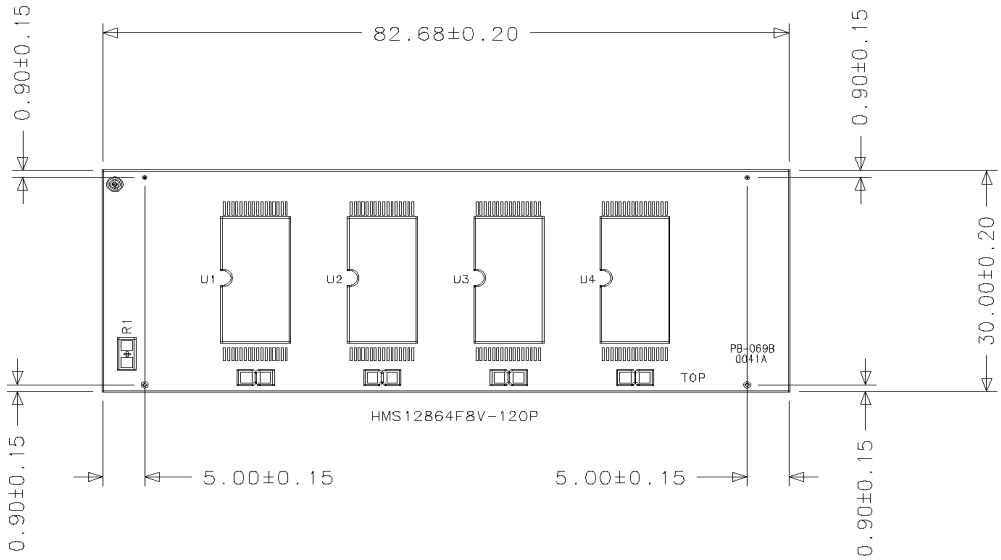
FUNCTIONAL DESCRIPTION

/CE	/WE	/OE	MODE	I/O PIN	SUPPLY CURRENT
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

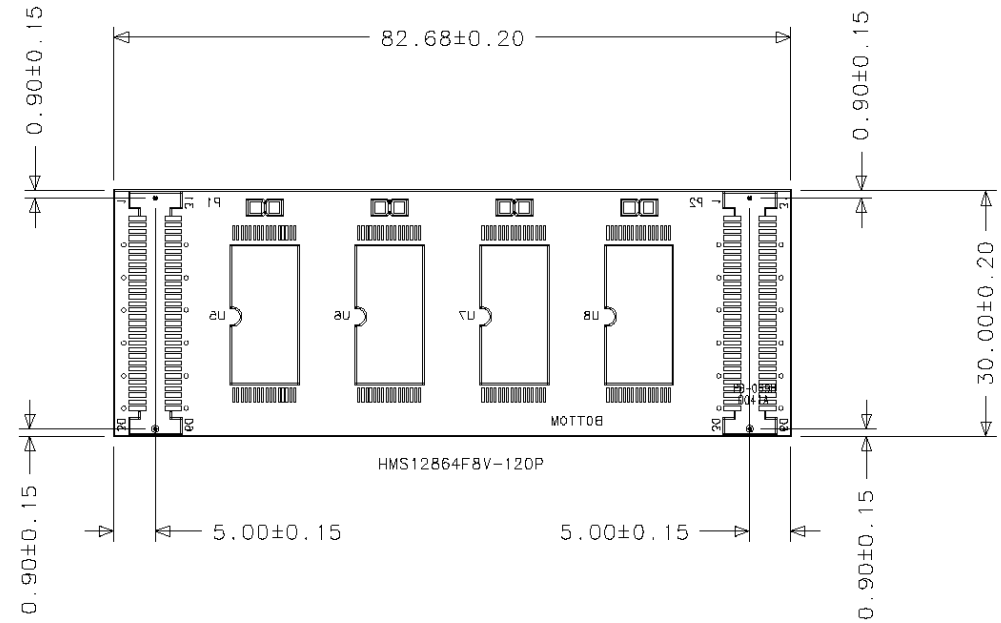
Note: X means Don't Care

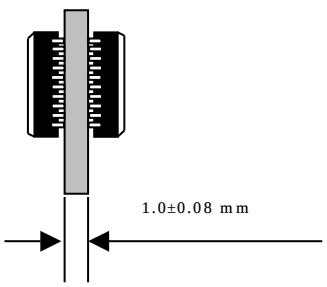
PACKAGING INFORMATION

FRONT SIDE



REAR SIDE





ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	SPEED
HMS12864F8VL-70	1MByte	X 64	120 Pin-SMM	8EA	3.3V	70ns
HMS12864F8VL-100	1MByte	X 64	120 Pin-SMM	8EA	3.3V	100ns