



**Synchronous DRAM Module 32Mbyte(4Mx64-Bit), 144pin SO-DIMM,  
4Banks, 4K Ref., 3.3V**

**Part No. HSD4M64B4W**

## GENERAL DESCRIPTION

The HSD4M64B4W is a 4M x 64 bit Synchronous Dynamic RAM high density memory module. The module consists of four CMOS 1M x 16 bit x 4banks Synchronous DRAMs in TSOP-II 400mil packages on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The HSD4M64B4W is a SO-DIMM(Small Outline Dual in line Memory Module) and is intended for mounting into 144-pin edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications All module components may be powered from a single 3.3V DC power supply and all inputs and outputs are LVTTTL-compatible.

## FEATURES

- Part Identification
  - HSD4M64B4W-10 : 100MHz (CL=2)
  - HSD4M64B4W-10L : 100MHz (CL=3)
  - HSD4M64B4W-12 : 125MHz (CL=3)
  - HSD4M64B4W-13 : 133MHz (CL=3)
- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V  $\pm$ 0.3V power supply
- MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- The used device is 1M x 16bit x 4Banks SDRAM

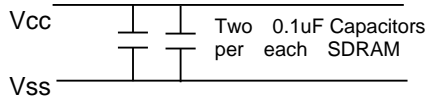
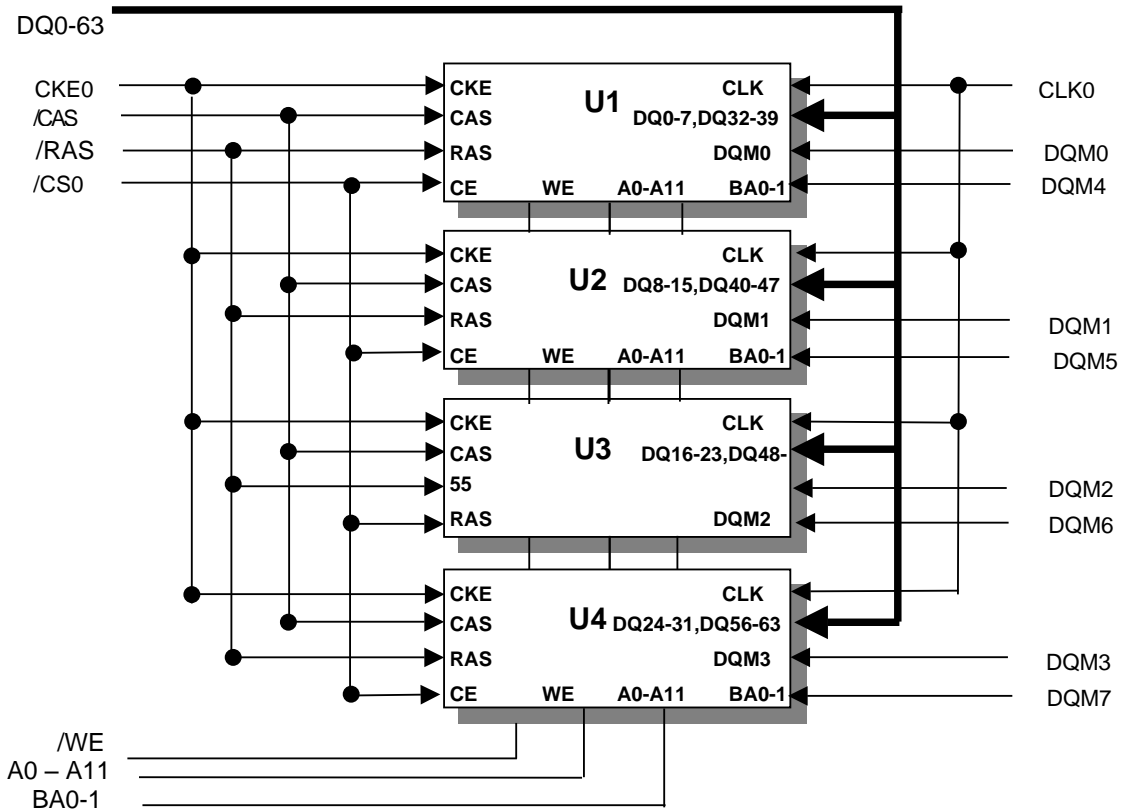
## PIN ASSIGNMENT

| PIN | Front | PIN | Back | PIN | Frontl   | PIN | Back     | PIN | Front  | PIN | Back |
|-----|-------|-----|------|-----|----------|-----|----------|-----|--------|-----|------|
| 1   | Vss   | 2   | Vss  | 49  | DQ13     | 50  | DQ45     | 97  | DQ22   | 98  | DQ54 |
| 3   | DQ0   | 4   | DQ32 | 51  | DQ14     | 52  | DQ46     | 99  | DQ23   | 100 | DQ55 |
| 5   | DQ1   | 6   | DQ33 | 53  | DQ15     | 54  | DQ47     | 101 | VCC    | 102 | VCC  |
| 7   | DQ2   | 8   | DQ34 | 55  | Vss      | 56  | Vss      | 103 | A6     | 104 | A7   |
| 9   | DQ3   | 10  | DQ35 | 57  | NC       | 58  | NC       | 105 | A8     | 106 | BA0  |
| 11  | VCC   | 12  | VCC  | 59  | NC       | 60  | NC       | 107 | Vss    | 108 | Vss  |
| 13  | DQ4   | 14  | DQ36 | 61  | CLK0     | 62  | CKE0     | 109 | A9     | 110 | BA1  |
| 15  | DQ4   | 16  | DQ37 | 63  | VCC      | 64  | VCC      | 111 | A10_AP | 112 | A11  |
| 17  | DQ6   | 18  | DQ38 | 65  | /RAS     | 66  | /CAS     | 113 | VCC    | 114 | VCC  |
| 19  | DQ7   | 20  | DQ39 | 67  | /WE      | 68  | NC(CKE1) | 115 | DQM2   | 116 | DQM6 |
| 21  | Vss   | 22  | Vss  | 69  | /CS0     | 70  | NC(A12)  | 117 | DQM3   | 118 | DQM7 |
| 23  | DQM0  | 24  | DQM4 | 71  | NC(/CS1) | 72  | NC       | 119 | Vss    | 120 | Vss  |
| 25  | DQM1  | 26  | DQM5 | 73  | NC       | 74  | NC(CLK1) | 121 | DQ24   | 122 | DQ56 |
| 27  | VCC   | 28  | VCC  | 75  | Vss      | 76  | Vss      | 123 | DQ25   | 124 | DQ57 |
| 29  | A0    | 30  | A3   | 77  | NC       | 78  | NC       | 125 | DQ26   | 126 | DQ58 |
| 31  | A1    | 32  | A4   | 79  | NC       | 80  | NC       | 127 | DQ27   | 128 | DQ59 |
| 33  | A2    | 34  | A5   | 81  | VCC      | 82  | VCC      | 129 | VCC    | 130 | VCC  |
| 35  | Vss   | 36  | Vss  | 83  | DQ16     | 84  | DQ48     | 131 | DQ28   | 132 | DQ60 |
| 37  | DQ8   | 38  | DQ40 | 85  | DQ17     | 86  | DQ49     | 133 | DQ29   | 134 | DQ61 |
| 39  | DQ9   | 40  | DQ41 | 87  | DQ18     | 88  | DQ50     | 135 | DQ30   | 136 | DQ62 |
| 41  | DQ10  | 42  | DQ42 | 89  | DQ19     | 90  | DQ51     | 137 | DQ31   | 138 | DQ63 |
| 43  | DQ11  | 44  | DQ43 | 91  | Vss      | 92  | Vss      | 139 | Vss    | 140 | Vss  |
| 45  | VCC   | 46  | VCC  | 93  | DQ20     | 94  | DQ52     | 141 | SDA    | 142 | SCL  |
| 47  | DQ12  | 48  | DQ44 | 95  | DQ21     | 96  | DQ53     | 143 | VCC    | 144 | VCC  |

## \*Pin Names

| Pin Name   | Function                    | Pin Name  | Function              |
|------------|-----------------------------|-----------|-----------------------|
| A0 ~ A11   | Address input (Multiplexed) | BA0 ~ BA1 | Select bank           |
| DQ0 ~ DQ63 | Data input/output           | CLK0      | Clock input           |
| CKE0       | Clock enable input          | /CS0      | Chip select input     |
| /RAS       | Row address strobe          | /CAS      | Column address strobe |
| /WE        | Write enable                | DQM0 ~ 7  | DQM                   |
| Vcc        | Power supply (3.3V)         | Vss       | Ground                |
| SDA        | Serial data I/O             | SCL       | Serial clock          |
| NC         | No connection               |           |                       |

FUNCTIONAL BLOCK DIAGRAM



**PIN FUNCTION DESCRIPTION**

| PIN        | NAME                   | INPUT FUNCTION  |
|------------|------------------------|---|
| CLK        | System clock           | Active on the positive going edge to sample all inputs.   |
| /CS        | Chip enable            | Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM  |
| CKE        | Clock enable           | Masks system clock to freeze operation from the next clock cycle.<br>CKE should be enabled at least one cycle prior to new command.<br>Disable input buffers for power down in standby.<br>CKE should be enabled 1CLK+tSS prior to valid command. |
| A0 ~ A11   | Address                | Row/column addresses are multiplexed on the same pins.<br>Row address : RA0 ~ RA11, Column address : CA0 ~ CA7  |
| BA0 ~ BA1  | Bank select address    | Selects bank to be activated during row address latch time.<br>Selects bank for read/write during column address latch time.  |
| /RAS       | Row address strobe     | Latches row addresses on the positive going edge of the CLK with RAS low.<br>Enables row access & precharge.  |
| /CAS       | Column address strobe  | Latches column addresses on the positive going edge of the CLK with CAS low.<br>Enables column access.  |
| /WE        | Write enable           | Enables write operation and row precharge.<br>Latches data in starting from CAS, WE active.   |
| DQM0 ~ 7   | Data input/output mask | Makes data output Hi-Z, tSHZ after the clock and masks the output.<br>Blocks data input when DQM active. (Byte masking)   |
| DQ0 ~ DQ63 | Data input/output      | Data inputs/outputs are multiplexed on the same pins.   |
| VDD/VSS    | Power supply/ground    | Power and ground for the input buffers and the core logic.  |

**ABSOLUTE MAXIMUM RATINGS**

| PARAMETER                             | SYMBOL        | RATING         |
|---------------------------------------|---------------|----------------|
| Voltage on Any Pin Relative to Vss    | $V_{IN\_OUT}$ | -1V to 4.6V    |
| Voltage on Vcc Supply Relative to Vss | VCC           | -1V to 4.6V    |
| Power Dissipation                     | $P_D$         | 4W             |
| Storage Temperature                   | $T_{STG}$     | -55°C to 150°C |
| Short Circuit Output Current          | $I_{OS}$      | 400mA          |

**Notes:**

Permanent device damage may occur if " Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC OPERATING CONDITIONS

(Recommended operating conditions (Voltage referenced to  $V_{SS} = 0V$ ,  $T_A = 0$  to  $70^{\circ}C$ ))

| PARAMETER             | SYMBOL   | MIN  | TYP. | MAX          | UNIT    | NOTE            |
|-----------------------|----------|------|------|--------------|---------|-----------------|
| Supply Voltage        | $V_{CC}$ | 3.0  | 3.3  | 3.6          | V       |                 |
| Input High Voltage    | $V_{IH}$ | 2.0  | 3.0  | $V_{CC}+0.3$ | V       | 1               |
| Input Low Voltage     | $V_{IL}$ | -0.3 | 0    | 0.8          | V       | 2               |
| Output High Voltage   | $V_{OH}$ | 2.4  | -    | -            | V       | $I_{OH} = -2mA$ |
| Output Low Voltage    | $V_{OL}$ | -    | -    | 0.4          | V       | $I_{OL} = 2mA$  |
| Input leakage current | $I_{LI}$ | -12  | -    | 12           | $\mu A$ | 3               |

### Notes :

- $V_{IH}$  (max) = 5.6V AC. The overshoot voltage duration is  $\leq 3ns$ .
- $V_{IL}$  (min) = -2.0V AC. The undershoot voltage duration is  $\leq 3ns$ .
- Any input  $0V \leq V_{IN} \leq V_{DDQ}$ .  
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

## CAPACITANCE

( $V_{CC} = 3.3V$ ,  $T_A = 23^{\circ}C$ ,  $f = 1MHz$ ,  $V_{REF} = 1.4V \pm 200 mV$ )

| DESCRIPTION                    | SYMBOL    | MIN | MAX | UNITS |
|--------------------------------|-----------|-----|-----|-------|
| Clock                          | $C_{CLK}$ | 10  | 16  | pF    |
| /RAS, /CAS, /WE, /CS, CKE, DQM | $C_{IN}$  | 10  | 20  | pF    |
| Address                        | $C_{ADD}$ | 10  | 20  | pF    |
| DQ (DQ0 ~ DQ63)                | $C_{OUT}$ | 16  | 26  | pF    |

## DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted,  $T_A = 0$  to  $70^{\circ}C$ )

| PARAMETER   | SYMBOL      | TEST<br>CONDITION  | VERSION |     |     |      | UNIT | NOTE |
|---|-------------|--|---------|-----|-----|------|------|------|
|   |             |  | -13     | -12 | -10 | -10L |      |      |
| Operating current<br>(One bank active)              | $I_{CC1}$   | Burst length = 1<br>$t_{RC} \geq t_{RC}(min)$<br>$I_O = 0mA$   | 440     | 440 | 400 | 400  | mA   | 1    |
| Precharge standby current in<br>power-down mode     | $I_{CC2P}$  | $CKE \leq V_{IL}(max)$<br>$t_{CC}=10ns$  | 4       |     |     |      | mA   |      |
|   | $I_{CC2PS}$ | $CKE \& CLK \leq V_{IL}(max)$<br>$t_{CC}=\infty$   | 4       |     |     |      | mA   |      |
| Precharge standby current in<br>non power-down mode | $I_{CC2N}$  | $CKE \geq V_{IH}(min)$<br>$CS^* \geq V_{IH}(min)$ , $t_{CC}=10ns$<br>Input signals are changed<br>one time during 20ns | 60      |     |     |      | mA   |      |

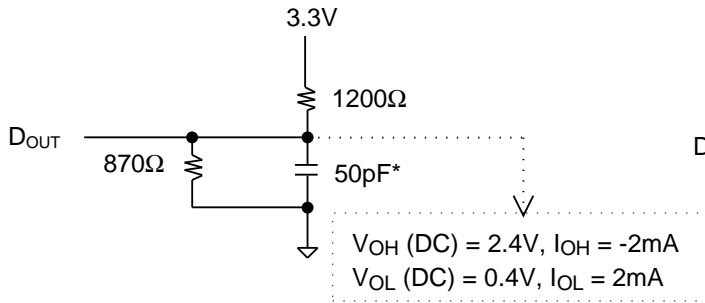
|   |             |   |     |     |     |     |    |   |
|---|-------------|---|-----|-----|-----|-----|----|---|
|   | $I_{CC2NS}$ | $CKE \geq V_{IH}(\min)$<br>$CLK \leq V_{IL}(\max), t_{CC}=\infty$<br>Input signals are stable                       | 24  |     |     |     |    |   |
| Active standby current in power-down mode                       | $I_{CC3P}$  | $CKE \leq V_{IL}(\max), t_{CC}=10ns$  | 12  |     |     |     | mA |   |
|   | $I_{CC3PS}$ | $CKE\&CLK \leq V_{IL}(\max)$<br>$t_{CC}=\infty$   | 12  |     |     |     |    |   |
| Active standby current in non power-down mode (One bank active) | $I_{CC3N}$  | $CKE \geq V_{IH}(\min),$<br>$CS^* \geq V_{IH}(\min), t_{CC}=10ns$<br>Input signals are changed one time during 20ns | 100 |     |     |     | mA |   |
|   | $I_{CC3NS}$ | $CKE \geq V_{IH}(\min)$<br>$CLK \leq V_{IL}(\max), t_{CC}=\infty$<br>Input signals are stable                       | 60  |     |     |     |    |   |
| Operating current (Burst mode)                                  | $I_{CC4}$   | $I_o = 0\text{ mA}$<br>Page burst<br>4Banks Activated<br>$t_{CCD} = 2CLKs$  | 540 | 520 | 440 | 440 | mA | 1 |
| Refresh current   | $I_{CC5}$   | $t_{RC} \geq t_{RC}(\min)$  | 540 | 520 | 440 | 440 | mA | 2 |
| Self refresh current  | $I_{CC6}$   | CKE $\leq 0.2V$   | 4   |     |     |     | mA |   |
|   |             |   | 1.6 |     |     |     | mA |   |

**Notes :**

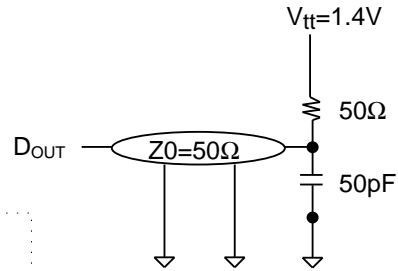
1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noticed, input swing level is CMOS( $V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}$ ).

**AC OPERATING TEST CONDITIONS**(vcc = 3.3V  $\pm$  0.3V, TA = 0 to 70°C)

| PARAMETER                                 | Value       | UNIT |
|---|-------------|------|
| AC Input levels (Vih/Vil)                 | 2.4/0.4     | V    |
| Input timing measurement reference level  | 1.4         | V    |
| Input rise and fall time                  | tr/tf = 1/1 | Ns   |
| Output timing measurement reference level | 1.4         | V    |
| Output load condition                     | See Fig. 2  |      |



(Fig. 1) DC output load



(Fig. 2) AC output load circuit

**OPERATING AC PARAMETER**

(AC operating conditions unless otherwise noted)

| PARAMETER                              | SYMBOL                | VERSION       |     |     |      | UNIT | NOTE |
|--|-----------------------|---------------|-----|-----|------|------|------|
|  |                       | -13           | -12 | -10 | -10L |      |      |
| Row active to row active delay         | $t_{RRD}(\text{min})$ | 15            | 16  | 20  | 20   | ns   | 1    |
| RAS to CAS delay                       | $t_{RP}(\text{min})$  | 20            | 20  | 20  | 20   | ns   | 1    |
| Row precharge time                     | $t_{RP}(\text{min})$  | 20            | 20  | 20  | 20   | ns   | 1    |
| Row active time                        | $t_{RAS}(\text{min})$ | 45            | 48  | 50  | 50   | ns   | 1    |
|  | $t_{RAS}(\text{max})$ | 100           |     |     |      | ns   |      |
| Row cycle time                         | $t_{RC}(\text{min})$  | 65            | 68  | 70  | 70   | ns   | 1    |
| Last data in to row precharge          | $t_{RDL}(\text{min})$ | 2             |     |     |      | CLK  | 2.5  |
| Last data in to Active delay           | $t_{DAL}(\text{min})$ | 2 CLK + 20 ns |     |     |      |      |      |
| Last data in to new col. address delay | $t_{CDL}(\text{min})$ | 1             |     |     |      | CLK  | 2    |
| Last data in to burst stop             | $t_{BDL}(\text{min})$ | 1             |     |     |      | CLK  | 2    |
| Col. address to col. address delay     | $t_{CCD}(\text{min})$ | 1             |     |     |      | CLK  | 3    |
| Number of valid output data            | CAS latency=3         | 2             |     |     |      | ea   | 4    |
|  | CAS latency=2         | -             |     | 1   |      |      |      |

**Notes :**

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

## AC CHARACTERISTICS

(AC operating conditions unless otherwise noted)

| PARAMETER                    |                  | SYMBO<br>L | -13 |      | -12 |      | -10 |      | -10L |      | UNIT | NOTE |
|------------------------------|------------------|------------|-----|------|-----|------|-----|------|------|------|------|------|
|                              |                  |            | MIN | MAX  | MIN | MAX  | MIN | MAX  | MIN  | MAX  |      |      |
| CLK cycle time               | CAS<br>latency=3 | $t_{CC}$   | 7.5 | 1000 | 8   | 1000 | 10  | 1000 | 10   | 1000 | ns   | 1    |
|                              | CAS<br>latency=2 |            | -   |      | -   |      | 10  |      | 12   |      |      |      |
| CLK to valid<br>output delay | CAS<br>latency=3 | $t_{SAC}$  |     | 5.4  |     | 6    |     | 6    |      | 6    | ns   | 1,2  |
|                              | CAS<br>latency=2 |            |     | -    |     | -    |     | 6    |      | 7    |      |      |
| Output data<br>hold time     | CAS<br>latency=3 | $t_{OH}$   | 2.7 |      | 3   |      | 3   |      | 3    |      | ns   | 2    |
|                              | CAS<br>latency=2 |            |     | -    |     | -    |     | 3    |      | 3    |      |      |
| CLK high pulse width         |                  | $t_{CH}$   | 2.5 |      | 3   |      | 3   |      | 3    |      | ns   | 3    |
| CLK low pulse width          |                  | $t_{CL}$   | 2.5 |      | 3   |      | 3   |      | 3    |      | ns   | 3    |
| Input setup time             |                  | $t_{SS}$   | 1.5 |      | 2   |      | 2   |      | 2    |      | ns   | 3    |
| Input hold time              |                  | $t_{SH}$   | 0.8 |      | 1   |      | 1   |      | 1    |      | ns   | 3    |
| CLK to output in Low-Z       |                  | $t_{SLZ}$  | 1   |      | 1   |      | 1   |      | 1    |      | ns   | 3    |
| CLK to output<br>in Hi-Z     | CAS<br>latency=3 | $t_{SHZ}$  |     | 5.4  |     | 6    |     | 6    |      | 6    | ns   | 2    |
|                              | CAS<br>latency=2 |            |     | -    |     | -    |     | 6    |      | 7    | ns   |      |

**Notes :**

- Parameters depend on programmed CAS latency.
- If clock rising time is longer than 1ns,  $(tr/2-0.5)ns$  should be added to the parameter.
- Assumed input rise and fall time ( $tr$  &  $tf$ ) = 1ns.  
If  $tr$  &  $tf$  is longer than 1ns, transient time compensation should be considered, ie.,  $[(tr + tf)/2-1]ns$  should be added to the parameter.



**SIMPLIFIED TRUTH TABLE**

| COMMAND                            |                        | CK E n-1 | CK E n | /C S | /R A S | /C A S | /W E | D Q M | BA 0,1  | A10/ AP     | A11 A9~A0                | NOTE |
|------------------------------------|------------------------|----------|--------|------|--------|--------|------|-------|---------|-------------|--------------------------|------|
| Register                           | Mode register set      | H        | X      | L    | L      | L      | L    | X     | OP code |             |                          | 1,2  |
| Refresh                            | Auto refresh           | H        | H      | L    | L      | L      | H    | X     | X       |             |                          | 3    |
|                                    | Self refresh           |          | Entry  |      |        |        |      |       |         |             |                          | L    |
|                                    |                        | Exit     | H      | L    | H      | H      | H    | X     | X       |             |                          | 3    |
|                                    | H                      |          |        | X    | X      | 3      |      |       |         |             |                          |      |
| Bank active & row addr.            |                        | H        | X      | L    | L      | H      | H    | X     | V       | Row address |                          |      |
| Read & column address              | Auto precharge disable | H        | X      | L    | H      | L      | H    | X     | V       | L           | Column Address (A0 ~ A7) | 4    |
|                                    | Auto precharge disable |          |        |      |        |        |      |       |         | H           |                          | 4,5  |
| Write & column address             | Auto precharge disable | H        | X      | L    | H      | L      | L    | X     | V       | L           | Column Address (A0 ~ A7) | 4    |
|                                    | Auto precharge disable |          |        |      |        |        |      |       |         | H           |                          | 4,5  |
| Burst Stop                         |                        | H        | X      | L    | L      | H      | L    | X     | X       |             |                          | 6    |
| Precharge                          | Bank selection         | H        | X      | L    | L      | H      | L    | X     | V       | L           | X                        |      |
|                                    | All banks              |          |        |      |        |        |      |       | X       | H           |                          |      |
| Clock suspend or active power down | Entry                  | H        | L      | H    | X      | X      | X    | X     | X       |             |                          |      |
|                                    |                        |          |        | L    | V      | V      | V    |       |         |             |                          |      |
| Exit                               | L                      | H        | X      | X    | X      | X      | X    | X     | X       |             |                          |      |
|                                    |                        |          |        |      |        |        |      |       |         |             |                          |      |
| Precharge power down mode          | Entry                  | H        | L      | H    | X      | X      | X    | X     | X       |             |                          |      |
|                                    |                        |          |        | L    | H      | H      | H    |       |         |             |                          |      |
|                                    | Exit                   | L        | H      | X    | X      | X      | X    | X     | X       |             |                          |      |
|                                    |                        |          |        |      |        |        |      |       |         |             |                          | L    |
| DQM                                |                        | H        | X      |      |        |        |      | V     | X       |             | 7                        |      |
| No operation command               |                        | H        | X      | H    | X      | X      | X    | X     | X       |             |                          |      |
|                                    |                        |          |        | L    | H      | H      | H    |       |         |             |                          |      |

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

**Notes :**

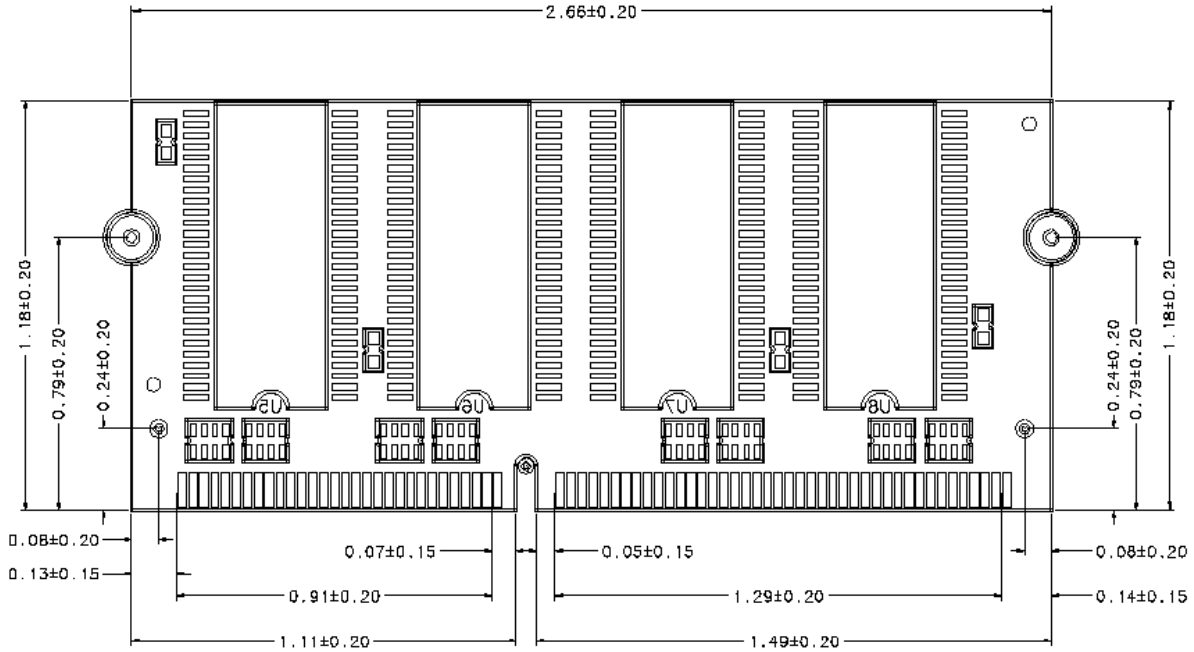
- OP Code : Operand code  
A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)
- MRS can be issued only at all banks precharge state.  
A new command can be issued after 2 CLK cycles of MRS.
- Auto refresh functions are as same as CBR refresh of DRAM.  
The automatical precharge without row precharge command is meant by "Auto".  
Auto/self refresh can be issued only at all banks precharge state.
- BA0 ~ BA1 : Bank select addresses.  
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.  
If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.  
If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.  
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.  
If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
- During burst read or write with auto precharge, new read/write command can not be issued.  
Another bank read/write command can be issued after the end of burst.  
New row active of the associated bank can be issued at tRP after the end of burst.
- Burst stop command is valid at every burst length.
- DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

**TIMING DIAGRAMS**

Please refer to attached timing diagram chart (II)

**PACKAGING INFORMATION**

Unit : Inch [mm]



PCB Thickness: 1.0mm (0.9t - 1.1t)

Immersion Gold PCB Pattern

**ORDERING INFORMATION**

| Part Number     | Density | Org.    | Package        | Ref. | Vcc  | MODE  | MAX.frq        |
|-----------------|---------|---------|----------------|------|------|-------|----------------|
| HSD4M64B4W-10   | 32MByte | 4M x 64 | 144 Pin-SODIMM | 4K   | 3.3V | SDRAM | CL2<br>100MHz  |
| HSD4M64B4W -10L | 32MByte | 4M x 64 | 144 Pin-SODIMM | 4K   | 3.3V | SDRAM | CL3<br>100MHz  |
| HSD4M64B4W -12  | 32MByte | 4M x 64 | 144 Pin-SODIMM | 4K   | 3.3V | SDRAM | CL3<br>125MHz  |
| HSD4M64B4W -13  | 32MByte | 4M x 64 | 144 Pin-SODIMM | 4K   | 3.3V | SDRAM | CL 3<br>133MHz |