82C431/82C432A/82C433/82C434A
CS8240: ENHANCED GRAPHICS CHIPSet™

- **100% hardware and software compatible to IBM™ Enhanced Graphics Adapter card**
- **Supports IBM Color Graphics and Monochrome adapters, and Hercules™ Graphics modes**
- **Bit mapped graphics in four planes**
- **640 × 350 resolution for IBM Enhanced Color Display**
- **Light pen interface**
- **Full 16 color support in 640 × 200 and 320 × 200 pixels for IBM Color Display**
- **Supports 720 × 350 pixels for IBM Monochrome Displays**
- **Supports 640 × 400 pixels for 400-line displays**
- **Soft scrolls, Pans and Windows through a 1M-pixels memory**
- **Supports 256K bytes of memory using 64K × 4 DRAMs**

The Enhanced Graphics CHIPSet offers a complete solution for implementing an IBM Enhanced Graphics Adapter compatible controller. The chip set provides a highly integrated solution, allowing a complete Enhanced Graphics control implementation using 32 chips, including 256K byte of display memory.

The chip set consists of the 82C431 Graphics Controller, 82C432A Sequencer, 82C433 Attributes Controller and 82C434A CRT Controller. The chip set supports color and monochrome direct drive displays in various modes. Other features include bit mapped graphics, light pen interface, and RAM loadable character generator. The chip set supports alphanumeric (AN) and all-points-addressable (APA) graphics modes, including all modes supported by the IBM Monochrome Display and Color/Graphics Adapters. Additionally, other modes provide 720 × 350 pixels support for the IBM Monochrome Display. It also provides full 16 color support for 320 × 200 pixel and 640 × 200 pixel resolutions for the IBM color display. The IBM Enhanced Color Display is supported with AN and APA graphics with a resolution of 640 × 400 (200-line double scan) mode for 400-line monitors.

The 82C432A and 82C434A are upgraded versions of 82C432 and 82C434 respectively. The 82C432A and 82C434A are fully compatible to the 82C432 and 82C434 respectively.

The 82C431 is packaged in 68-pin Plastic Leaded Chip Carrier (PLCC), 82C432A and 82C433 in 40-pin DIPs and 44-pin PFPs, and 82C434A in 84-pin PLCC.

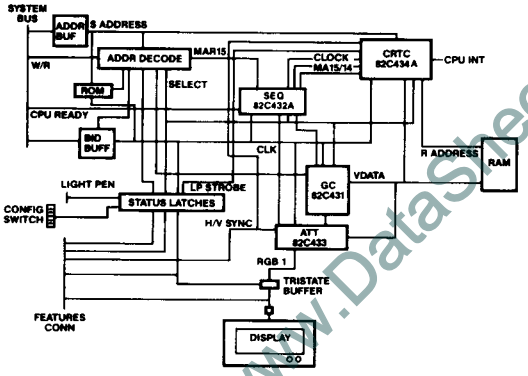
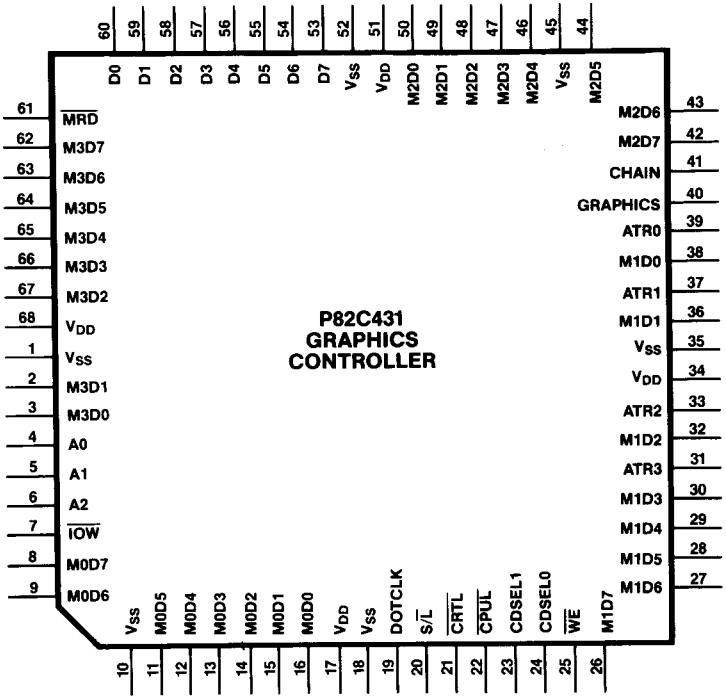
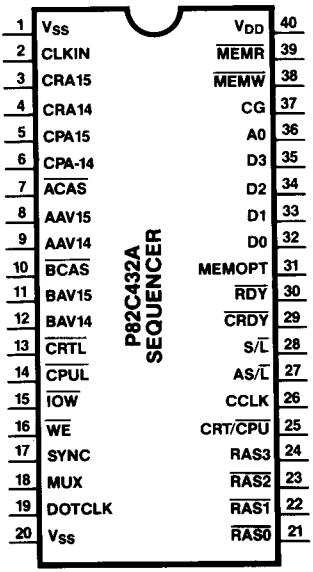
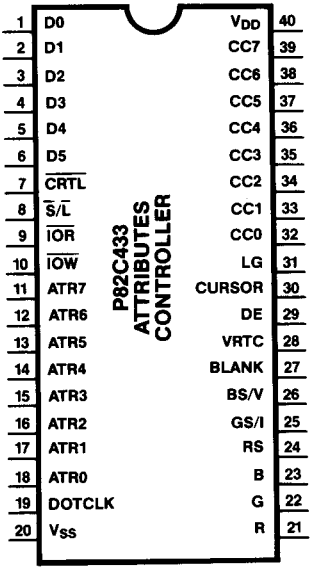
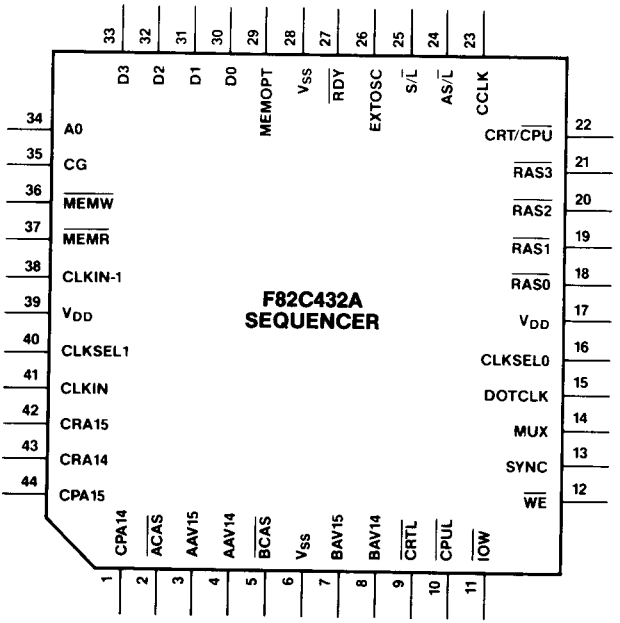


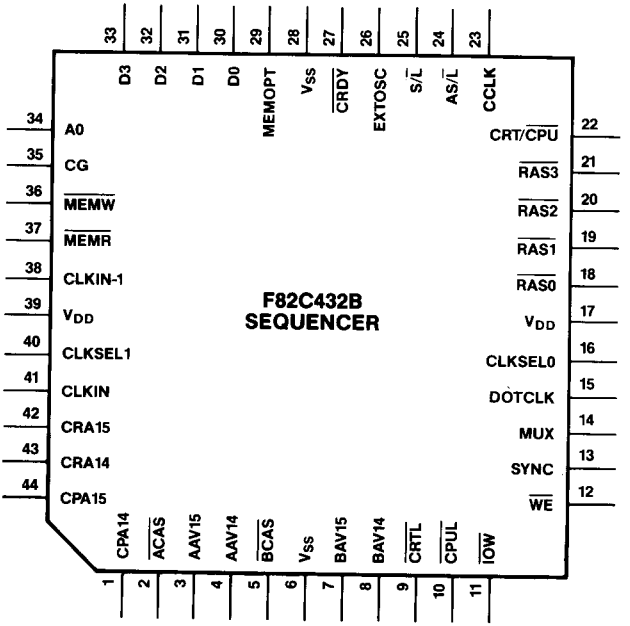
Figure 1. Enhanced Graphics Controller

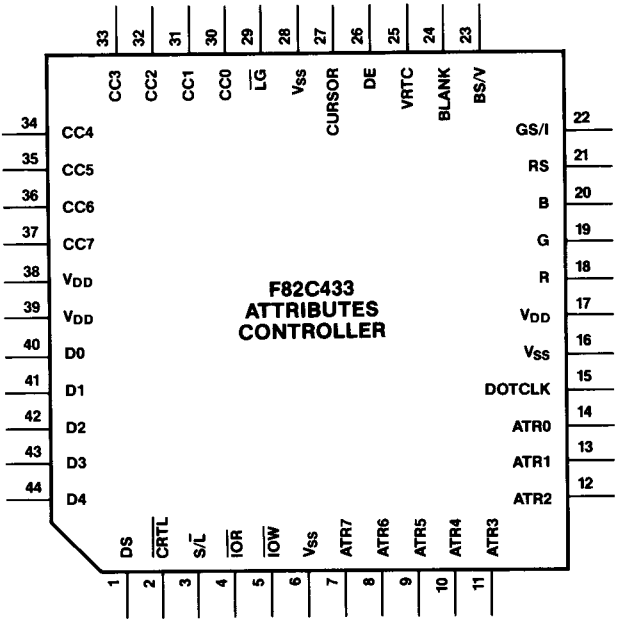

P82C431
GRAPHICS
CONTROLLER
1 VSS
2 M3D1
3 M3D0
4 A0
5 A1
6 A2
7 IOW
8 M0D7
9 M0D6
10 VSS
11 M0D5
12 M0D4
13 M0D3
14 M0D2
15 M0D1
16 M0D0
17 VDD
18 VSS
19 DOTCLK
20 S/L
21 CRTL
22 CPUL
23 CDSEL1
24 CDSEL0
25 WE
26 M1D7
27 M1D6
28 M1D5
29 M1D4
30 M1D3
31 M1D2
32 ATR3
33 M1D1
34 ATR2
35 VDD
36 VSS
37 M1D1
38 ATR1
39 M1D0
40 ATR0
41 GRAPHICS
42 CHAIN
43 M2D7
44 M2D6
45 M2D5
46 VSS
47 M2D4
48 M2D3
49 M2D2
50 M2D1
51 M2D0
52 VDD
53 VSS
54 D7
55 D6
56 D5
57 D4
58 D3
59 D2
60 D1
61 D0
62 MRD
63 M3D7
64 M3D6
65 M3D5
66 M3D4
67 M3D3
68 M3D2

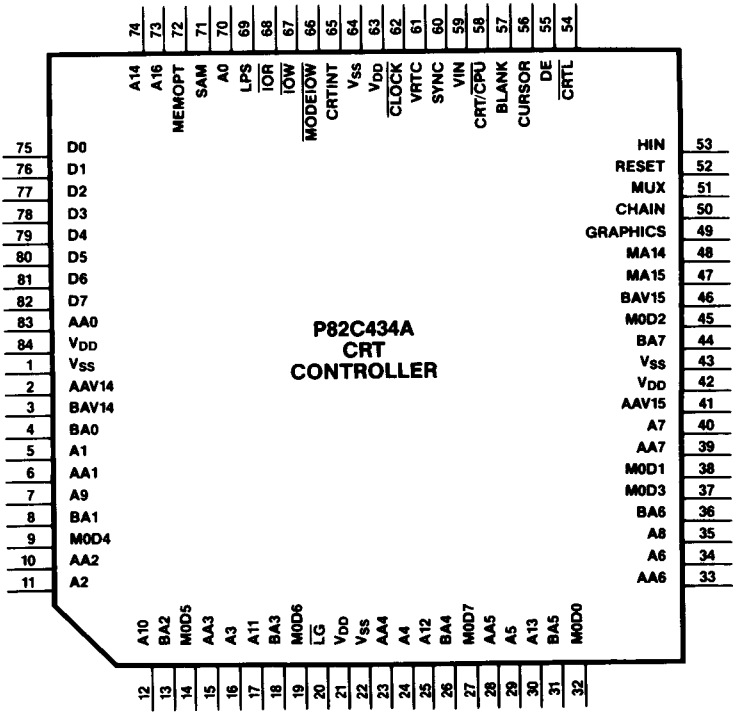

P82C432A
SEQUENCER
1 VSS
2 CLKIN
3 CRA15
4 CRA14
5 CPA15
6 CPA-14
7 ACAS
8 AAV15
9 AAV14
10 BCAS
11 BAV15
12 BAV14
13 CRTL
14 CPUL
15 IOW
16 WE
17 SYNC
18 MUX
19 DOTCLK
20 VSS
21 RAS0
22 RAS1
23 RAS2
24 RAS3
25 CRT/CPU
26 CCLK
27 AS/L
28 S/L
29 CRDY
30 RDY
31 MEMOPT
32 D0
33 D1
34 D2
35 D3
36 A0
37 CG
38 MEMW
39 MEMR
40 VDD


P82C433
ATTRIBUTES
CONTROLLER
1 D0
2 D1
3 D2
4 D3
5 D4
6 D5
7 CRTL
8 S/L
9 IOR
10 IOW
11 ATR7
12 ATR6
13 ATR5
14 ATR4
15 ATR3
16 ATR2
17 ATR1
18 ATR0
19 DOTCLK
20 VSS
21 R
22 G
23 B
24 RS
25 GS/I
26 BS/V
27 BLANK
28 VRTC
29 DE
30 CURSOR
31 LG
32 CC0
33 CC1
34 CC2
35 CC3
36 CC4
37 CC5
38 CC6
39 CC7
40 VDD


F82C432A
SEQUENCER
1 CPA14
2 ACAS
3 AAV15
4 AAV14
5 BCAS
6 VSS
7 BAV15
8 BAV14
9 CRTL
10 CPUL
11 IOW
12 WE
13 SYNC
14 MUX
15 DOTCLK
16 CLKSEL0
17 VDD
18 RAS0
19 RAS1
20 RAS2
21 RAS3
22 CRT/CPU
23 CCLK
24 AS/L
25 S/L
26 EXTOSC
27 RDY
28 VSS
29 MEMOPT
30 D0
31 D1
32 D2
33 D3
34 A0
35 CG
36 MEMW
37 MEMR
38 CLKIN-1
39 VDD
40 CLKSEL1
41 CLKIN
42 CRA15
43 CRA14
44 CPA15


F82C432B
SEQUENCER
1 CPA14
2 ACAS
3 AAV15
4 AAV14
5 BCAS
6 VSS
7 BAV15
8 BAV14
9 CRTL
10 CPUL
11 IOW
12 WE
13 SYNC
14 MUX
15 DOTCLK
16 CLKSEL0
17 VDD
18 RAS0
19 RAS1
20 RAS2
21 RAS3
22 CRT/CPU
23 CCLK
24 AS/L
25 S/L
26 EXTOSC
27 CRDY
28 VSS
29 MEMOPT
30 D0
31 D1
32 D2
33 D3
34 A0
35 CG
36 MEMW
37 MEMR
38 CLKIN-1
39 VDD
40 CLKSEL1
41 CLKIN
42 CRA15
43 CRA14
44 CPA15


F82C433
ATTRIBUTES
CONTROLLER
1 DS
2 CRTL
3 S/L
4 IOR
5 IOW
6 VSS
7 ATR7
8 ATR6
9 ATR5
10 ATR4
11 ATR3
12 ATR2
13 ATR1
14 ATR0
15 DOTCLK
16 VSS
17 VDD
18 R
19 G
20 B
21 RS
22 GS/I
23 BS/V
24 BLANK
25 VRTC
26 DE
27 CURSOR
28 VSS
29 LG
30 CC0
31 CC1
32 CC2
33 CC3
34 CC4
35 CC5
36 CC6
37 CC7
38 VDD
39 VDD
40 D0
41 D1
42 D2
43 D3
44 D4


P82C434A
CRT
CONTROLLER
1 VSS
2 AAV14
3 BAV14
4 BA0
5 A1
6 AA1
7 A9
8 BA1
9 M0D4
10 AA2
11 A2
12 A10
13 BA2
14 M0D5
15 AA3
16 A3
17 A11
18 BA3
19 M0D6
20 LG
21 VDD
22 VSS
23 AA4
24 A4
25 A12
26 BA4
27 M0D7
28 AA5
29 A5
30 A13
31 BA5
32 M0D0
33 AA6
34 A6
35 A8
36 BA6
37 M0D3
38 M0D1
39 AA7
40 A7
41 AAV15
42 VDD
43 VSS
44 BA7
45 M0D2
46 BAV15
47 MA15
48 MA14
49 GRAPHICS
50 CHAIN
51 MUX
52 RESET
53 HIN
54 CRTL
55 DE
56 CURSOR
57 BLANK
58 CRT/CPU
59 VIN
60 SYNC
61 VRTC
62 CLOCK
63 VDD
64 VSS
65 CRTINT
66 MODEIOW
67 IOW
68 IOR
69 LPS
70 A0
71 SAM
72 MEMOPT
73 A16
74 A14
75 D0
76 D1
77 D2
78 D3
79 D4
80 D5
81 D6
82 D7
83 AA0
84 VDD

82C431 Pin Description

Pin No.	Pin Type	Symbol	Description
60-53	I/O	D0-D7	CPU data bus pins are bidirectional tri-state signals. They are used to load data into the 82C431. The data bus is also used to send/receive data to/from the display memory.
16-11, 9-8	I/O	M0D0-M0D7	Memory data buses M0D0-M0D7, M1D0-M1D7, M2D0-M2D7 and M3D0-M3D7 are memory data buses used to send and receive data to/from the display memory. These buses are bidirectional tri-state pins.
38, 36, 32, 30-26		M1D0-M1D7	
50-46, 44-42		M2D0-M2D7	
3, 2, 67-62		M3D0-M3D7	
22	I	$\overline{\text{CPUL}}$	CPU Latch is active low input. It is generated by the 82C432A Sequencer. When active the display memory data will be read into the graphics controller. The low-to-high going edge of this signal along with $\overline{\text{MRD}}$ active will output the data onto the data bus D0-D7 for a CPU memory read operation.
21	I	$\overline{\text{CRTL}}$	CRT Latch is an active low input. It is generated by the 82C432A Sequencer. When active the display memory graphics data will be loaded into the graphics controller on the low-to-high going edge. The data on the display memory should meet the set up and hold requirements. The data loaded is transferred into the Shifter register when S/$\overline{\text{L}}$ is low.
19	I	DOTCLK	Dot Clock is used by the graphics controller to shift the data in the Shifter register.
20	I	S/$\overline{\text{L}}$	Shift or Load input serves dual functions. It is generated by the 82C432A Sequencer. When low, the display memory data will be loaded into the Shifter. When high, it will shift the data in the Shifter by one bit.
25	I	$\overline{\text{WE}}$	Write Enable is an active low input. When it is active , the display memory data is output on the M0D0-D7, M1D1-D7, M2D0-D7 and M3D0-D7 data buses. When $\overline{\text{WE}}$ is high, these data buses are tri-stated.
7	I	$\overline{\text{IOW}}$	I/O Write is an active low input. It is used to load internal registers of the graphics controller by the CPU. The address and data setup and hold times must be met in order to write data into the internal registers.
61	I	$\overline{\text{MRD}}$	Memory Read is an active low input. It is used by the CPU to read display memory data in conjunction with the high going edge of the $\overline{\text{CPUL}}$ input.

82C431 Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Description
4-6	I	A0-A2	Address signals A0, A1 and A2 are used by CPU to select the internal registers of the graphic controller.
40 41 24-23	O O O	GRAPHICS CHAIN CDSEL0-1	Graphics, Chain, CDSEL0 and CDSEL1 are outputs of the Miscellaneous register. They can be tri-stated by setting the Mode register bit 2 to logical 1. Graphics & Chain outputs are used to multiplex the address buses in the 82C434A CRT Controller. CDSEL0 and CDSEL1 outputs control the mapping of the display memory.
39, 37 33, 31	O	ATR0-ATR3	Attributes 0-3 are used to transfer the output of the Shifter register to the 82C433 Attributes Controller in the graphics mode. In the alphanumeric mode, ATR0-ATR3 transfer the data on the M1D0-M1D3 to the Attributes Controller.
1, 10, 18 35, 45, 52	—	V_{SS}	Ground.
68, 17, 34, 51	—	V_{DD}	5 Volt Power Supply.

82C432A Pin Description

Pin No.	Pin Type	Symbol	Description
2	I	CLKIN	Clock In is the input clock. It is the primary clock source for the chip. The output Dot Clock is of the same frequency as the CLKIN frequency.
36	I	A0	Address 0 is the address 0 of the CPU address bus. It is used to select between the index register and the control registers on the device. It is also used to write into even/odd memory planes.
32-35	I	D0-D3	D0-D3 are low order data bus bits. They are used to load the Sequencer registers.
4,3	I	CRA14,15	CRA14 and CRA15 are the high order address bits for the CRT display read. These bits are generated by the 82C434A CRT Controller.
6,5	I	CPA14,15	CPA14 and CPA15 are the high order address bits for the CPU read/write operations. CPA14 is bit 14 of the CPU address bus. CPA15 is the decoded signal from the CPU address bus signals A13-A19. During memory read and write cycles, AAV14 = BAV14 = CPA14, and AAV15 = BAV15 = CPA15.
37	I	CG	CG is the Character Generator bit from the display memory. It is the attribute bit 3. It is used to select between the character maps A and B.
39,38	I	$\overline{\text{MEMR}}$ $\overline{\text{MEMW}}$	Memory Read and Memory Write are active low inputs. These inputs are used by the processor to read from and write into the display memory.
15	I	$\overline{\text{IOW}}$	I/O Write is the control signal from the system bus. It is used to load the various registers on the Sequencer.
31	I	MEMOPT	Memory Option is the control signal used to select 64K or 256K byte memory configurations as follows: MEMOPT — Memory Configuration 0 — 256K Bytes 1 — 64K Bytes
17	I	SYNC	Sync is generated by the 82C434A CRT Controller. It is used to disable the AS/$\overline{\text{L}}$ (Address Strobe/Load) signal during non-active display periods.
21-24	O	$\overline{\text{RAS0}}$- $\overline{\text{RAS3}}$	$\overline{\text{RAS0}}$-$\overline{\text{RAS3}}$ are the Row Access Strobe signals for the four memory planes.
7,10	O	$\overline{\text{ACAS}}$ $\overline{\text{BCAS}}$	$\overline{\text{ACAS}}$ and $\overline{\text{BCAS}}$ are the Column Access Strobe signals for the memory planes.
9, 8, 12, 11	O	AAV14, AAV15, BAV14, BAV15	AAV14, AAV15, BAV14 and BAV15 are high order active high signals for the two memory maps. During memory read and write cycles, AAV14 = BAV14 = CPA14, and AAV15 = BAV15 = CPA15.

82C432A Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Description
13	O	$\overline{\text{CRTL}}$	CRT LATCH is an active low signal. It is used to latch the memory data into the 82C431 Graphics Controller, and the 82C433 Attributes Controller, for CRT display read cycles.
14	O	$\overline{\text{CPUL}}$	CPU LATCH is an active low signal. It is used to load memory data into the Graphics Controller 82C431, for CPU memory read cycles.
16	O	$\overline{\text{WE}}$	Write Enable is an active low signal used to enable the CPU to write into the display memory.
18	O	MUX	MULTIPLEXER output is used to multiplex the RAS and CAS signals.
19	O	DOTCLK	Dot Clock output is used by the 82C431 Graphics Controller and by the 82C433 Attributes Controller.
26	O	CCLK	Character Clock is an active high signal. It is used by the 82C434A CRT Controller.
28	O	S/$\overline{\text{L}}$	Shift/$\overline{\text{Load}}$ output is used to load display memory graphics data into the 82C431 Graphics Controller.
27	O	AS/$\overline{\text{L}}$	Attributes Shift/$\overline{\text{Load}}$ signal is used to load alpha-numeric display memory data into the 82C433 Attributes Controller.
25	O	CRT/$\overline{\text{CPU}}$	CRT/$\overline{\text{CPU}}$ control signal is used by the 82C434A CRT Controller to enable either the CRT read address or the CPU read/write address.
30	O	$\overline{\text{RDY}}$	Ready is an active low output. It is used by the CPU to indicate that a data transfer will be completed. It becomes inactive as soon as the memory read or write operation is completed. $\overline{\text{RDY}}$ acts as an enable input for a tri-state driver which drives the CPU Ready input.
29	O	$\overline{\text{CRDY}}$	$\overline{\text{CReady}}$ is similar to the $\overline{\text{RDY}}$ output. The difference between the two signals is the way they go inactive (high). The $\overline{\text{RDY}}$ when inactive goes high and stays high. The $\overline{\text{CRDY}}$ when inactive goes high for one dot clock period, and then goes tri-state. $\overline{\text{CRDY}}$ can directly drive the CPU Ready input.
1,20	—	V_{SS}	Ground.
40	—	V_{DD}	5 Volt Power Supply.

82C433 Pin Description

Pin No.	Pin Type	Symbol	Description
32-39	I	CC0-CC7	CC0-CC7 are the 8 Condition Code inputs coming directly from the display memory (plane 2). These 8 inputs are loaded into a parallel-to-serial shift register. The output of this shift register enables either ATR0-3 (CC=1), or ATR4-7 (CC=0) to address the color palette.
11-14	I	ATR7-ATR4	ATR7-ATR4 are the 4 high order attributes bits for alphanumeric data coming directly from the display memory (plane 1). The proper Condition Code bit chooses between ATR7-4 and ATR3-0.
15-18	I	ATR3-ATR0	ATR3-ATR0 are the 4 low order attributes bits. They could either be graphics data, in which case they come from the 82C431 Graphics Controller or alphanumeric data, in which case they come from the display memory multiplexed through the Graphics Controller along with the graphics data. The Graphics Controller decides whether the incoming data is graphic or alphanumeric.
1-6	I/O I I I/O I/O I/O	D0 D1 D2 D3 D4 D5	D0-D5 are the 6 data bus signals. Four of these D5, D4, D3 and D0 are bidirectional while the other two, D2 and D1 are inputs only. The 4 bidirectional pins when read, output the following 4 status bits: D5: Color palette bit 1, D4: Color palette bit 0, D3: VRTC (Vertical retrace), D0: DE (Display Enable). Bits D5 and D4 are controlled by the Color Plane Enable register bits 5, 4. Bits D3 and D0 are generated by the 82C434A CRT Controller.
9	I	$\overline{IOR}$	I/O Read is an active low signal. This signal has the dual purpose of reading the status, as well as clearing the address/data flip-flop.
10	I	$\overline{IOW}$	I/O Write is an active low signal. It loads either the address register, one of the 16 color palette registers, or one of the 4 control registers.
19	I	DOTCLK	Dot Clock is the active high clock generated by the 82C432A Sequencer.
7	I	$\overline{CRTL}$	$\overline{CRT\ Latch}$ is an active low signal. It is used to load display memory data into the 82C433. It is generated by the 82C432A Sequencer.
8	I	S/$\overline{L}$	S/$\overline{L}$ is the Shift/Load signal to load display memory data into the 82C433. It is generated by the 82C432A Sequencer as AS/$\overline{L}$ signal.

82C433 Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Description
27	I	BLANK	BLANK is the Blank output from the 82C434A CRT Controller. It is low during the time the monitor is displaying data.
28	I	VRTC	VRTC is the Vertical Retrace output from the 82C434A CRT Controller. It is used by an internal 5 bit counter (divide by 32) to generate the blink clock required by blinking displays. The blink clock is ON for 16 VRTC periods and OFF for 16 VRTC periods. It is output on the data bus bit D3 as a status bit.
29	I	DE	DE is the active high Display Enable output from the 82C434A CRT Controller. It is used for enabling the display area on the screen. When the DE and Blank signals are inactive at the same time, the border is displayed on the monitor. It is output on data bus bit D0 as a status bit.
30	I	CURSOR	CURSOR is an active high signal. It provides two functions: 1. During DE active time it indicates a valid cursor position. 2. If Cursor is active during the high-to-low edge of Blank, it indicates that the contents of the CRT Controller Underline Location register (R14) are equal to the line count (contents of the Raster Counter).
31	I	$\overline{LG}$	Line Graphics is an active low input from the CRT Controller. It is a logical NAND of M0D5, M0D6 and M0D7 (bits 5, 6 and 7 of plane 0 in display memory).
21-26	O	R, G, B RS, GS/I, BS/V	R, G, B, RS, GS/I, BS/V are the 6 outputs that drive the monochrome or color monitor. R, G, B are the Red, Green, and Blue signals.The RS, GS/I, and BS/V are the Secondary Red, Secondary Green/Intensity, Secondary Blue/Monochrome Video (display) signals.
40	—	V_{DD}	5 Volt Power Supply.
20	—	V_{SS}	Ground.

82C434A Pin Description

Pin No.	Pin Type	Symbol	Description
70	I	A0	CPU Address bits 0-14 and 16. They are used to generate addresses for the display memory.
5	I	A1	
11	I	A2	
16	I	A3	
24	I	A4	
29	I	A5	
34	I	A6	
40	I	A7	
35	I	A8	
7	I	A9	
12	I	A10	
17	I	A11	
25	I	A12	
30	I	A13	
74	I	A14	
73	I	A16	
75-82	I/O	D0-D7	CPU Data Bus bits 0-7. They are used to transfer data to and from the CPU data bus.
83	O	AA0	Address bus AA0-7 for memory planes 0 and 1.
6	O	AA1	
10	O	AA2	
15	O	AA3	
23	O	AA4	
28	O	AA5	
33	O	AA6	
39	O	AA7	
4	O	BA0	Address Bus BA0-7 for memory planes 2 and 3.
8	O	BA1	
13	O	BA2	
18	O	BA3	
26	O	BA4	
31	O	BA5	
36	O	BA6	
44	O	BA7	
2,41	I	AAV14, AAV15	High address bits 14 and 15 for the A address bus. They are generated by the 82C432A Sequencer.
3,46	I	BAV14, BAV15	High address bits 14 and 15 for the B address bus. They are generated by the 82C432A Sequencer.
48,47	O	MA14, MA15	Address bits 14, 15 is used by the 82C432A Sequencer to generate the high order address bits AAV14, AAV15, BAV14 and BAV15. These bits can be tri-stated through Mode Control register R17.
20	O	$\overline{LG}$	Line Graphics is an active low output. It is used by the 82C433 Attributes Controller.

82C434A Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Description
50	I	CHAIN	CHAIN is a select input. It is generated by the 82C431 Graphics Controller. It is used with the SAM and MEMOPT inputs to select the LSB of the CPU address.
49	I	GRAPHICS	GRAPHICS is an active low input. It is generated by the 82C431 Graphics Controller. It is used to change RAM BA addresses from graphics to text mode.
51	I	MUX	MULTIPLEXER input is used to multiplex the RAS and CAS address control. MUX is generated by the 82C432A Sequencer.
52	I	RESET	RESET initializes the CRT Controller as follows: a. It initializes the horizontal and vertical polarity control to logical 0. b. Mode register bits 4,7 are reset. c. All counters in the CRT Controller are reset. d. Address register bits 3,4 are reset. e. PGSEL is reset to logical 0. All other control registers remain unchanged. RESET must be active for at least 5 dot clocks.
54	I	$\overline{\text{CRTL}}$	CRT Latch is an active low input. It latches M0D0-M0D7 data. It is generated by the 82C432A Sequencer.
55	O	DE	Display Enable is an active high output. It enables the display areas on the screen. When DE and Blank signals are inactive at the same time, the border is displayed on the monitor.
56	O	CURSOR	CURSOR serves dual functions. It indicates a valid cursor position when DE is active. In the other case if CURSOR is active during the trailing edge of Blank signal, it signifies that the contents of the Underline Location register R14 are equal to the line count (contents of Raster Count register).
57	O	BLANK	BLANK is an active high output for blanking the screen during retrace periods.
58	I	CRT/$\overline{\text{CPU}}$	CRT/$\overline{\text{CPU}}$ is used by the CRT Controller to enable the CRT read address when CRT/$\overline{\text{CPU}}$ = 1. When CRT/$\overline{\text{CPU}}$ = 0, the CPU read or write address is enabled.
53	O	HIN	HIN is horizontal sync output. It is active high if horizontal polarity bit HPOL is low. It is active low if HPOL is high. HPOL is programmed through MODEIOW register. This signal is identical to the HPOL bit of the MISCELLANEOUS output register located in the Graphics Controller.

82C434A Pin Description
(Continued)

Pin No.	Pin Type	Symbol	Description
59	O	VIN	VIN is vertical sync output. Like the HIN signal, VIN polarity is also controlled by VPOL. VPOL is programmed through the MODEIOW register. This signal is identical to the VPOL bit of the MISCELLANEOUS output register.
60	O	SYNC	SYNC is an active high output used by the Sequencer 82C432A to control the AS/$\overline{L}$ output.
61	O	VRTC	VERTICAL SYNC is active high vertical retrace signal. it is used by the 82C433 Attributes Controller, to generate the blink clock required by the blinking displays.
62	I	$\overline{\text{CLOCK}}$	CLOCK is used to synchronize all the functions for the device except the bus interface. The active transition is high to low. It is the $\overline{\text{CCLK}}$ (Character Clock) output from the 82C432A Sequencer.
65	O	CRTINT	CRT INTERRUPT is an active high output. It is the frame interrupt generated by the 82C434A. It is enabled by bit 5 of the Vertical Retrace End register. It can be cleared by programming bit 4 of Vertical Retrace End register to 0. When not active, the CRTINT output is in a tri-state condition.
66	I	$\overline{\text{MODEIOW}}$	$\overline{\text{MODEIOW}}$ is used to program the MODEIOW register bits D5 (PGSEL), D6 (HPOL) and D7 (VPOL). The MODEIOW register is cleared by a chip reset.
67	I	$\overline{\text{IOW}}$	I/O WRITE is an active low input. It is used to write to the 82C434A registers.
68	I	$\overline{\text{IOR}}$	I/O READ is an active low input. It is used to read the 82C434A registers.
69	I	LPS	LIGHT PEN STROBE is used to latch the current refresh address in the light pen register. The address is latched on a low-to-high transition on this input.
71	I	SAM	SAM is used with MEMOPT and CHAIN to select LSB of the CPU address.
72	I	MEMOPT	MEMORY OPTION is used with SAM and CHAIN to select the LSB of CPU address. When MEMOPT is low, there are 256K Bytes of display memory configured. When MEMOPT is high, 64K Bytes of display memory is configured.
32,38 45,37 9,14 19,27	I	MD0,1 MD2,3 MD4,5 MD6,7	Memory Data Bus 0-7 are the character data bits.
1,22,43,64	—	V_{SS}	Ground.
21,42,63,84	—	V_{DD}	5 Volt Power Supply.

Flat Pack Package Options

The 82C432 Sequencer and 82C433 Attributes controller are also available in Plastic Flat-Pack (PFP) packages. The pin diagrams on pages 3-4 describe the pin assignments. Most of the pins on the PFP packages are the same as for 40-pin DIP packages. The differences between the DIP and PFP packages are described here.

F82C432A:

The F82C432A features an option to select input clock source from three sources: CLKIN, CLKIN-1 and EXT-OSC. The CLKIN and CLKIN-1 can be clock inputs of 14.318 MHz and 16.257 MHz respectively. Alternatively, a user defined EXT-OSC input clock source can also be selected. CLKSEL0 and CLKSEL1 inputs are used to select the clock input source.

CLKSEL0	CLKSEL1	Clock Source
0	0	CLKIN
0	1	CLKIN-1
1	0	EXT-OSC
1	1	ILLEGAL

The CLKSEL0 and CLKSEL1 inputs must be pulled high or low (as desired) for proper operation of the device.

The F82C432A also has only one Ready signal output, $\overline{RDY}$. Note that $\overline{CRDY}$ output is not bonded out on the F82C432A.

F82C432B:

The F82C432B is similar to F82C432A in all respects except for the ready output. In this package, $\overline{CRDY}$ is bonded out as an output. Note that $\overline{RDY}$ is not bonded out on this package. The differences between the $\overline{RDY}$ and $\overline{CRDY}$ signals are described under pin description for 82C432A. The CLKSEL0, CLKSEL1, CLKIN, CLKIN-1 and EXTOSC inputs operate exactly the same way as for F82C432A.

Note that CLKSEL0, CLKSEL1 and CLKIN-1 and EXTOSC inputs are not available on the 40-pin DIP packages. The inputs on CLKIN, CLKIN-1 and EXTOSC must meet the electrical specifications as described under D.C. and A.C. characteristics for 82C432A.

F82C433:

The F82C433 is the Plastic Flat Pack (PFP) package available for the Attributes controller. The input-output signals for the F82C433 are exactly the same as for the 40-pin DIP package. The pin diagram on page 4 describes the pin assignment for this package.

82C431 Functional Description

The 82C431 Graphics Controller is responsible for directing data from the display memory to the 82C433 Attributes Controller and the CPU. The 82C431 operates in two basic modes: Alphanumeric and Graphics. In the Alphanumeric Mode, the data is sent in parallel mode through the Graphics Controller directly to the 82C433 Attributes Controller. In the Graphics Mode, memory data is sent in serial mode to the 82C433 Attributes Controller. Figures 2 and 3 illustrate a typical write and read process for Graphics Controller.

The 82C431 formats the data for use in various compatible modes. The controller also provides color comparators which can be used in color painting modes. Data can be written to the display memory planes in 32 bit words to expedite fast color presetting of the display areas on the monitor. Logical functions on the chip allows for manipulation of the data before being written to the display memory.

The Graphics Controller has basically two major sections, Graphics A and Graphics B. The Graphics A writes to the display memory planes 0 and 1, and the Graphics B writes to the memory planes 2 and 3. The following description will refer to these two sections as Graphics A and Graphics B.

82C431 Graphics Controller Register Summary

Register Number	Register Name	Pointer Value in Hex
—	Graphics A Position	—
—	Graphics B Position	—
—	Address Register	—
R0	Set/Reset	00
R1	Enable Set/Reset	01
R2	Color Compare	02
R3	Data Rotate	03
R4	Read Map Select	04
R5	Mode Register	05
R6	Miscellaneous	06
R7	Color Don't Care	07
R8	Bit Mask	08

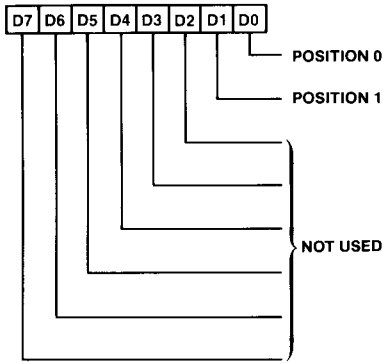
82C431 Internal Registers

82C431 internal registers are selected through address inputs A0-A2. The following table describes the addressing scheme:

A2	A1	A0	Register selected
1	0	0	Graphics A Position
0	1	0	Graphics B Position
1	1	0	Graphics Address register
1	1	1	Registers pointed to by Graphics Address register

Graphics A Position Register:

The Graphics A Position register is a write-only register. This register must be programmed to 0 to select Graphics A for the data bus input and output operations. Graphics A operates on the display memory planes 0 and 1, while the Graphics B operates on the display memory planes 2 and 3. CPU data bus signals D0 and D1 should be directed to Graphics A. D2 and D3 should be directed to Graphics B.



Graphics B Position Register:

The Graphics B Position register is a write-only register. This register must be programmed to 1 to select Graphics B for the data bus input and output operations. Graphics B operates on the display memory planes 2 and 3, while the Graphics A operates on the display memory planes 0 and 1. CPU data bus signals D0 and D1 should be directed to Graphics A. D2 and D3 should be directed to Graphics B.

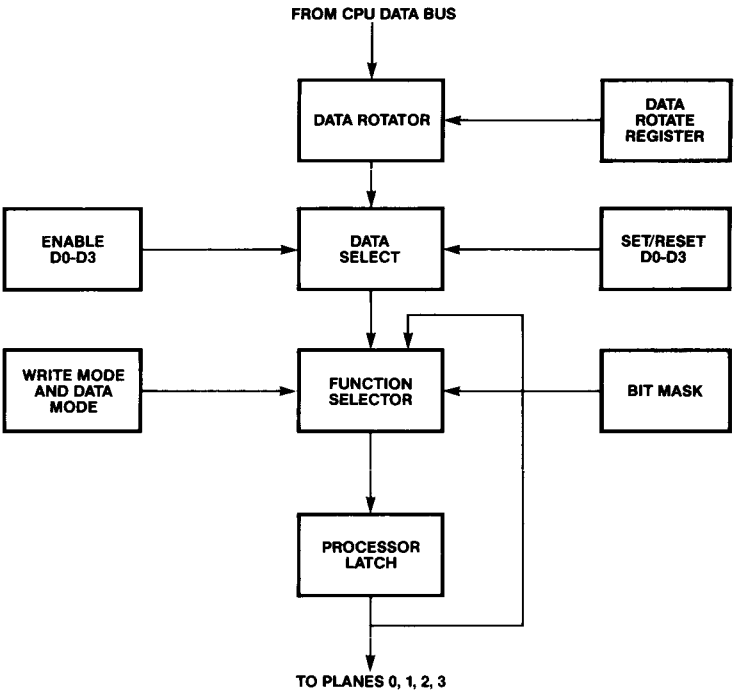


Figure 2. 82C431 Write Process

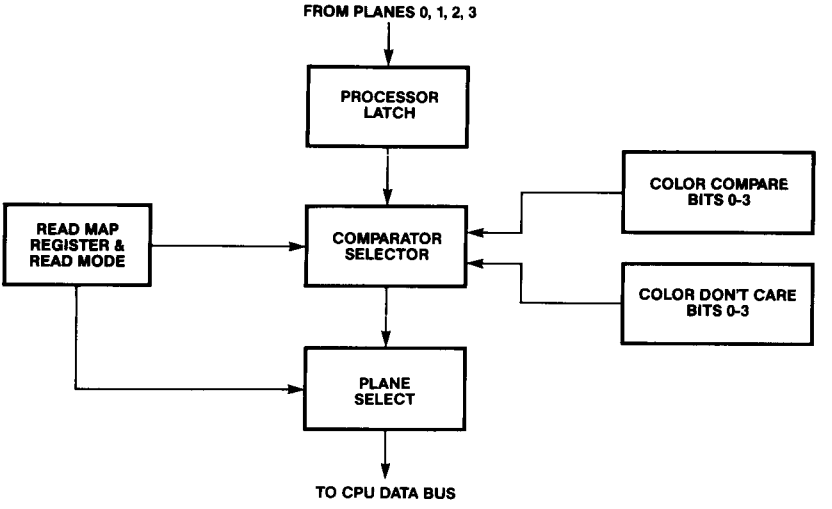
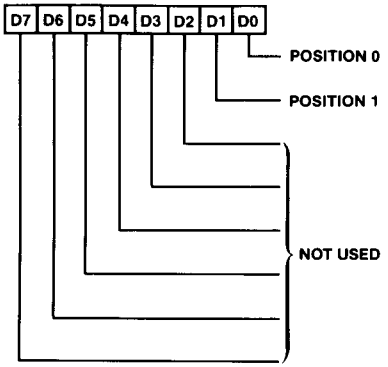
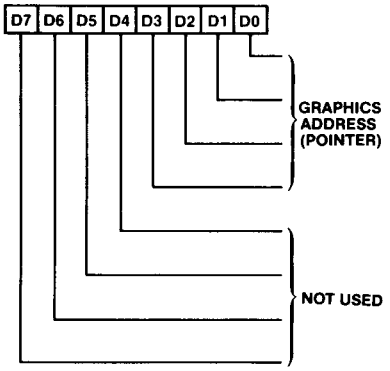


Figure 3. 82C431 Read Process



Graphics Address Register:

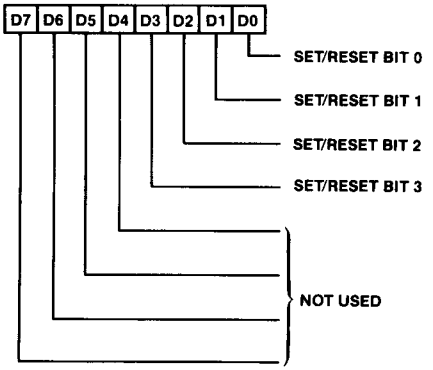
The Graphics Address register is used to point to other internal registers of the 82C431. The four least significant bits determine the register which will be pointed to in the next register write operation. In order to write to the registers selected by the pointer in this register, the position registers A and B should be programmed with 0 and 1, respectively. The data bus signals D0-D3 are used to write to the control registers of the 82C431. D0,D1 correspond to the planes 0 and 1, while D2, D3 correspond to the planes 2 and 3 of the display memory.



The following is a description of the registers pointed to by the Address register.

Set/Reset Register

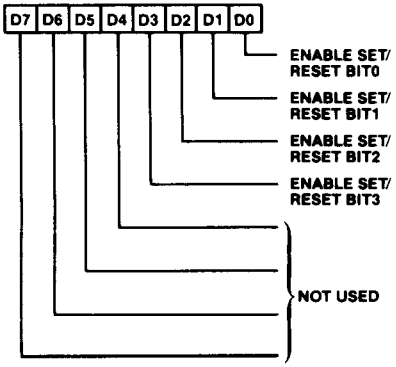
The Set/Reset register is a write-only register. The pointer in the Graphics Address register must be 00H before this register can be written into.



When the Mode register (to be described later) selects the 'write' mode 0, and the Set/Reset mode is enabled through the Enable Set/Reset register (to be described later), bits D0-D3 are the value written to the display memory planes 0-3 respectively. The planes can be written to individually by separate writes to the Set/Reset register.

Enable Set/Reset Register

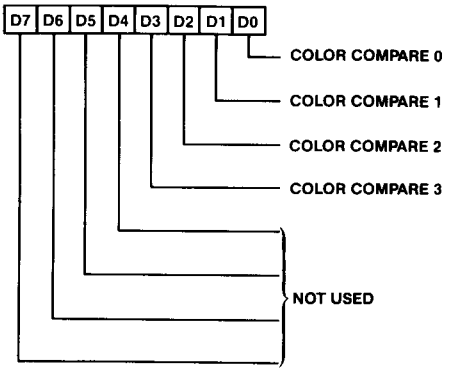
The Enable Set/Reset register is a write-only register. The register can be written to by setting the pointer in the Graphics Address register to 01H.



This register works in conjunction with the Set/Reset register. If the mode register is programmed to write mode 0, then the contents of the Set/Reset register are written to the respective display memory planes. If the write mode is 0 and Set/Reset is not enabled on a plane, the plane is written with the data from the CPU data bus.

Color Compare Register

The Color Compare register is a write-only register. It can be written into by setting the pointer in the Graphics Address register to 02H.



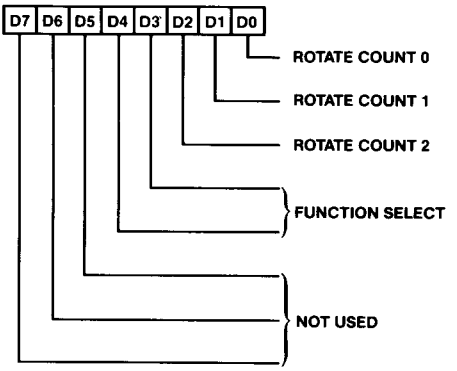
If the Mode register has the 'read' mode set, the data read from the display memory planes 0-3, is compared to the bits D0 through D3 programmed in the Color Compare register. A match between the two bit fields will result in a logical 1 being output on the corresponding data bus bit. Following is an example to illustrate the mechanism:

If the contents of the Color Compare register are 0011 (D3-D0), and:

		D7	D6	D5	D4	D3	D2	D1	D0
Plane 0 data	=	1	1	1	1	1	1	1	1
Plane 1 data	=	0	0	0	0	0	0	0	1
Plane 2 data	=	1	1	1	1	1	1	1	0
Plane 3 data	=	0	0	0	0	0	0	0	0
then data bus result	=	0	0	0	0	0	0	0	1

Data Rotate Register

The Data Rotate register is a write-only register. It is written to by setting the pointer in the Graphics Address register to 03H.



This register is used to perform a rotate function on the data written by the CPU. If the Mode register is programmed for the write mode 0, then the value in the Rotate Count field represents the number of bits the CPU data will be rotated during CPU write cycles.

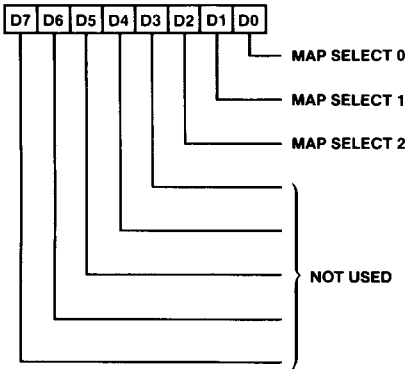
The Function select bits (D3, D4) allow data in the CPU latches to be logically operated upon by the data written into the memory. The bits operate as follows:

D4	D3	
0	0	No change to the Data
0	1	Logical 'AND' between Data and latched data.
1	0	Logical 'OR' between Data and latched data.
1	1	Logical 'XOR' between Data and latched data.

'Data' may be any of the various options available with the Write Mode register. Data cannot be the CPU latched data.

Read Map Select Register

Read Map Select register is a write-only register. It is written to by setting the pointer in the Graphics Address register to 04H.

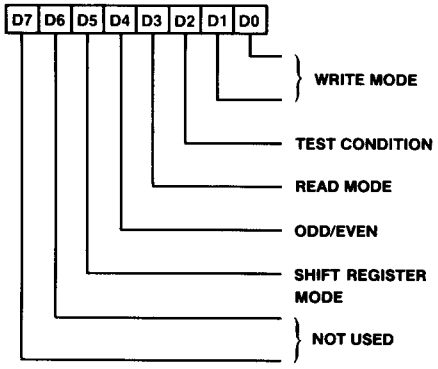


The contents of the register represent the memory plane from which the CPU reads the data. This register does not effect the read operation performed through the Color compare register. The four memory plane or maps are selected as follows:

D2	D1	D0	
0	0	0	Map 0
0	0	1	Map 1
0	1	0	Map 2
0	1	1	Map 3

Mode Register

This is a write-only register. It can be written to by setting the pointer in the Graphics Address register to 05H.



The functions of the bits are as follows:

Write Mode (D0, D1)

D1 D0

0 0 Mode 0: Each of the four display memory plane is written with the CPU data rotated by the number of counts in the Rotate register. This is always true, except when the Set/Reset register is enabled for any of the four planes. In this case, the corresponding plane is written with the data stored in the Set/Reset register.

0 1 Mode 1: Each of the four display memory planes is written with the data in the CPU latches. These latches are loaded during a previous CPU read operation.

1 0 Mode 2: Memory planes 0-3 is filled up with the value of data bits 0-3, respectively. For example, memory plane 0 is filled up with the value of data bit D0, memory plane 1 is filled up with value of data bus bit D1, and so on.

1 1 Illegal

The operations specified above will also work in conjunction with the Function Select options available through Data Rotate register.

Test Condition (D2)

D2 = 1 will tri-state the Graphics Controller outputs, including the GRAPHICS, CHAIN, CDSEL0 and CDSEL1 outputs. This feature is used for testing the chip. The ATR0-3 outputs are not tri-stated.

Read Mode (D3)

D3

0 When D3 = 0, the CPU reads the data from the display memory planes. The plane is selected through the Read Map Select register.

1 When D3 = 1, the CPU reads the result of the logical comparison between the four display memory planes data and the contents of the Color Compare register.

Odd/Even (D4)

D4 = 1 will put the Graphics Controller in the Odd/Even addressing mode. This option is useful for emulating the IBM Color Graphics Adapter mode. The value of this bit should be the same as the value programmed in D3 of the 82C432 Sequencer Memory Mode register.

Shift Register (D5)

The data bits in the memory planes 0-3 are represented as M0D0-M0D7, M1D0-M1D7, M2D0-M2D7, and M3D0-M3D7, respectively. When D5 = 1, the data in the 4 serial shift registers will be formatted as follows:

MSB							LSB	Output to
M1D0	M1D2	M1D4	M1D6	M0D0	M0D2	M0D4	M0D6	ATR0
M1D1	M1D3	M1D5	M1D7	M0D1	M0D3	M0D5	M0D7	ATR1
M3D0	M3D2	M3D4	M3D6	M2D0	M2D2	M2D4	M2D6	ATR2
M3D1	M3D3	M3D5	M3D7	M2D1	M2D3	M2D5	M2D7	ATR3

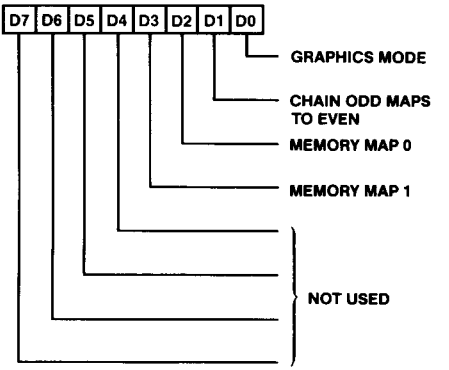
The Least Significant Bit (LSB) is shifted out first.

When D5 = 0, then M0D7-M0D0, M1D7-M1D0, M2D7-M2D0 and M3D7-M3D0 are shifted out with the bit D7 going out first in all cases. The output pins being ATR0-ATR3 respectively, for M0-M3 planes.

The first two registers correspond to the Graphics A shift registers, while the following two correspond to the Graphics B shift registers.

Miscellaneous Register

Miscellaneous register is a write-only register. It can be written into by setting the pointer in the Graphics Address register to 06H.



Graphics Mode

When D0 = 1, the graphics mode is selected. The character generator latches (which are located outside the chip) are disabled. The bit D0 is output on the GRAPHICS pin of the controller.

Chain Odd Maps to Even

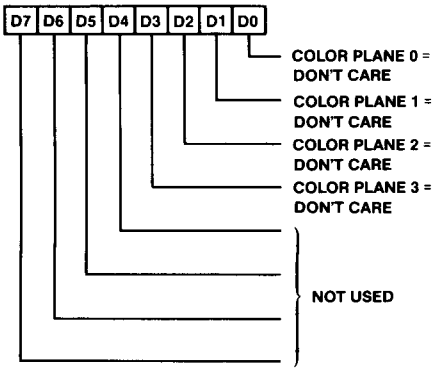
When D1 = 1, the CPU address bit A0 is replaced by a higher order address bit. (The contents of A0 determine which memory map is to be selected. A '0' will select planes 0 and 2, and a '1' will select planes 1 and 3. This function is also provided outside the chip.) The 82C431 will output the D1 onto the output pin CHAIN of the controller.

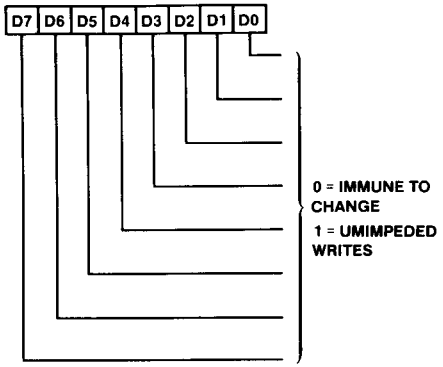
Memory Maps

These bits control the mapping of the address memory buffers into the CPU address space. The D3 and D2 are output as CDSEL1 and CDSEL0 signals from the Graphics Controller. The mapping function is not performed on the chip.

Color Don't Care Register

The Color Don't Care register is a write only register. It can be written into by setting the pointer in the Graphics Address register to 07H.





D0 = 0 will mean that color plane 0 is a don't care when the Color Compare register is performed.

D1 = 0 will mean that color plane 1 is a don't care when the Color compare register is performed.

D2 = 0 will mean that color plane 2 is a don't care when the Color compare register is performed.

D3 = 0 will mean that color plane 3 is a don't care when the Color Compare register is performed.

Bit Mask Register

Bit Mask Register is a write only register. It can be written into by setting the pointer in the Graphics Address register to 08H.

Any bit programmed to 0 in this register will cause the corresponding bit in each of the four memory planes to be immune to change. The data written into memory in this case will be the data which was read in the previous cycle, and was stored in an internal latch on the chip.

Any bit programmed to 1 will allow unrestricted manipulation of the data in the corresponding bit in each of the four memory planes.

The bit mask is applicable to any data written by the CPU, including rotate, logical functions (AND, OR, XOR), Set/Reset and No Change. The data to be preserved using the bit mask must be latched internally by reading the location. The bit mask applies to all the four planes simultaneously.

82C431 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	V_{DD} + .5	V
Output Voltage	V_O	-0.5	V_{DD} + .5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C431 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C431 DC Characterisitcs

Parameter	Symbol	Min.	Max.	Units
Input High Voltage	V_{IL}		0.8	V
Input High Voltage (Note 1)	V_{IH}	2.0		V
Output Low Voltage I_{OL} = 4mA (Note 2)	V_{OL}		0.45	V
Output High Voltage I_{OH} = -4mA (Note 2)	V_{OH}	2.4		V
Input Low Current $0 < V_{IN} < V_{CC}$	I_{IL}		±10	μA
Output Short Circuit Current V_O=0V	I_{OS}	—	20	mA
Power Supply Current @ 20 MHz Clock	I_{CC}		20	mA
Output HI-Z Leak Current $0.45 < V_{OUT} < V_{CC}$	I_{OZ1}		±10	μA

NOTES:
1. Following inputs require VIH = 3.0V (min.): DOTCLK, $\overline{\text{CPUL}}$, $\overline{\text{CRTL}}$, S/$\overline{\text{L}}$, $\overline{\text{WE}}$.
   All other inputs require VIH = 2.0V (min.)
2. All outputs and bidirectional pins.

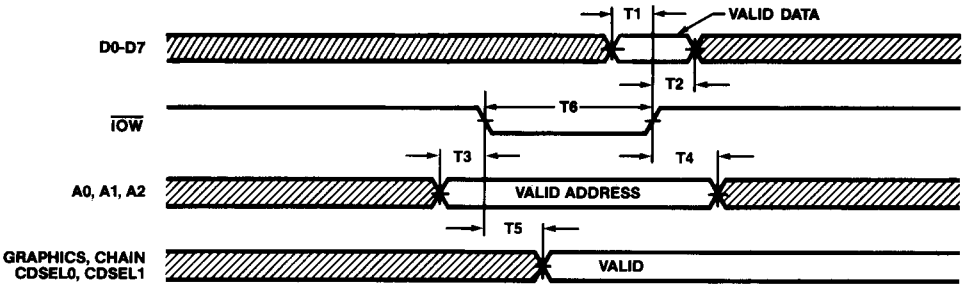
82C431 AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

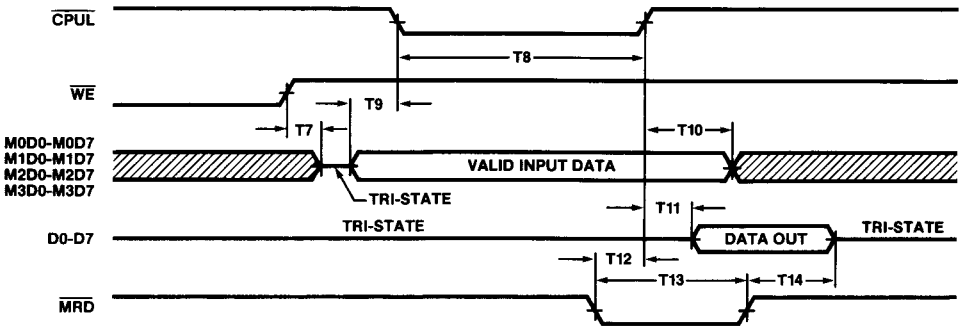
Sym	Description	Min.	Max.	Units	Notes
t1	Data set-up time to $\overline{IOW}$	55		ns	
t2	Data hold time from $\overline{IOW}$	16		ns	
t3	Address set-up time to $\overline{IOW}$	10		ns	
t4	Address hold time from $\overline{IOW}$	8		ns	
t5	Miscellaneous register output delay	21	83	ns	See Note
t6	$\overline{IOW}$ pulse width	45		ns	
t7	$\overline{WE}$ inactive to memory data bus float delay	9	35	ns	
t8	$\overline{CPUL}$ pulse width	40		ns	
t9	Input data set-up time to $\overline{CPUL}$	0		ns	
t10	Input data hold time from $\overline{CPUL}$	14		ns	
t11	Output data delay time	16	56	ns	
t12	$\overline{MRD}$ set-up time to $\overline{CPUL}$	10		ns	
t13	$\overline{MRD}$ pulse width	66		ns	
t14	$\overline{MRD}$ inactive to D0-D7 float delay	11	42	ns	
t15	Display memory data M0-M3 bus set-up time	5		ns	
t16	Display memory data M0-M3 bus hold time	13		ns	
t17	$\overline{CRTL}$ pulse width	40		ns	
t18	$\overline{WE}$ active to display memory data outputs enabled	11	45	ns	
t19	S/$\overline{L}$ to $\overline{CRTL}$ delay	10		ns	
t20	S/$\overline{L}$ to DOTCLK set-up time	25		ns	
t21	S/$\overline{L}$ to DOTCLK hold time	8	—	ns	
t22	Attributes output data delay from DOTCLK	9	37	ns	C_L = 35pF
t23	Data bus D0-D7 hold time from $\overline{WE}$	85		ns	
t24	Data bus D0-D7 hold time from $\overline{WE}$	0		ns	
t25	D0-D7 in to display memory data delay	26	103	ns	
t26	$\overline{WE}$ pulse width	90			
t27	M1D0, M1D1, M1D2, M1D3 to ATTR0-3 delay	8	31	ns	C_L = 30pF
t28	Dot Clock period	42	—	ns	
t28A	Dot Clock low time	19	—	ns	
t28B	Dot Clock high time	19	—	ns	

NOTE: A.C. TEST CONDITIONS: All A.C. timings are measured with a load capacitance of C_L = 85pF, except where noted otherwise.

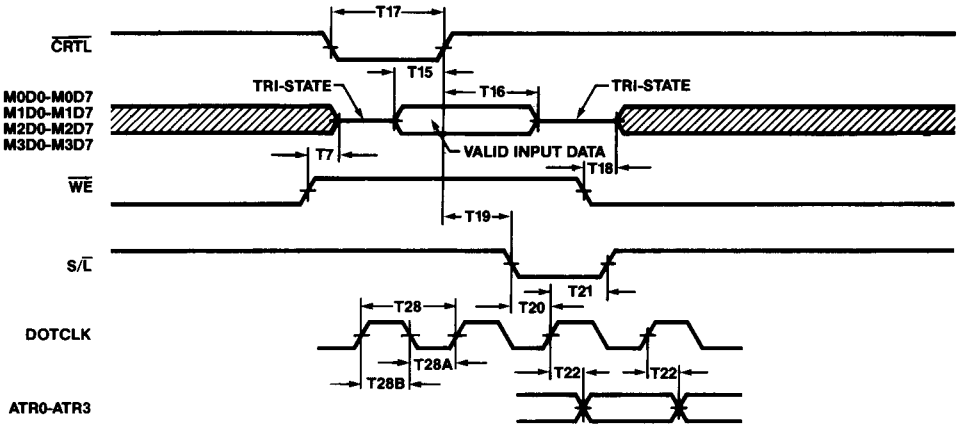
REGISTER WRITE TIMING



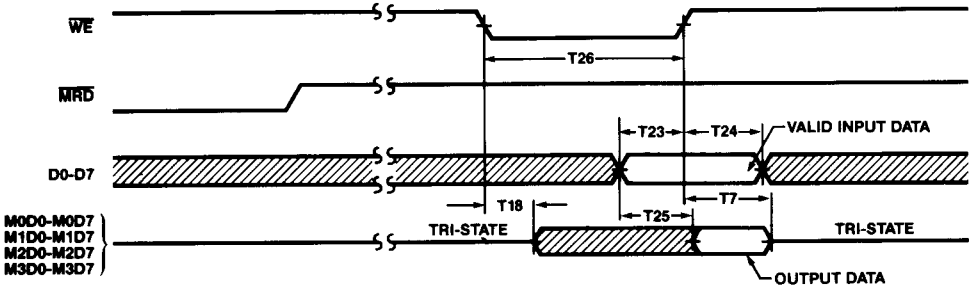
CPU READ TIMING



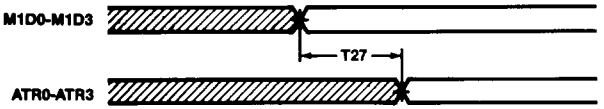
CRT READ TIMING



CPU WRITE TIMING
(MEMORY WRITE)



M1D0-M1D3 TO ATR0-ATR3 DELAY (ALPHA MODE)



82C432A Functional Description

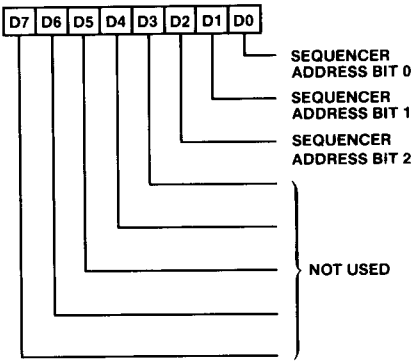
The 82C432A Sequencer generates memory timings for the display RAMs and the character clock for controlling the regenerative memory fetches. Figure 4 shows a functional diagram of the Sequencer. As shown in the figure, the Sequencer also provides control signals for other components in the Enhanced Graphics CHIPSet. The 82C432A allows the CPU to access memory during active display intervals by inserting dedicated CPU memory cycles. Figures 5-8 illustrate various memory cycles for different configurations. As is shown in the figures, the memory cycle selection allows different screen resolutions. The 82C432A also protects the entire memory from being altered, by selectively masking out planes through the configurable Mask register.

82C432A internal registers are selected through address input A0. The following table describes the addressing scheme:

A0	POINTER REGISTER SELECTED	
0	—	Address
1	0	Reset
1	1	Clocking Mode
1	2	Plane Mask (Map Mask)
1	3	Character Map Select
1	4	Memory Mode

Address Register

The Address Register is a 3-bit write-only pointer register. When loaded with a binary value (pointer) it points to the data register where data is to be written.



Reset Register

The Reset Register is a write-only register pointed to when the contents of the Address Register are 00H.

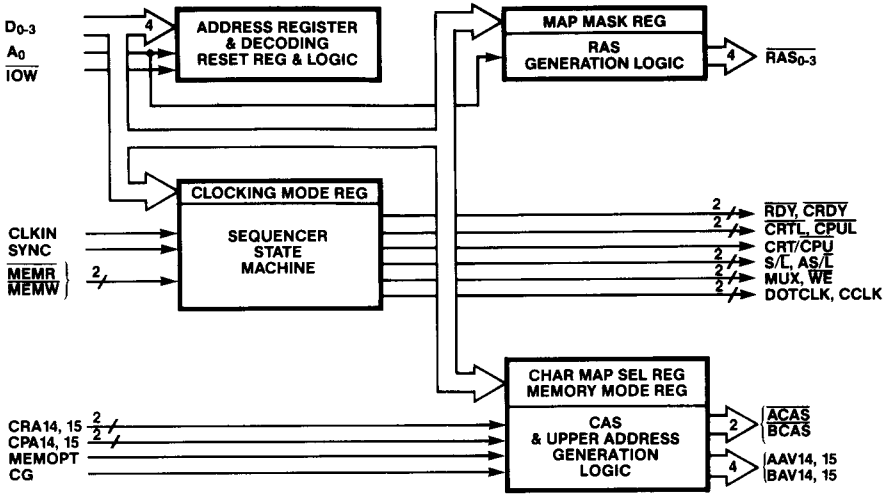
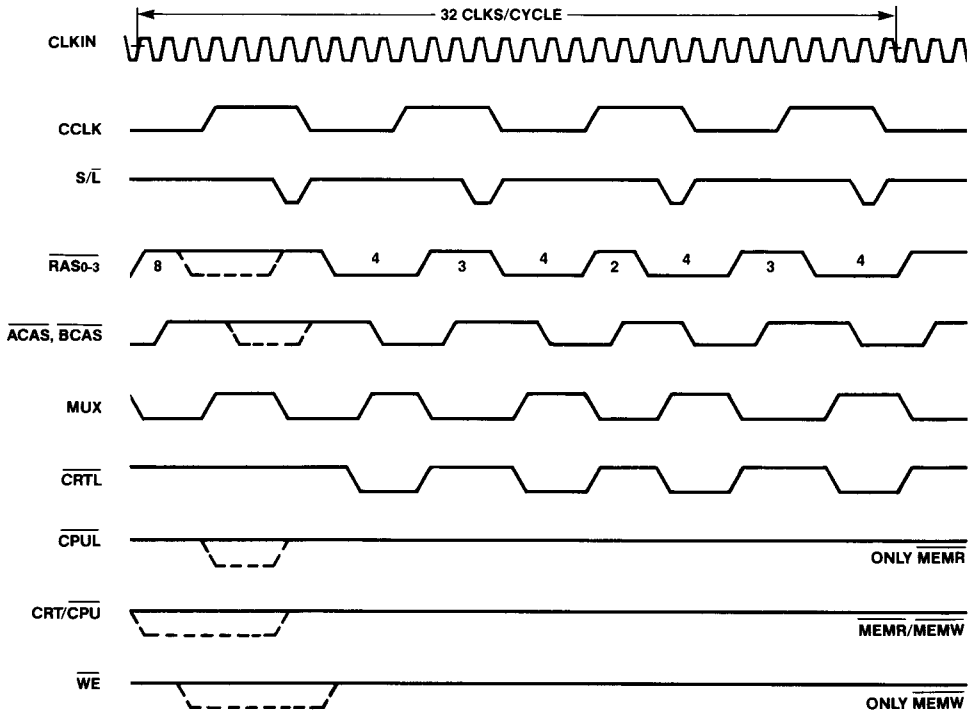


Figure 4: 82C432 Sequencer Function Diagram



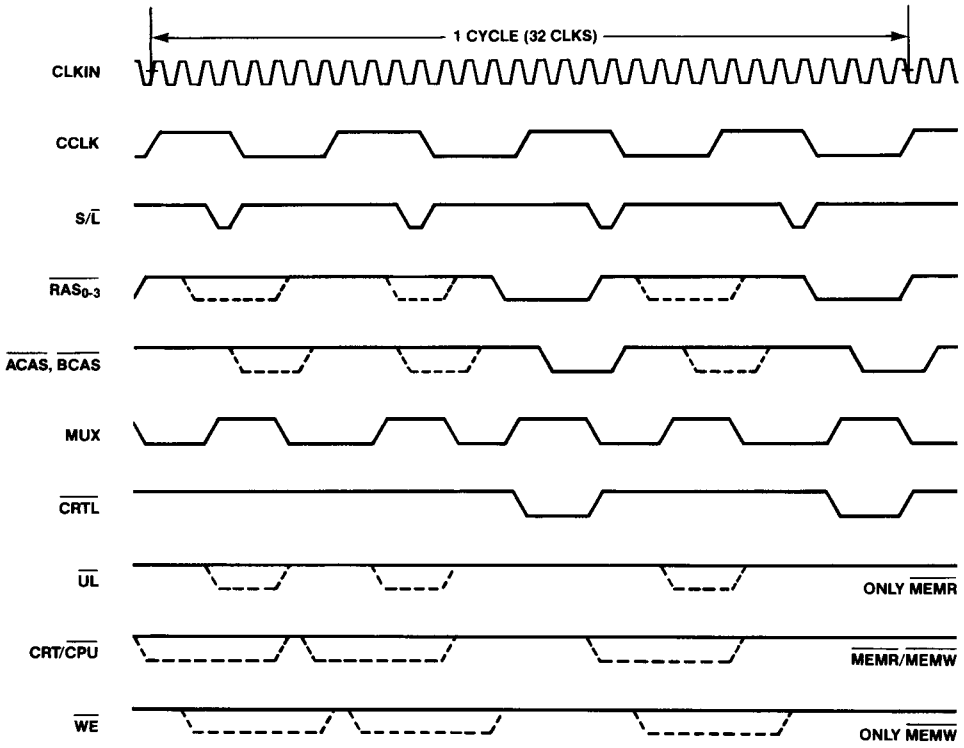
NOTE

1. Dotted waveforms indicate CPU MEMR/MEMW
   RAS/CAS occur for both CPU MEMR/MEMW

CONDITIONS:

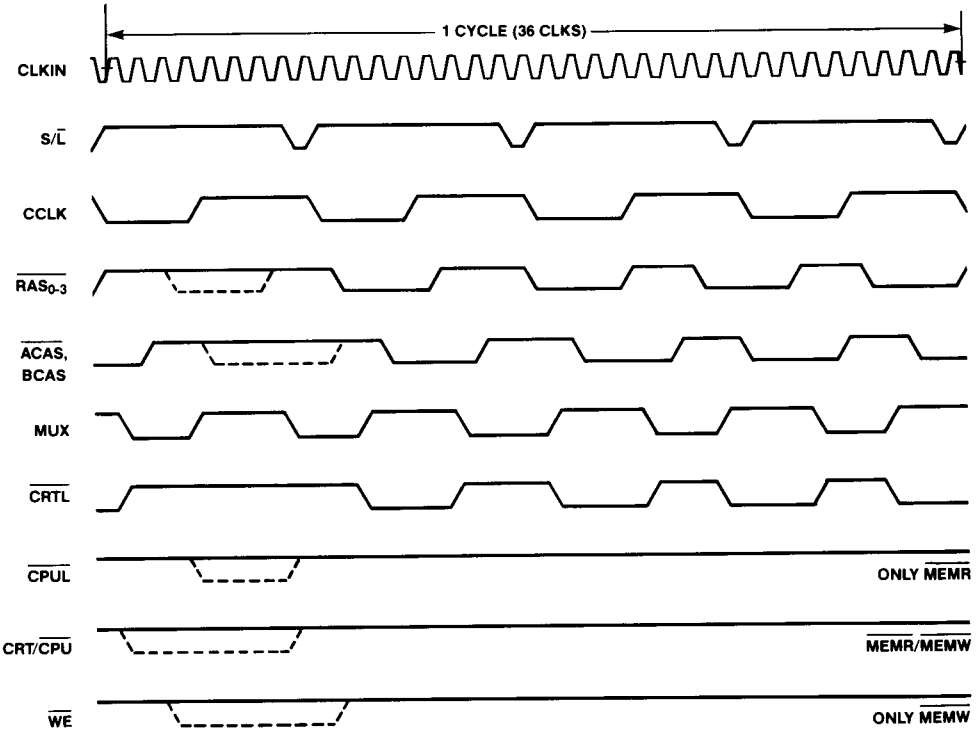
Mode Reg = 01H CRT read 4 out of 5 memory cycles
8 Dots/Char, load every char clock, normal DOTCLK

Figure 5. A Typical 640 × 350 Mode Operation



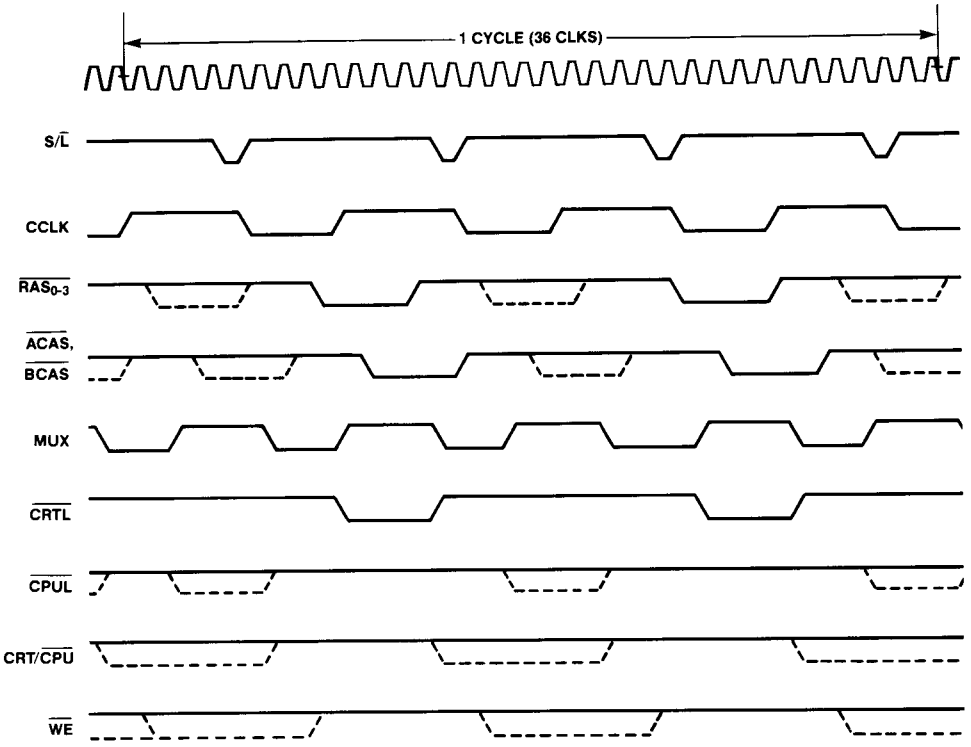
CONDITIONS:
Mode Reg = 03H CRT reads 2 out of 5 memory cycles
8 Dots/Char, load every char clock, normal DOTCLK

Figure 6. A Typical 320 × 200 Mode of Operation



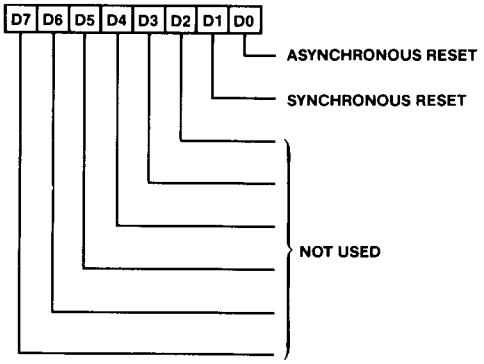
CONDITIONS:
Mode Reg = 00H CRT reads 4 out of 5 memory cycles
9 Dots/Char, load every char clock, normal DOTCLK

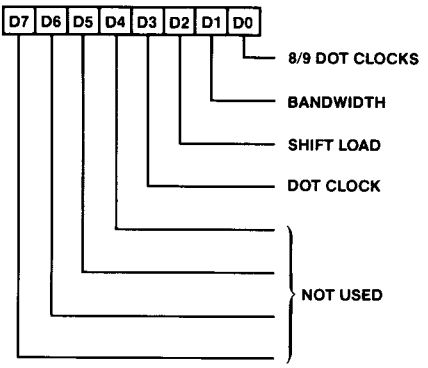
Figure 7. A Typical 720 × 350 Monochrome Operation



CONDITIONS:
Mode Reg = 02H CRT reads 2 out of 5 memory cycles
9 Dots/Char, load every char clock, normal DOTCLK

Figure 8. A Typical 9 Dots/Character with 2 out of 5 Memory Cycle Operation





Asynchronous Reset

D0=0 causes the Sequencer to clear asynchronously and halt. It also places all the outputs in a high impedance state.
D0=1 causes the Sequencer to run unless D1=0 (Synchronous Reset).

Asynchronous Reset can cause data loss in the dynamic display RAMs.

Synchronous Reset

D1=0 causes the Sequencer to clear synchronously and halt. D1=1 causes the Sequencer to run unless D0 (Asynchronous Reset) is cleared to zero. Before changing the Clocking Mode Register, the Sequencer should be reset with this bit. This will preserve the memory contents. Both the Reset Register bits must be a logical 1 to allow the Sequencer to operate.

Clocking Mode Register

This register is a 4-bit write-only register pointed to when the contents of the Address Register are 01H.

8/9 Dot Clocks (D0)

D0=0 causes the Sequencer to generate character clocks which are 9 dots wide. D0=1 causes the Sequencer to generate character clocks which are 8 dots wide.

The only IBM mode that uses 9 dots wide character clocks is the monochrome alphanumeric mode. The resolution for this mode is 720 x 350. All other modes use 8 dots wide character clocks.

Bandwidth (D1)

D1=0 makes CRT memory cycles occur on 4 out of 5 available display memory cycles.

D1=1 makes CRT memory cycles occur on 2 out of 5 available display memory cycles. Medium resolution modes (horizontal resolution of 320 pixels) require less data to be fetched from the display memory driving the horizontal scan time . This allows the CPU greater access time to the display memory. All high resolution modes (horizontal resolution of 640 or 720 pixels) must provide the CRT Controller with 4 out of 5 available display memory cycles in order to refresh the display image.

Shift Load (D2)
D2=0 causes the display serializers in the Graphics Controller to be reloaded every character clock.

D2=1 causes the display serializers to be reloaded every other character clock. This mode is useful when 16 bits are fetched every memory cycle and chained together in the shift registers.

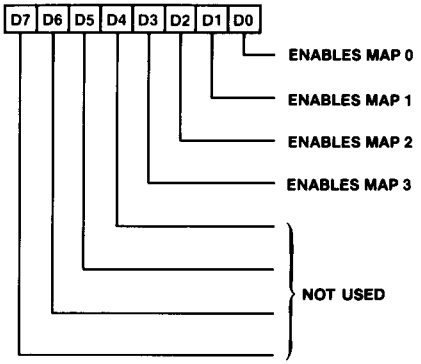
This bit is only set for APA (all-points-addressable) graphics modes.

Dot Clock (D3)
D3=0 selects the Sequencer master clock input to be output on the Dot Clock output pin.

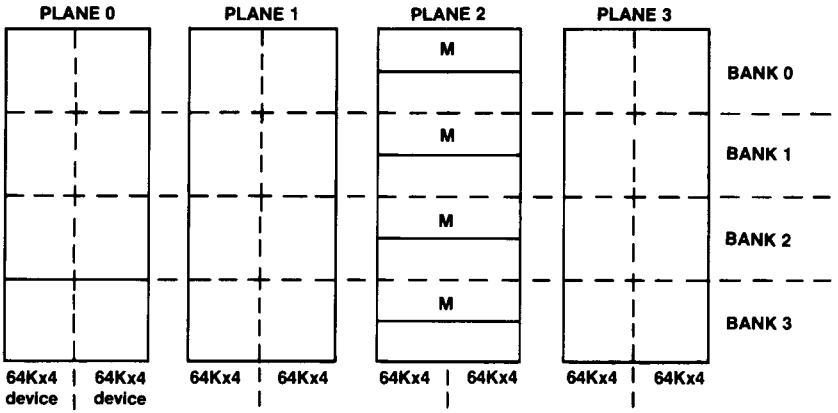
D3=1 causes the master clock to be divided by 2 to generate the dot clock. As the Dot Clock is the primary clock used by the Enhanced Graphics CHIPSet, all other timings will be stretched as they are derived from the Dot Clock. Dot Clock divided by 2 is used for 320 x 200 modes.

Plane Mask Register (also referred as Map Mask Register)

This register is a 4-bit write-only register pointed to when the contents of the Address Register are 02H.



The Plane Mask register is also referred to in some cases as Map Mask register. However, it is actually a plane mask register as illustrated in figure 9. The maps only correspond to the



M = Memory Maps in Plane 2. Each map corresponds to 8 Kbytes of memory.
Banks 0, 1, 2, 3 correspond to 16 Kbytes of memory segments in each of the four planes.

In the alphanumeric mode:
Plane 0 has Address data
Plane 1 has Attribute data
Plane 2 has Pixel (character) data
Plane 3 not used

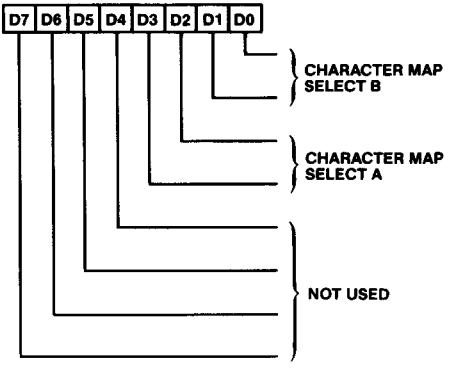
Figure 9. Enhanced Graphics Controller Memory Organization

upper 8 K bytes of every 16 K byte block of display memory in plane 2. A logical 1 in any of the bits 0 through 3 enables the CPU to write to the corresponding memory planes 0 through 3. These bits disable the corresponding $\overline{RAS0}$ through $\overline{RAS3}$ signals during CPU memory writes. When this register is loaded with 0FH, the CPU can perform a 32-bit write operation in one memory cycle. This substantially reduces the overhead on the CPU during display update cycles in graphics modes.

When odd/even modes are selected (by clearing bit 2 of the Memory Mode Register) planes 0,1 and planes 2,3 should have the same plane mask value.

Character Map Select Register

This register is a 4-bit write-only register pointed to when the contents of the Address Register are 03H. This register only affects the B-address bus (signals $\overline{BCAS}$, BAV14 and BAV15).



Character Map Select B

D1-D0 select the map used to generate alpha characters when attribute bit 3 is 0 (display memory bit M1D3) according to the following table:

D1	D0	Map Selected	Table Location
0	0	0	1st 8K of Plane 2 Bank 0
0	1	1	1st 8K of Plane 2 Bank 1
1	0	2	1st 8K of Plane 2 Bank 2
1	1	3	1st 8K of Plane 2 Bank 3

Character Map Select A

D3-D2 select the map used to generate alpha-numeric characters when attribute bit 3 is a 1, according to the following table:

D1	D2	Map Selection	Table Location
0	0	0	1st 8K of Plane 2 Bank 0
0	1	1	1st 8K of Plane 2 Bank 1
1	0	2	1st 8K of Plane 2 Bank 2
1	1	3	1st 8K of Plane 2 Bank 3

In alphanumeric modes, bit 3 of the attribute byte (M1D3) normally turns the foreground intensity on or off. This bit may be redefined to be a switch between character sets. This function is enabled when there is a difference between the values of Character Map Select A and Character Map Select B bits. Whenever the two values are the same, the character select function is disabled. Memory Mode Register bit 1=0 (indicating the presence of a full 256K byte memory configuration) enables this function; otherwise bank 0 (indicating the presence of a minimum 64K byte memory configuration) is always selected. 256K bytes of memory support 4 character sets.

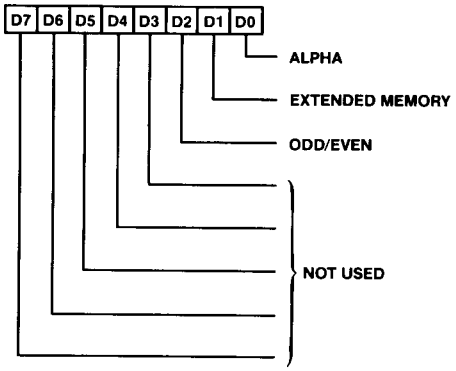
Asynchronous Reset (Reset Register bit 0) clears the Character Map Select Register to 0. This should only be done during a system reset.

Memory Mode Register

This register is a 3-bit write-only register pointed to when the contents of the Address Register are 04H.

Alphanumeric (D0)

D0=0 indicates that a non-alphanumeric mode is active. This forces BAV14 = AAV14 and BAV15 = AAV15.



D0=1 indicates that the alpha mode is active and enables the Character Map Select register description.

Extended Memory (D1)

D1=0 indicates that 1 bank of 16Kx4 dynamic RAMs is present (64K bytes of display memory). AAV14, AAV15, BAV14, BAV15 address bits are disabled.

D1=1 indicates that 1 bank of 64Kx4 dynamic RAMs are present (256K bytes of display memory), and the high order address bits AAV14, AAV15, BAV14 and BAV15 are enabled to the CRT Controller.

Odd/Even (D2)

D2=0 directs even CPU addresses to access maps 0 and 2 ($\overline{RAS0}$ and $\overline{RAS2}$ are enabled), while odd CPU addresses access maps 1 and 3 ($\overline{RAS1}$ and $\overline{RAS3}$ are enabled).

D2=1 causes CPU addresses to sequentially access data within a bit map (all 4 $\overline{RAS}$ signals are enabled).

The maps are accessed according to the value in the Map Mask Register.

82C432A Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	V_{DD} + .5	V
Output Voltage	V_O	-0.5	V_{DD} + .5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C432A Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C432A DC Characterisitcs

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL1} = 2mA (Note 1) I_{OL2} = 4mA (Note 2) I_{OL3} = 8mA (Note 3)	V_{OL}		0.45	V
Output High Voltage I_{OH} = (Note 4)	V_{OH}	3.5		V
Input Low Current $0 < V_{IN} < V_{CC}$	I_{IL}	-10	+10	μA
Output Short Circuit Current V_O=0V	I_{OS}		20	mA
Power Supply Current @ 8 MHz Clock	I_{CC}		20	mA
Output HI-Z Leak Current $0.45 < V_{OUT} < V_{CC}$ (Note 5)	I_{OZ1}		±10	μA

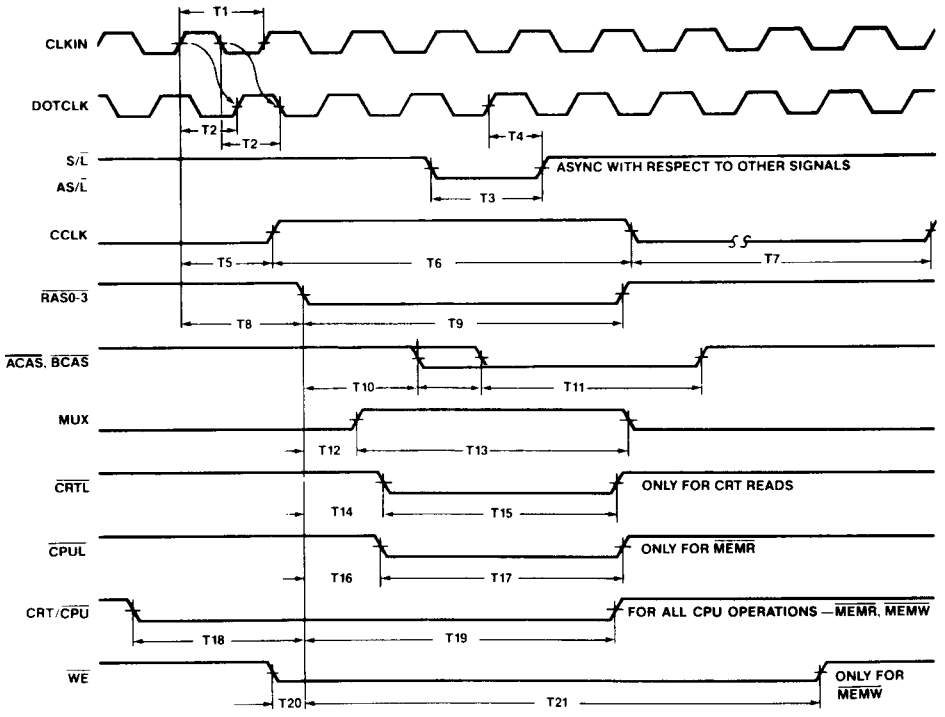
NOTES:
1. For AAV14, AAV15, BAV14, BAV15, MUX, $\overline{\text{RDY}}$, CCLK, and CRT/$\overline{\text{CPU}}$ pins only.
2. For $\overline{\text{CRTL}}$, $\overline{\text{CPUL}}$, S/L, DOTCLK, and $\overline{\text{RAS0}}$-$\overline{\text{RAS3}}$ only, $\overline{\text{ACAS}}$, $\overline{\text{BCAS}}$, $\overline{\text{WE}}$
3. For and $\overline{\text{CRDY}}$ only.
4. I_{OH} is equal to the corresponding I_{OL} for the pin.
5. For $\overline{\text{CRTL}}$, I_{OZ1} is ±100μA.

82C432A AC Characteristics

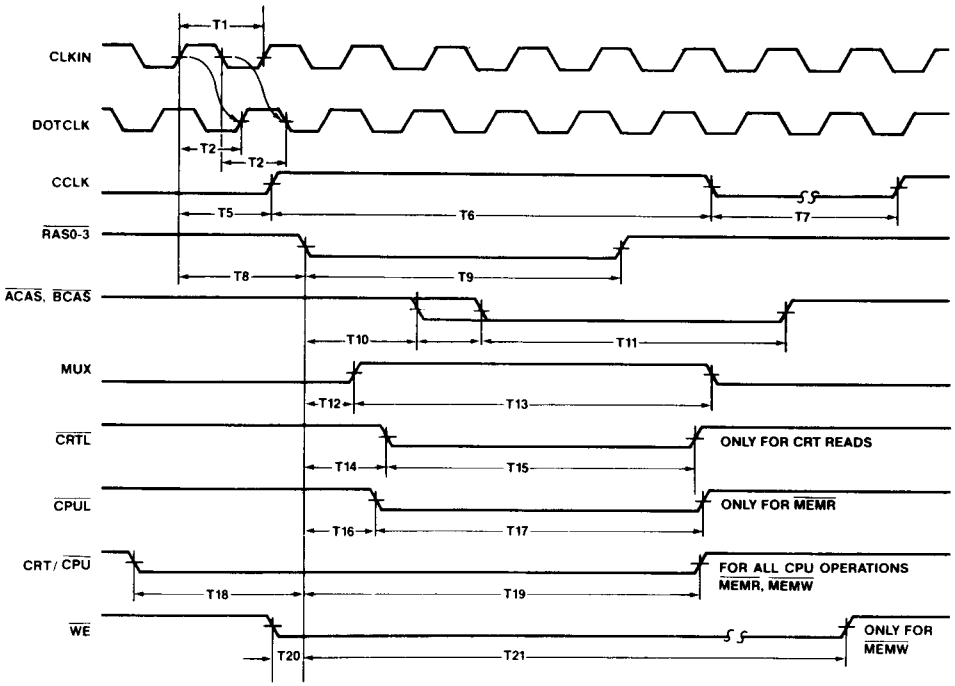
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Description	8 Dots/Char Min.	8 Dots/Char Max.	9 Dots/Char Min.	9 Dots/Char Max.	Units
t1	CLKIN period	42		42		ns
t1A	CLKIN Low time	19		19		ns
t1B	CLKIN high time	19		19		ns
t2	CLKIN to DOTCLK delay	6	40	6	40	ns
t3	S/$\overline{L}$ pulse width	t1-10	t1+10	t1-10	t1+10	ns
t4	DOTCLK edge to S/$\overline{L}$ hold time	6		6		ns
t5	CLKIN to CCLK delay		56		56	ns
t6	CCLK high time	4t1	4t1+30	5t1	5t1+30	ns
t7	CCLK low time	4t1-30	4t1	4t1-30	4t1	ns
t8	CLKIN to $\overline{RAS0\text{-}3}$ active delay		76		76	ns
t9	$\overline{RAS0\text{-}3}$ width	4t1-10	4t1+10	5t1-10	5t1+10	ns
t10	$\overline{RAS0\text{-}3}$ to $\overline{ACAS}$ and $\overline{BCAS}$ delay		1.5t1+6		1.5t1+6	ns
t11	$\overline{ACAS}$ and $\overline{BCAS}$ width	3.5t1-18		3.5t1-18		ns
t12	$\overline{RAS0\text{-}3}$ to MUX delay	.5t1-10	.5t1+10	.5t1-10	.5t1+10	ns
t13	MUX width	3t1-10	3t1+10	4t1-10	4t1+10	ns
t14	$\overline{RAS0\text{-}3}$ to $\overline{CRTL}$ delay		t1+20		t1+20	ns
t15	$\overline{CRTL}$ width	3t1-20		4t1-20		ns
t16	$\overline{RAS0\text{-}3}$ to $\overline{CPUL}$ delay		t1+20		t1+20	ns
t17	$\overline{CPUL}$ width	3t1-10		4t1-10		ns
t18	CRT/$\overline{CPU}$ set-up time to $\overline{RAS0\text{-}3}$	2t1-30		2t1-30		ns
t19	CRT/$\overline{CPU}$ hold time to $\overline{RAS0\text{-}3}$	4t1-14		5t1-15		ns
t20	$\overline{WE}$ set-up time to $\overline{RAS0\text{-}3}$	0		0		ns
t21	$\overline{WE}$ hold time to $\overline{RAS0\text{-}3}$	6t1		7t1		ns
t22	$\overline{MEMR}$ or $\overline{MEMW}$ delay to $\overline{CRDY}$		51		51	ns
t23	$\overline{MEMR}$ or $\overline{MEMW}$ delay to $\overline{RDY}$		58		58	ns
t24	$\overline{ACAS}$ and $\overline{BCAS}$ to $\overline{CRDY}$ delay		11		11	ns
t25	$\overline{ACAS}$ and $\overline{BCAS}$ to $\overline{RDY}$ delay		14		14	ns
t26	$\overline{IOW}$ pulse width	50		50		ns
t27	Data set-up time to $\overline{IOW}$	15		15		ns
t28	Data hold time from $\overline{IOW}$	15		15		ns

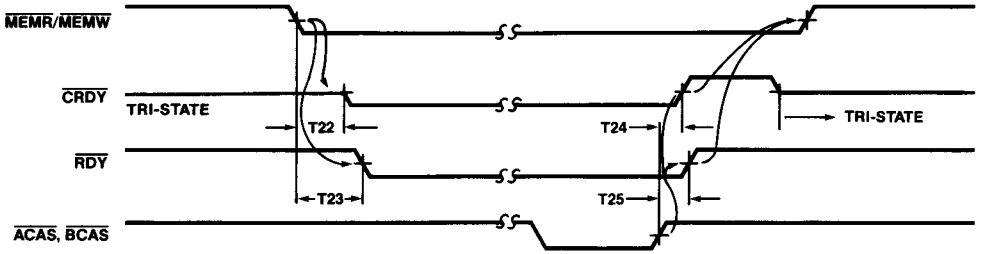
8 Dots/Char.

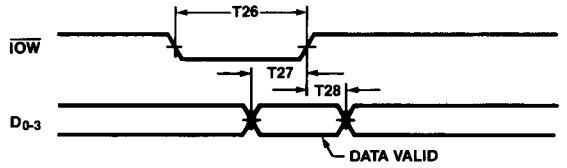

T1
CLKIN
DOTCLK
T2
T2
T4
S/L
AS/L
ASYNC WITH RESPECT TO OTHER SIGNALS
T3
CCLK
T5
T6
T7
RAS0-3
T8
T9
ACAS, BCAS
T10
T11
MUX
T12
T13
CRTL
ONLY FOR CRT READS
T14
T15
CPUL
ONLY FOR MEMR
T16
T17
CRT/CPU
FOR ALL CPU OPERATIONS — MEMR, MEMW
T18
T19
WE
ONLY FOR MEMW
T20
T21

9 Dots/Char.


T1
CLKIN
DOTCLK
T2
T2
CCLK
T5
T6
T7
RAS0-3
T8
T9
ACAS, BCAS
T10
T11
MUX
T12
T13
CRTL
T14
T15
ONLY FOR CRT READS
CPUL
T16
T17
ONLY FOR MEMR
CRT/CPU
T18
T19
FOR ALL CPU OPERATIONS
MEMR, MEMW
WE
T20
T21
ONLY FOR
MEMW

RDY & CRDY TIMINGS





82C433 Functional Description

The 82C433 Attributes Controller provides a palette of 16 colors selectable from a possible 64, each one of which may be specified separately. Six color outputs, Red (R), Green (G), Blue (B), Secondary Red (RS), Secondary Green/Intensity (GS/I) and Secondary Blue/ Monochrome (BS/V) are available as outputs. The 82C433 also controls blinking and underline operations. The Attributes controller takes data from the display memory and formats it for display on the screen. It also provides the horizontal pixel panning capability in both alphanumeric and all-points-addressable modes. Figure 10 illustrates a functional diagram of the chip. In the alphanumeric mode, the ATR0-3 or the ATR4-7 inputs are selected by the Condition Code inputs, CC0-CC7. (Note that in the Alphanumeric mode the ATR0-7 data is obtained directly from the display memory.) The 4 attribute signals are then decoded to select one of the 16 color palette registers. The color palette, which consists of 16 registers, each 6-bit wide, can be loaded with any color combination. Thus it is possible to display the characters in any one of the 16 colors out of a possible of 64 (6-bit wide registers). In the graphics mode the condition code inputs have no affect on the ATR0-7 inputs. Also, in the graphics mode, the ATR4-7 are don't care inputs. The ATR0-3 inputs are obtained from the Graphics Controller and are used to select one of the 16 color registers. This determines the display color for each individual pixel. Figures 11, 12 and 13 illustrate examples of Cursor control, Alphanumeric data timings and Graphics data timings.

An internal flip-flop controls the selection of the address and data registers. To select the Address register, an IOR signal is used to clear this flip-flop. After the Address Register has been loaded by an IOW, this flip-flop toggles, and the chip is ready to have a data register (pointed to by the Address Register) loaded. Every IOW input toggles this flip-flop.

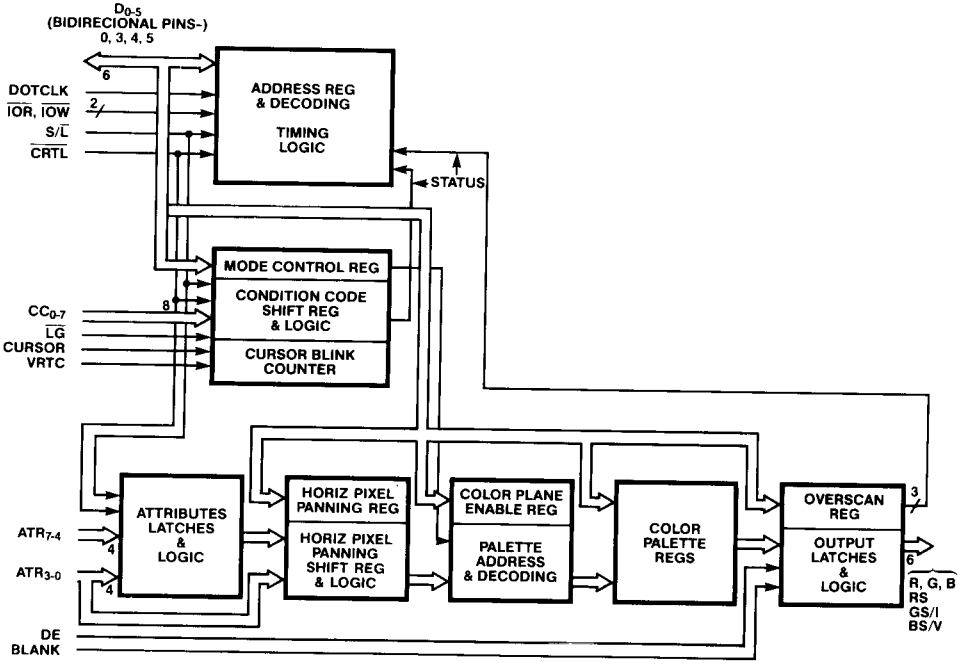
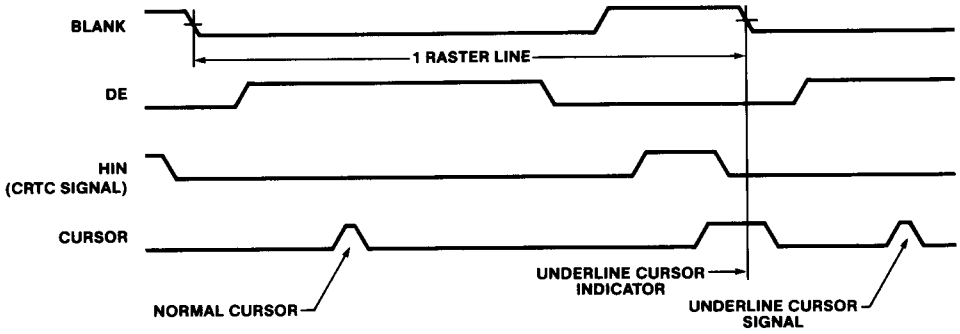


Figure 10. 82C433 Functional Diagram



NOTES
1. To enable underline cursor ATR_{7-0} = X009 X001 B
2. Color of cursor is set by ATR_{3-0}
3. Polarity of HIN is set by HPOL in CRT Controller

Figure 11. Cursor Operation

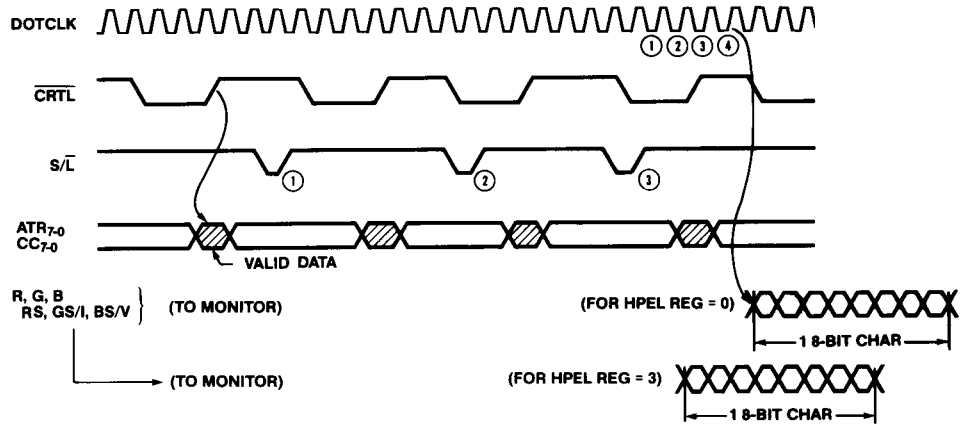


Figure 12. Alphanumeric Data Timings

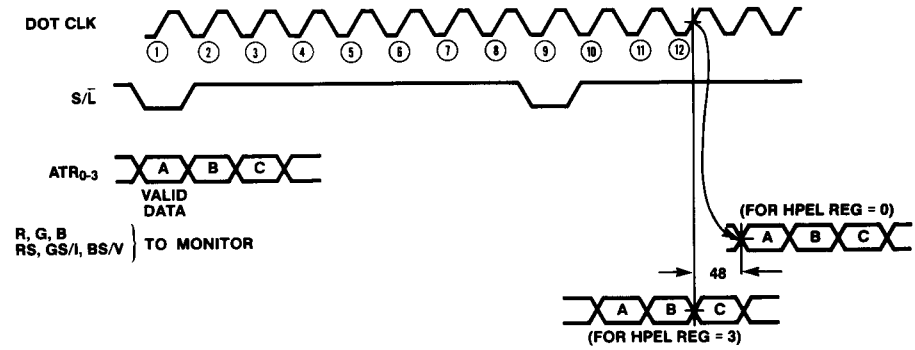


Figure 13. Graphics Data Timings

The Condition Code CC0-7 inputs select between ATR0-3 and ATR4-7 inputs. ATR0-3 and ATR4-7 control the foreground and background on the display screen, respectively. When the corresponding condition code is 1, ATR0-3 is selected, while a logical 0 on the condition code input will select ATR4-7 as the attributes inputs. Following is an example to illustrate this selection:

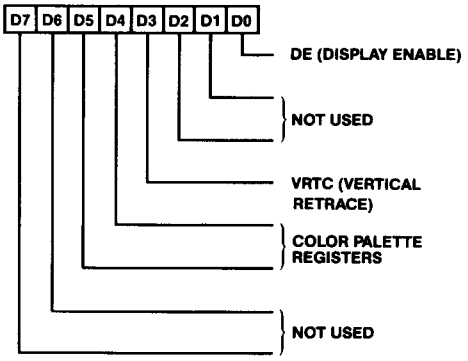
	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
Input	1	0	1	1	0	0	1	1
Attributes selected	a	b	a	a	b	b	a	a

where a = ATR0-3 and b = ATR4-7.

Note that the Attributes inputs are clocked in on the dot clock and the Condition Code is loaded into the chip by Select/Load input.

Status Port

The 4-bit Status Port is accessed when the Attributes Controller receives an IOR input signal. Status data is output on the Data Bus as shown below:



DE (D0)

D0 output is an active low Display Enable signal, which is an inversion of the active high Display Enable output from the CRT Controller.

VRTC (D3)

D3 output is an active high vertical retrace signal, which is functionally the same as the active high Vertical Retrace output from the CRT Controller.

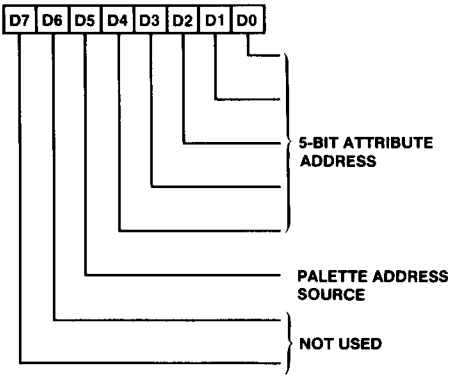
Color Palette Registers (D4, D5)

D4 and D5 outputs are two of the six color outputs of the Palette registers to the CRT screen. There are 3 pairs of the two color outputs, which are controlled by bits D4 and D5 of the COLOR PLANE ENABLE register which is described later.

82C433 Attributes Controller Register Summary

Register Number	Register Name	Pointer Value in Hex
—	Address Register	—
R0-RF	Palette Registers	00-0F
R10	Mode Control	10
R11	Overscan Color	11
R12	Color Plane Enable	12
R13	Horizontal Pixel Panning	13

Attribute Address Register



This is a 6-bit write-only register.

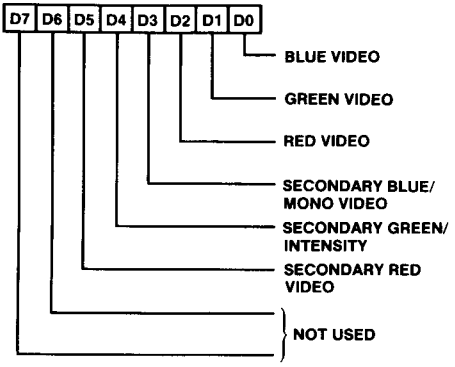
D0-D4 bits are used to point to the internal data registers in the Attribute Controller.

D5=0 allows the loading of the Color Palette registers.

D5=1 allows nqrmal operation by enabling access to the Color Palette registers for CRT read operations.

Palette Registers

These are 16 6-bit write-only registers pointed to when the contents of the Address register are 00H through 0FH.

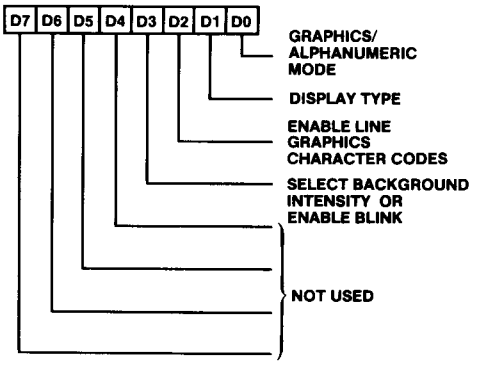


These 6-bit registers allow a dynamic mapping between the text attribute or graphic color input and the display color on the CRT screen. The six bits, D0-D5 are output as B, G, R, BS/V, GS/I, and RS, respectively. A logical 1 in a bit selects the corresponding color for that bit while a 0 de-selects it. The maximum number of possible displayable colors is 64 for monitors with 6 color inputs. Monitors with 3 color inputs allow a maximum of 6 displayable colors, while monitors which also have an intensity input allow a maximum of 16 displayable colors.

The Color Palette Register should be loaded only during vertical retrace time to avoid glitches on the CRT monitor screen. (An interrupt is generated by the CRT Controller to indicate the end of the vertical Display Enable signal.)

Mode Control Register

This is a 4-bit write-only register pointed to when the contents of the Address Register are 10H.



Graphics/Alphanumeric Mode (D0)

D0=0 selects alphanumeric mode.
D0=1 selects graphics mode.

Monochrome/Color Display (D1)

D1=0 selects color display attributes.
D1=1 selects IBM Monochrome display attributes.

Enable Drive Graphics Character Codes (D2)

D2=0 makes the ninth dot the same as the background. This will enable compatibility with the IBM Monochrome display adapter, which uses 9 dots per character.

D2=1 enables the special line graphics character codes for the IBM Monochrome Display Adapter. When this bit is set, it forces the ninth dot of a line graphics character to be identical to the eighth dot of the character. The line graphics character codes for the Monochrome Display Adapter are C0H through DFH. The Line Graphics input LG from the CRT Controller determines when a special line graphics character is to be displayed. The LG is activated by the CRT Controller at this time. The Attributes Controller will monitor the LG input (if D2 = 1) and when LG is active, it will force the ninth dot bit of a line graphics to be identical to the eighth dot of the character.

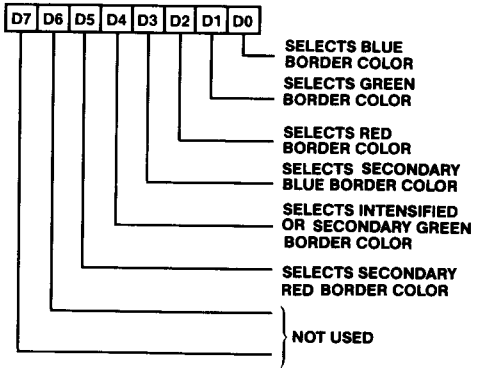
Enable Blink/Select Background Intensity (D3)

D3=0 selects the background intensity for the attribute input. This is required for Monochrome and Color Graphics Adapter compatibility.

D3=1 enables the blink attribute in alphanumeric and graphics modes. The blinking counter operates off the VRTC input. It divides the VRTC input by 32. For Alphanumeric and Graphics modes,the blink is ON for 16 VRTC clocks and OFF for 16 VRTC clocks. In the Alphanumeric mode, blink is usually used in Monochrome display modes only. In this case, the blink affect displays the character for 16 frames and blanks the screen for 16 frames. In the graphics mode, when the blink is activated, the attributes bit ATR3 is inverted alternately, thus allowing two different colors to be displayed for 16 CRT Controller clocks each. When the CURSOR is displayed in the Alphanumeric mode, the 'characters' are blinked at the rate of 16 frames ON and 16 frames OFF. The CURSOR, however, is blinked at a rate of ON for 8 frames and OFF for 8 frames.

Overscan Color Register

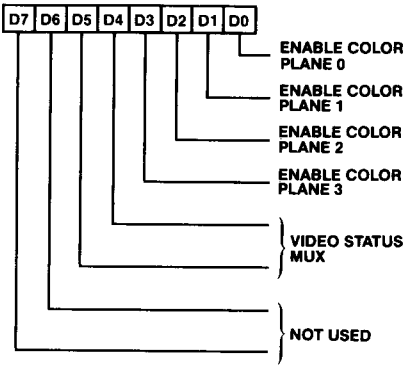
This is a 6-bit write-only register pointed to when the content of the Address Register is 11H.



This 6-bit register defines the overscan or border color displayed on the CRT screen. For monochrome displays, this register should be cleared to logical 0. A logical 1 selects the corresponding color. The border color is displayed when both BLANK and DE (Display Enable) input signals are inactive.

Color Plane Enable Register

This is a 6-bit write only register pointed to when the content of the Address Register is 12H.



Enable Color Plane (D0–D3)

A logical 1 in any of the bits D0-D3 enables the respective display memory color plane 0-3.

Display Status MUX (D4–D5)

Bits D4 and D5 select two of the six color outputs to the CRT screen, which are 2 outputs of the 4 status bits. The output color combinations available on the status bits are listed in the following table:

Color Plane Enable Register		Attributes Controller Status Register Outputs	
D5	**D4**	**Bit 5**	**Bit 4**
0	0	Red	Blue
0	1	Secondary Blue	Green
1	0	Secondary Red	Secondary Green
1	1	Not Used	Not Used

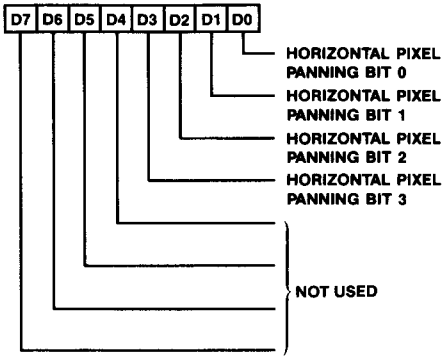
This capability can be used to run diagnostics on the color subsystem card.

D4 = 1 will also:

- Tri-state the color monitor outputs,R,G,B, RS, GS/I and BS/V and,
- Clear the cursor blink counter. D4 has to be cleared to logical 0 for the cursor blink counter to function.

Horizontal Pixel Panning Register

This is a 4-bit write-only register pointed to when the content of the Address Register is 13H.



Bits D0-D3 select the number of picture elements (pels) to shift the display data horizontally to the left. Pixel (Pel) panning is available in both A/N (alphanumeric) and APA (all-points-addressable) modes. In Monochrome A/N mode the output can be shifted a maximum of 9 pels, whereas in all other modes a maximum shift of 8 pels is possible. The start address register specifies the byte of the upper left corner of the screen display, and the pixel panning makes it possible to move it in portions of a byte, pixel by pixel.

82C433 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	V_{DD} + .5	V
Output Voltage	V_O	-0.5	V_{DD} + .5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C433 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C433 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage	V_{IH}	2.0		V
Output Low Voltage I_{OL}=4mA (Note 1)	V_{OL}		0.45	V
Output High Voltage (Note 2)	V_{OH}	3.5		V
Input Low Current $0 < V_{IN} < V_{CC}$	I_{IL}		±10	μA
Output Short Circuit Current V_O=0V	I_{OS}		20	mA
Power Supply Current @ 20 MHz Clock	I_{CC}		20	mA
Output HI-Z Leak Current $0.45 < V_{OUT} < V_{CC}$	I_{OZ1}		±10	μA

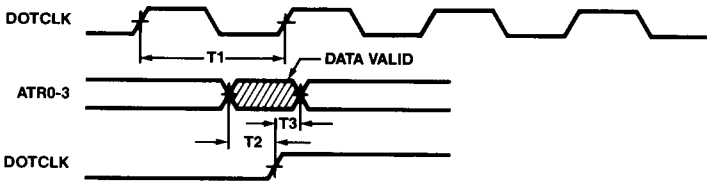
NOTES:
1. All outputs and bidirectional pins.
2. I_{OH} is equal to the I_{OL} for the pin.

82C433 AC Characteristics

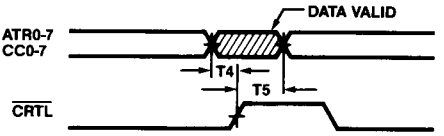
(T_A = 0° C to 70° C, V_{CC} = 5V ± 5%)

Sym	Description	Min.	Max.	Units
t1	Dot Clock period	42	—	ns
t2	ATR0-3 set-up time to Dot Clock (for graphics data)	10	—	ns
t3	ATR0-3 hold time from Dot Clock (for graphics data)	5	—	ns
t4	ATR0-3 and CC0-7 set-up time to $\overline{\text{CRTL}}$ (alphanumeric data)	0	—	ns
t5	ATR0-3 and CC0-7 hold time from $\overline{\text{CRTL}}$ (alphanumeric data)	15	—	ns
t6	Dot Clock to R, G, B, RS, GS/I, BS/V delay	—	48	ns
t7	$\overline{\text{IOW}}$ pulse width	50	—	ns
t8	$\overline{\text{IOW}}$ to data set-up time	15	—	ns
t9	$\overline{\text{IOW}}$ to data hold time	15	—	ns
t10	$\overline{\text{IOR}}$ pulse width	100	—	ns
t11	$\overline{\text{IOR}}$ to data delay	—	70	ns
t12	$\overline{\text{IOR}}$ hold time to data valid	20	—	ns

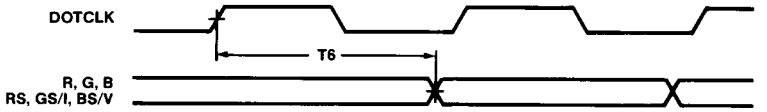
FOR GRAPHICS DATA (FROM 82C431)



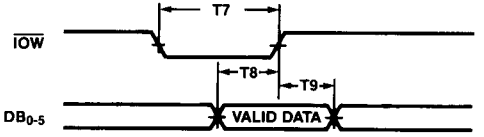
FOR ALPHANUMERIC DATA (FROM DISPLAY RAMS)

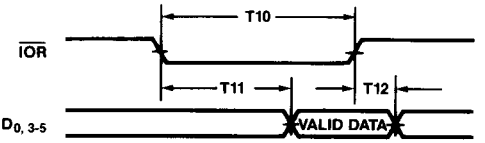


OUTPUT DATA (TO MONITOR)



CPU WRITE





82C434A Functional Description

The 82C434A CRT Controller provides the synchronization signals for the display monitor. The device contains various CPU accessible I/O registers, that allow flexible configuration options. These options include user configurable horizontal and vertical timings and polarity, cursor type and position, horizontal scan lines, and several other display related characteristics. The chip also provides split screen capability, soft scrolling and a light pen interface.

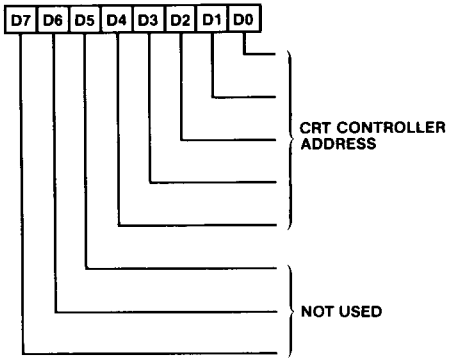
The highly programmable chip consists of 26 configurable registers. Out of the 26, 25 are addressed by activating the appropriate address lines, while one is written to by activating the MODEIOW input. Following is a detailed description of each one of these registers. Figure 13 illustrates a block diagram of the CRT Controller.

82C434 CRT Controller Register Summary

Register Number	Register Name	Pointer Value in Hex
—	Address Register	—
R0	Horizontal Total	00
R1	Horizontal Display End	01
R2	Start Horizontal Blank	02
R3	End Horizontal Blank	03
R4	Start Hor. Retrace	04
R5	End Hor. Retrace	05
R6	Vertical Total	06
R7	Overflow	07
R8	Preset Row Scan	08
R9	Max Scan Line	09
RA	Cursor Start	0A
RB	Cursor End	0B
RC	Start Address High	0C
RD	Start Address Low	0D
RE	Cursor Location High	0E
RF	Cursor Location Low	0F
R10	Vertical Retrace Start	10
R10	Light Pen High	10
R11	Vertical Retrace End	11
R11	Light Pen Low	11
R12	Vertical Display End	12
R13	Offset	13
R14	Underline Location	14
R15	Start Vertical Blank	15
R16	End Vertical Blank	16
R17	Mode Control	17
R18	Line Compare	18
R(F9)	400 Line Register	F9

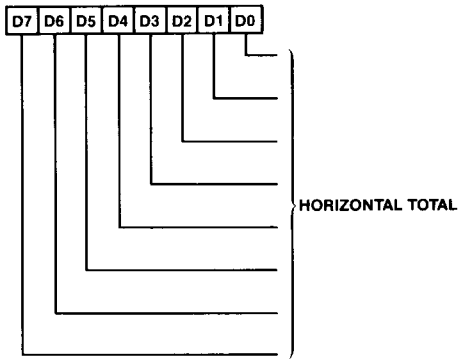
Address Register

The Address register contains the pointer to the I/O registers which can be written to in subsequent writes by the CPU. The Address register itself is selected by A0 = 0. Data bus bits D0-D4 contain the pointer to the I/O registers.



Horizontal Total Register (R0)

The Horizontal Total register is a write-only register. It can be written into by setting the pointer in the Address register to 00H, and writing to the chip with A0 = 1. All the registers described in the following pages will be addressed similarly. Any difference will be pointed out specifically.



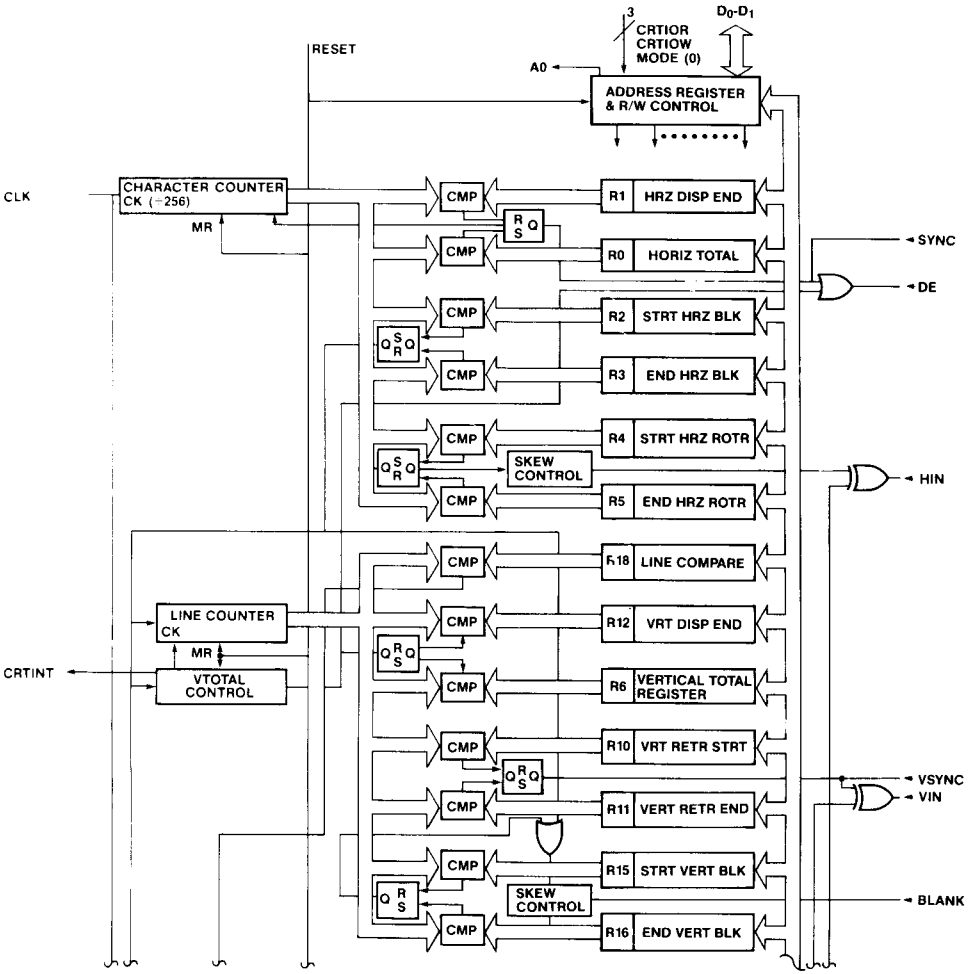


Figure 14. 82C434A Function Diagram

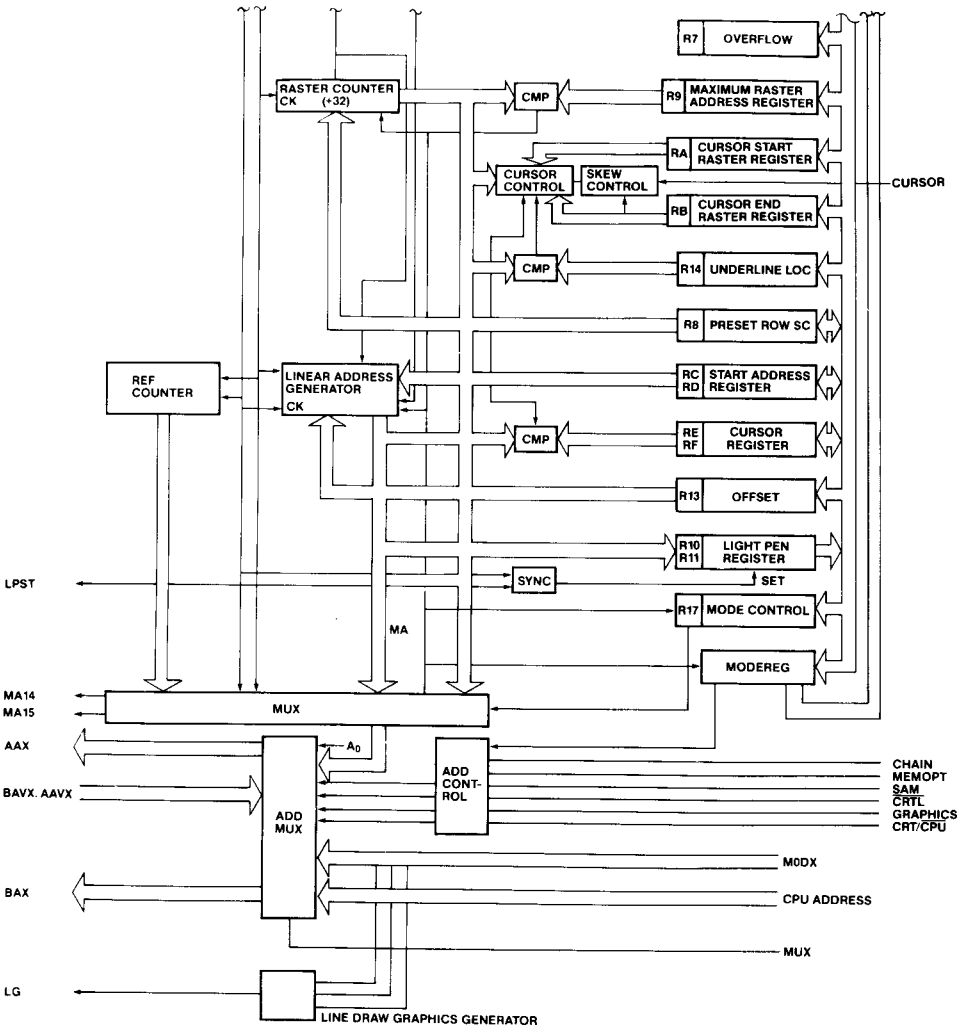


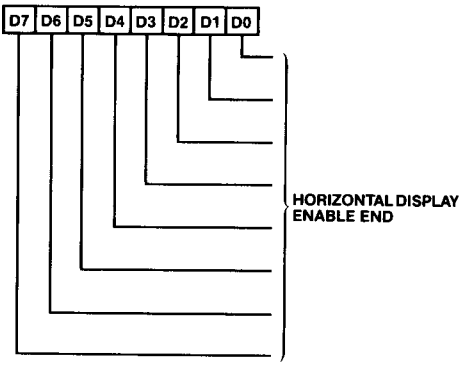
Figure 14. 82C434A Function Diagram (continued)

The Horizontal Total register defines the total number of characters in a horizontal scan line, including the retrace time. Together with the value in the Retrace timing registers R4 and R5, the period of the retrace output signal is determined by the value in this register. The character clock input to the device is counted by a character counter. The value of the character counter is compared with the value in this register to provide the horizontal timing. All horizontal and vertical timings are based upon the contents of this register.

The value in the register is equal to Total number of characters less 2.

Horizontal Display Enable End Register (R1)

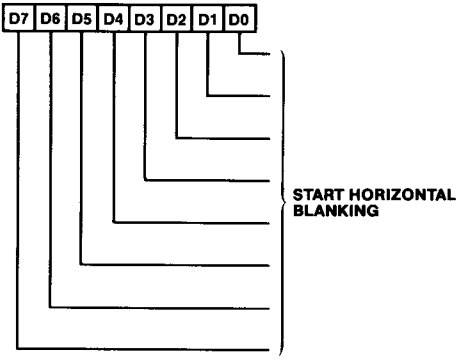
Write-only register.
Address register pointer: 01H
A0 = 1.



The Horizontal Display Enable End register defines the number of characters to be displayed per horizontal line. The actual characters displayed per horizontal line is one less than the contents of this register.

Start Horizontal Blanking Register (R2)

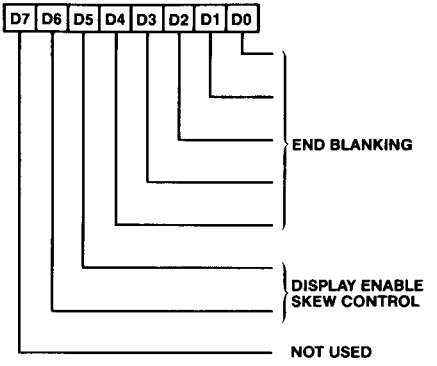
Write-only register.
Address register pointer: 02H
A0 = 1.



The contents of this register define the time when the horizontal blanking will start. The register is defined in terms of the number of horizontal character clocks. The horizontal blanking signal becomes active when the horizontal character count is equal to the contents of this register. The underline scan line decode output is multiplexed on the cursor output during the blanking period. The underline signal is valid for one character count beyond the end of blanking signal.

End Horizontal Blanking Register (R3)

Write-only register.
Address register pointer: 03H
A0 = 1.



The contents of this register define the time when the horizontal blanking will terminate. The register is defined in terms of the number of horizontal character clocks. The underline scan line decode output is multiplexed on the cursor output during the blanking period. The underline signal is valid for one character count beyond the end of blanking signal.

D0–D4 End Horizontal Blanking: The horizontal blanking signal width W is determined by the following algorithm:

Value in Start Blanking register + Width of Blanking signal W = 5-bit value to be programmed in End Horizontal Blanking register.

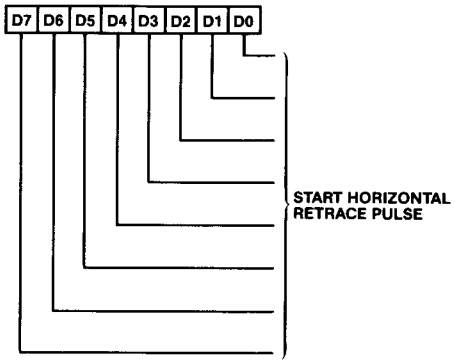
The five least significant bits of the horizontal scan line register are compared with the contents of this register. When a match occurs, the horizontal blanking pulse becomes inactive. Note that the five bits of this register limit the length of the blanking pulse to be 31 character clocks.

D5–D6 Display Enable Skew Control: Prior to displaying data on the screen, the CRT Controller has to access the display buffer to obtain a character to be displayed, access the attribute code, access the character generator font, and finally read the Pixel Panning register in the 82C433 Attributes Controller. Each one of these accesses require the display enable signal to be skewed by one character clock to allow for synchronization with the horizontal and vertical retrace pulses. The display enable skew bits in this register allow for this skew. The skew can be programmed from 0–3 character clocks as follows:

D6	D5	Skew in character clocks
0	0	0
0	1	1
1	0	2
1	1	3

Start Horizontal Retrace Pulse Register (R4)

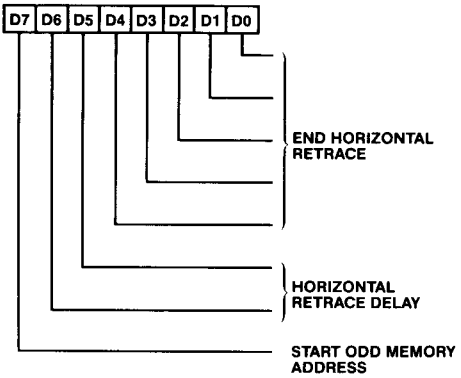
Write-only register.
Address register pointer: 04H
A0 = 1.



This register defines the character position at which the Horizontal Retrace Pulse becomes active. It is used to center the monitor screen horizontally. The value in the register is the character count at which the Horizontal Retrace Pulse becomes active.

End Horizontal Retrace Pulse Register (R5)

Write-only register.
Address register pointer: 05H
A0 = 1.



The contents of the register define the character count at which the Horizontal Retrace Pulse becomes inactive.

D0-D4 End Horizontal Retrace: The horizontal retrace signal becomes inactive after the character count becomes equal to the count in these bits. The width W of the retrace signal is determined by the following algorithm:

Value in Start Retrace register + Width of Retrace signal W in character clocks = 5-bit result to be programmed in End Horizontal Retrace register.

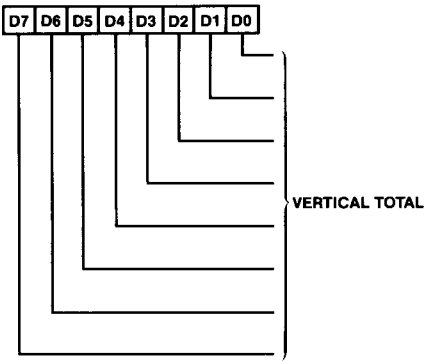
The five least significant bits of the horizontal scan line counter are compared to the contents of this register. When a match occurs, the horizontal retrace pulse becomes inactive. Note that the 5 bit register limits the length of the retrace signal to 31 character clocks maximum.

D5-D6 Horizontal Retrace Delay: The skew of the horizontal retrace signal is controlled by these bits. In some modes, it is necessary to provide a horizontal retrace signal that takes up the entire blanking period. The horizontal retrace signal also triggers some internal timings on the falling edge of the signal. To ensure that the signals are latched properly, the retrace signal is started before the end of the display enable signal. It is then skewed several character clock times to provide the proper screen centering.

D7 Start Odd/Even Memory Address: This bit determines the CRT memory address after a horizontal retrace. D7 = 0 selects an even address, and D7 = 1 selects an odd address. In most cases this bit should be set to '0'. The bit is useful in applications where horizontal pixel panning is required.

Vertical Total Register (R6)

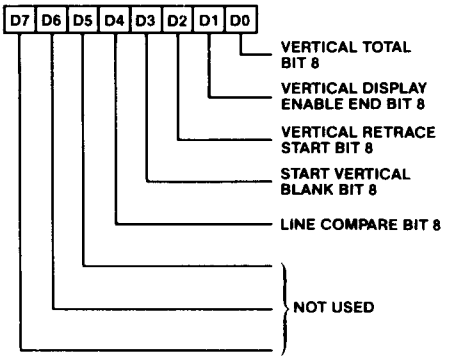
Write-only register.
Address register pointer: 06H
A0 = 1.



The Vertical Total register contains the low order 8 bits of a 9 bit register. The ninth bit is located in the CRT Controller Overflow register. The Vertical Total register defines the horizontal raster scans on the CRT screen, including the vertical retrace.

CRT Controller Overflow Register (R7)

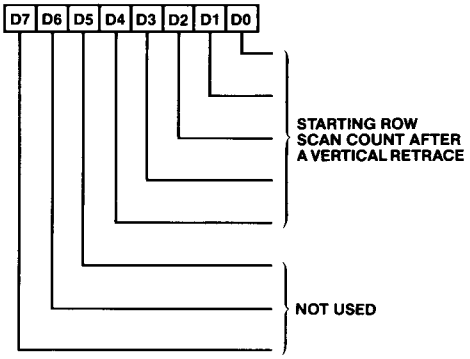
Write-only register.
Address register pointer: 07H
A0 = 1.



The CRT Controller Overflow register contains the ninth bit (D8) of several other control registers. This register is used in conjunction with registers for which it stores the ninth bit.

Preset Row Scan Register (R8)

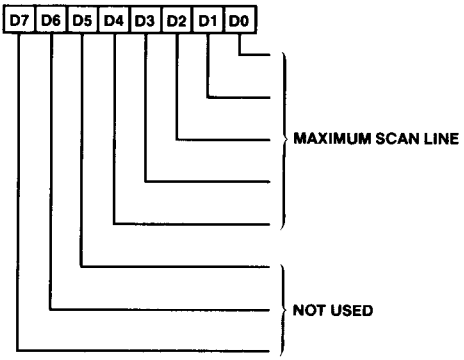
Write-only register.
Address register pointer: 08H
A0 = 1.



D0-D4 of the Preset Row Scan register specify the starting row scan count after a vertical retrace. Each horizontal retrace increments the horizontal row scan counter. The horizontal row scan counter is cleared at maximum row scan count, which is programmed through register R9. In the Hercules Graphics or CGA compatible modes, this register can be used for soft scrolling by setting the register value between 0 and 3. For example, by setting the start scan row address to 1 instead of 0, the next frame will start at address 1, which will give the effect of shifting vertically by 1 row, or vertical scrolling.

Maximum Scan Line Register (R9)

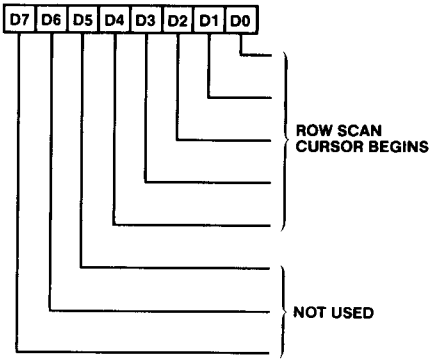
Write-only register.
Address register pointer: 09H
A0 = 1.



The contents of the Maximum Scan Line register specifies the number of scan lines per character row minus one.

Cursor Start Register (RA)

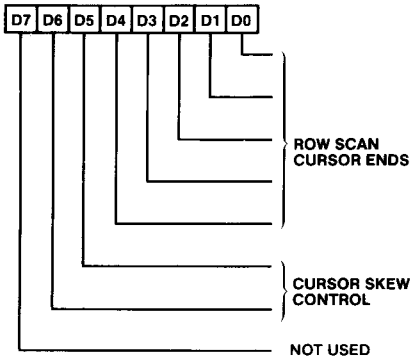
Write-only register.
Address register pointer: 0AH
A0 = 1.



The Cursor Start register defines the row scan of a character line where a cursor is to begin. The value in the register is one less than the starting cursor row scan.

Cursor End Address (RB)

Write-only register.
Address register pointer: 0BH
A0 = 1.



The Cursor End register defines the row scan of a character line where the cursor has to end. It also controls the cursor skew as described below:

D0-D4 D0-D5 define the row scan where the cursor is to end.

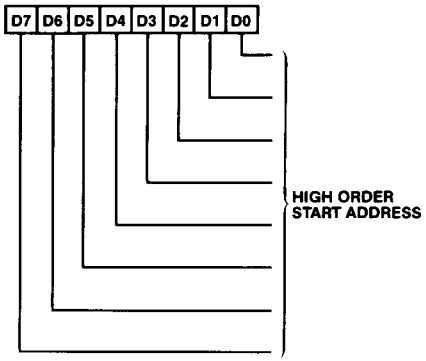
D5-D6 The cursor skew is controlled by these two bits. The bits control the skew as follows:

D6	D5	Skew
0	0	One character skew
0	1	One character skew
1	0	Two character skew
1	1	Three character skew

The Cursor Start and End registers allow a cursor to be up to 32 scan lines in height be placed on any scan line of the character block. The values in the Start and End registers define the height of the cursor.

Start Address High Register (RC)

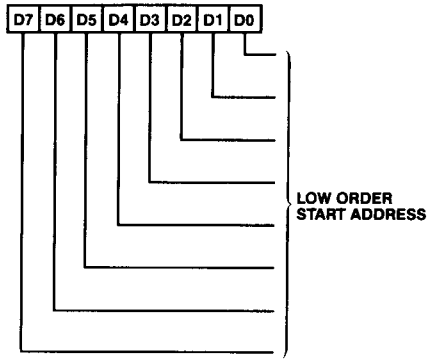
Read/Write register.
Address register pointer: 0CH
A0 = 1.



The Start Address is a 16-bit value which specifies first address after a vertical retrace at which the display on the screen begins on each screen refresh. This register contains 8 high order bits of the address, while the Start Address Low register specifies the other 8 low order bits.

Start Address Low Register (RD)

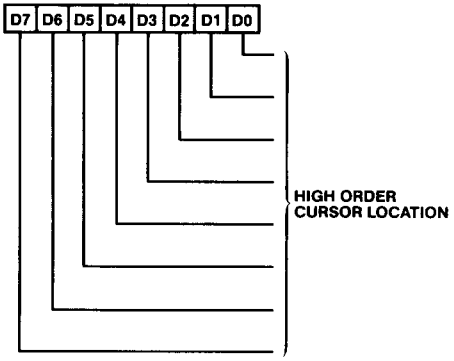
Read/Write register.
Address register pointer: 0DH
A0 = 1.



As explained above, the Start Address Low register contains the 8 low order bits of the Start Address.

Cursor Location High Register (RE)

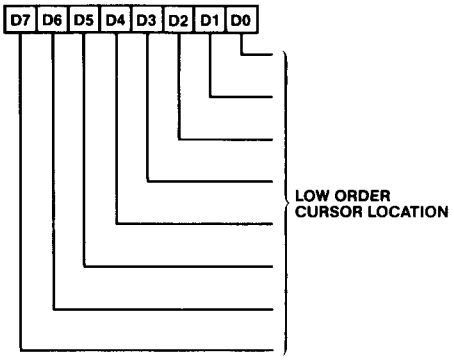
Read/Write register.
Address register pointer: 0EH
A0 = 1.



The Cursor Location High register is a read/write register. The address is a 16-bit value. The 8 high order bits are programmed in this register. The other 8 low order bits are programmed in the Cursor Address Low register. The 16 bit address defines the start address for the cursor in the 64K bytes of display RAM memory. Note that the 64K bytes correspond to one plane in the display memory. This allows hardware paging and scrolling through the memory without loss of the original cursor position.

Cursor Location Low Register (RF)

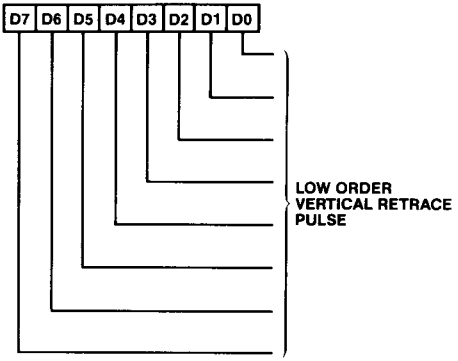
Read/Write register.
Address register pointer: 0FH
A0 = 1.



In conjunction with the Cursor Location High register, the Cursor Location Low register defines the low order 8 bits of the Cursor location.

Vertical Retrace Start Register (R10)

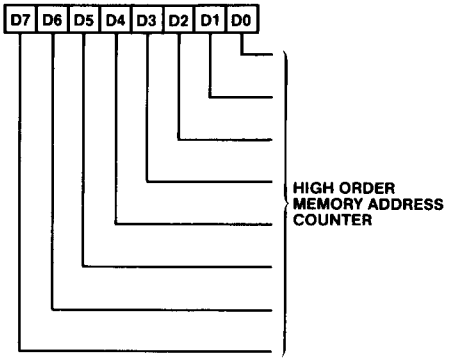
Write-only register.
Address register pointer: 10H
A0 = 1.



The Vertical Retrace Start register is a 9-bit address which defines the position of the vertical retrace start signal in terms of the number of horizontal scan lines. The low order 8 bits are programmed through this register, while the high order ninth bit is programmed through the Overflow register R7.

Light Pen High Register (R10)

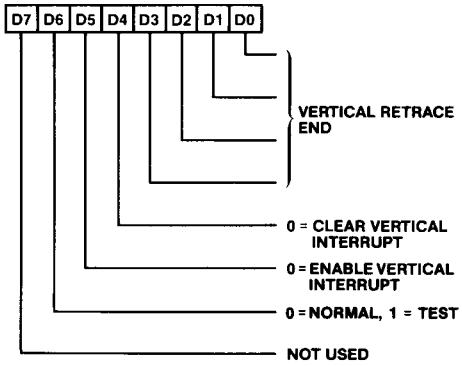
Read-only register.
Address register pointer: 10H
A0 = 1.



The Light Pen High register contains the 8 high order bits of the memory address at which time the light pen strobe signal was triggered. The low order 8 bits are stored in the Light Pen Low register (R11 read-only register).

Vertical Retrace End Register (R11)

Write-only register.
Address register pointer: 11H
A0 = 1.



Vertical Retrace End register performs multiple functions, as described below:

D3-D0 Vertical Retrace End: The 4 bits specify the horizontal scan line count at which the vertical retrace output pulse becomes inactive. The four bits are compared with the four least significant bits of the horizontal scan line counter. When the four counter bits are equal to the contents in this register, the vertical retrace is terminated. The Width W of the vertical retrace pulse can be determined from the following algorithm:

Value of Start Vertical Retrace register + W =

4 bit value to be programmed into the End Vertical Retrace register. Note that the four least significant bits of the algorithm result are to be programmed into this register. Thus the maximum retrace pulse width can only be 15 character clocks.

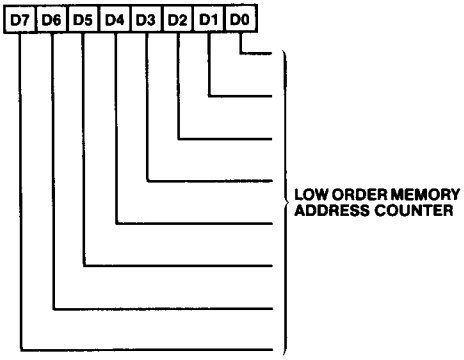
D4 Clear Vertical Interrupt: This bit is used to clear the vertical interrupt generated on the CRTINT output of the CRT Controller. A logical 0 will clear the interrupt. The CRTINT output is tri-stated when not active.

D5 A logical 0 will enable the vertical interrupt of the CRT Controller.

D6 Test: For normal operation this bit must be set to logical 0.

Light Pen Low Register (R11)

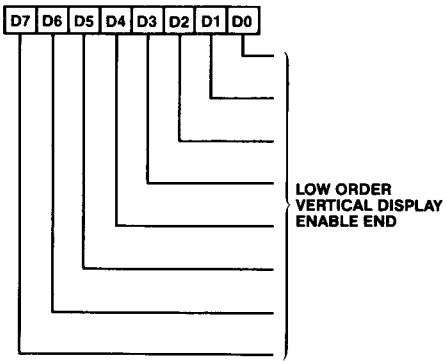
Read-only register.
Address register pointer: 11H
A0 = 1.



The Light Pen Low register contains the low order 8 bits of the address at which the light pen strobe was triggered.

Vertical Display Enable End Register (R12)

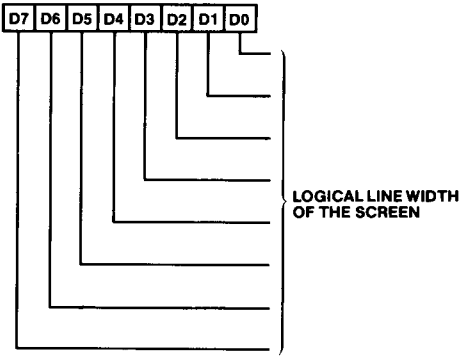
Write-only register.
Address register pointer: 12H
A0 = 1.



The Vertical Display Enable End register defines 8 bit of the 9-bit address which specifies the scan line position where the display on the screen ends. The ninth bit is located in the overflow register R7.

Offset Register (R13)

Write-only register.
Address register pointer: 13H
A0 = 1.



The Offset register contents define the logical line width of the screen. The starting address of the next character row is determined by the value in the the Offset register.

Figure 15 illustrates a functional diagram of how the Offset register is used. The register start address is sent to the memory address counter. When the memory address counter counts bytes, the next line address is the current line start address + 2*Offset register contents. This is illustrated in the figure by the fact that the adder has one of the input port's least significant forced to a logical 0. When the memory address counter is counting words, the next line address is the current line start address + 4*Offset register contents. The byte or word mode for the memory address counter is selected by the Mode Control register R17, bit 6. The Start address High and Low bytes in the figure correspond to the first address after a vertical retrace at which the display on the screen begins. The multiplexer switches the control over to the address sum port, after the first line has been scanned.

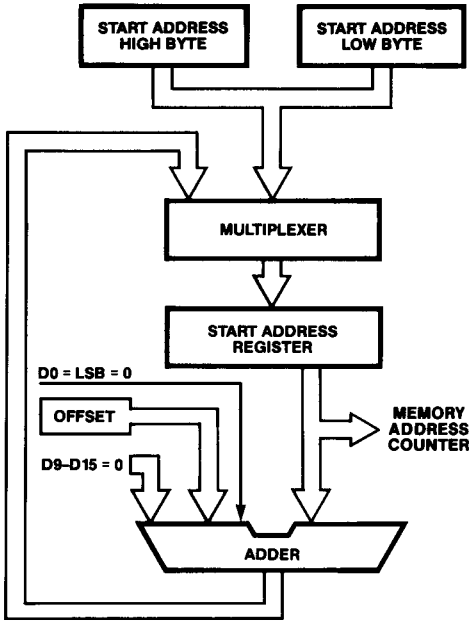
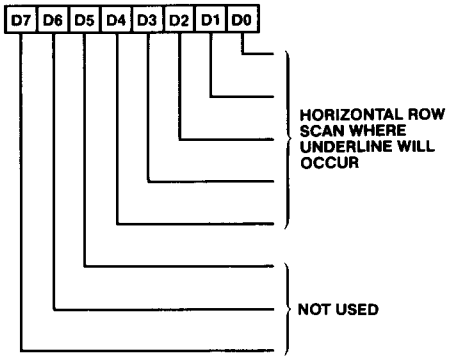


Figure 15. Offset Register Operation

Underline Location Register (R14)

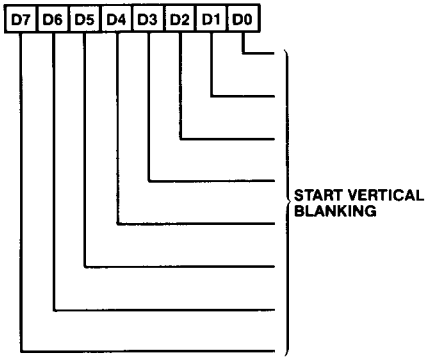
Write-only register.
Address register pointer: 14H
A0 = 1.



The Underline Location register specifies the horizontal row scan count at which the underline will occur. The value in the register is one less than the desired scan line number.

Start Vertical Blanking Register (R15)

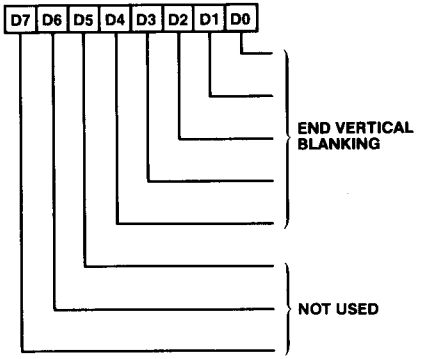
Write-only register.
Address register pointer: 15H
A0 = 1.



The Start Vertical blanking register contain the low order 8 bits of the horizontal scan line count at which the vertical blanking pulse becomes active. The ninth bit is located in the Overflow register R7.

End Vertical Blanking Register (R16)

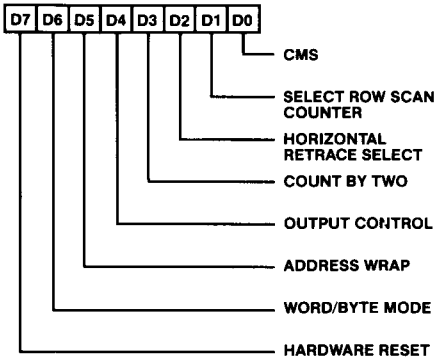
Write-only register.
Address register pointer: 16H
A0 = 1.



The End Vertical Blanking register specifies the horizontal scan line count at which the vertical blanking pulse becomes inactive. The vertical blanking width W is determined from the following algorithm: Value of Start Vertical register + W = 5-bit value to be programmed into the End Vertical Blanking register. The five least significant bits of the algorithm result are programmed into this register. When the five least significant bits of the horizontal scan line counter are equal to the value in this register, Vertical Blanking is terminated. Note that the maximum width of the vertical blanking is limited to 31 character clocks.

Mode Control Register (R17)

Write-only register.
Address register pointer: 17H
A0 = 1.



Mode Control register is a multi-function register, with each bit defining a different option. Following is a description of these bits:

D0 Compatibility Mode Support: This bit allows compatibility with the IBM Color Graphics Adapter. When D0=0, the row scan address bit 0 is substituted for memory address bit 13 during active display time. When D0=1, no such substitution takes place.

D1 Select Row Scan Counter: This bit allows compatibility with the Hercules graphics card and with any other 400 line graphics system. D1=0 selects the row scan counter bit 1 on MA 14 output pin. D0=1 selects row scan counter bit 14 on MA14 output pin.

D2 Horizontal Retrace Select: This bit controls the vertical resolution capability of the CRT Controller. The vertical counter has a maximum resolution of 512 scan lines as defined by the Vertical Total register. If the vertical retrace counter is clocked with the horizontal retrace clock divided by 2, then the vertical resolution is doubled to 1024 horizontal scan lines. D2=0 selects the horizontal retrace clock, and D2=1 selects the horizontal retrace clock divided by 2.

D3 Count By Two: This bit selects the character clock as the clock input or character clock divided by 2 as the character clock. This bit defines whether the contents of the Offset register are a word or a double word value. When D3=0, the memory address counter is clocked by the character clock input. When D3=1, the memory address is clocked by the character clock input divided by 2. This bit is also used to create either a byte or word refresh address for the display memory.

D4 Output Control: D4 = 0 enables the output drivers of the CRT Controller, D4=1 will tri-state the following outputs of the CRT Controller: VRTC, SYNC, BLANK, CURSOR, DE, MA14 and MA15.

D5 Address Wrap: This bit selects memory address counter bit MA13 or MA15. When a byte mode is selected through D6 of this register, MA0 counter output appears on the MA0 output pin. When word mode is selected through D6 of this register, either MA13 or MA15 appears on the MA0 output pin. MA13 or MA15 selection depends on the size of memory selected through the MEMOPT pin. When the 64K byte option is configured, MA13 is selected through D5=0. When greater than 64K bytes is configured, and D5 is set to logical 1,then MA15 is selected to be an output on the MA0 output pin. This bit is useful in implementing the IBM Color Graphics Adapter mode.

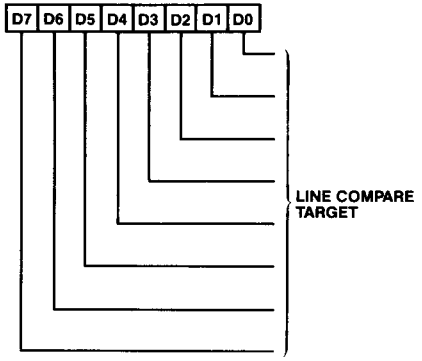
D6 Word Mode or Byte Mode: When D6=0, Word Mode is selected. This mode causes the memory address counter bits to shift down one bit, and the most significant bit of the counter appears on the least significant bit of the memory address output. D6=1 selects the Byte mode.

D7 Hardware Reset: A logical zero clears vertical and horizontal retraces. A logical "1" enables the vertical and horizontal retraces.

	Internal Memory Address Counter Wiring to the Output Multiplexer	
CRTC Out Pin	**Byte Address Mode**	**Word Address Mode**
MA 0	MA 0	MA 15 or MA 13
MA 1	MA 1	MA 0
MA 2	MA 2	MA 1
MA 3	MA 3	MA 2
—	—	—
—	—	—
—	—	—
MA 14	MA 14	MA 13
MA 15	MA 15	MA 14

Line Compare Register (R18)

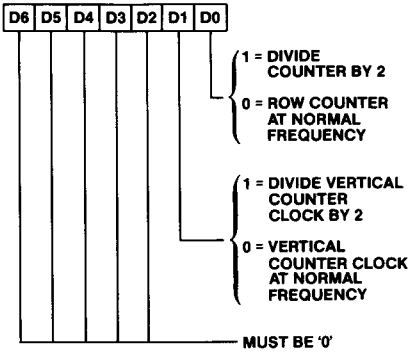
Write-only register.
Address register pointer: 18H
A0 = 1.



The Line Compare register is used to implement a split screen function. When the horizontal scan counter value is equal to the contents of this register, the memory address generator is cleared to 0. The linear address generator then sequentially addresses the display buffer starting at address 0. Each subsequent row address is determined by the 16-bit addition of the Start of Line Latch and the Offset register contents. This feature allows a given area on the screen to be immune to scrolling. The scrolling operation utilizes the Start Address High and Low registers, and the split screen screen capability will allow scrolling through some areas of the screen while the remaining screen remains immune to it.

400-Line Register (R F9)

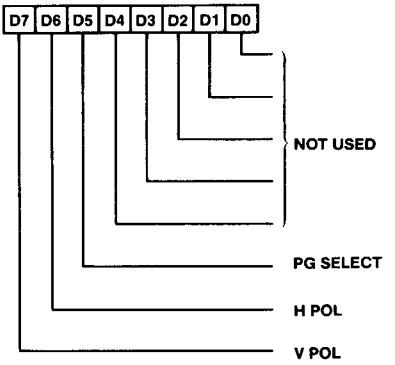
Write-only register.
Address register pointer: 0F9 H
A0 = 1



The 400-Line Register is added to the 82C34A to allow the CRT Controller to be used with 400-Line monitors. The 400-Line Mode (200-line double scan) can be selected by setting D0 = 1 and D1 = 1. Note that the D1 = 1 will divide the Vertical Counter Clock by 2. This is in addition to the divide by 2 option selected by Register R17, bit D2, Power-on reset will clear the bits D0 and D1 to '0' in the R(F9) register.

Mode Register

The Mode register is written to by activating the MODEIOW input to the CRT Controller. The address inputs A0-A2 are don't care inputs in this case.



The Mode register uses three most significant bits D7-D5. These three bits perform the following functions:

D5 D5 is the least significant bit of the display RAM address when the inputs SAM = MEMOPT = 0, and CHAIN input = 1. See Table 1 for more details on this.

D6 D6 selects the polarity for the Horizontal Sync pulse.
0 Positive horizontal sync pulse
1 Negative horizontal sync pulse

D7 D7 selects the polarity for the Vertical Sync pulse.
0 Positive vertical sync pulse
1 Negative vertical sync pulse

As described in the preceeding text, the CRT Controller provides all the timing and control signals for the display monitor. Figure 16 shows a graphic illustration of how the contents of these registers control the display screen. The horizontal blanking signal is controlled by the contents of R2 and R3 registers. Similarly, the contents of R15 and R16 determine the location and length of the vertical blanking signal. The screen blanking signal BLANK is a logical 'OR' of H_BLANK and V_BLANK signals. The horizontal sync start location and width are controlled by the contents of R4 and R5 registers, while the vertical sync start location and width are controlled by the R10 and R11 registers. R0 controls the total number of characters in the horizontal scan interval, including the retrace time. The total number of scan lines on one raster are determined by the vertical total register R6. R1 and R12 define the effective display area on the screen by specifying the horizontal and vertical display enable positions, respectively.

Split Screen

The CRT Controller is also capable of displaying split screens. Figure 16 also shows a split screen display. The two screens, Screen 1 and Screen 2, are created by properly setting the Memory Address registers (RC and RD) and the Line Compare register (R18). The RC and RD register contents specify the memory address for the first pixel to be displayed on the active screen. Thus Screen 1 in figure 16 start address is determined by the contents of the registers RC and RD. Split screens are created with the use of Line Compare register R18. The internal start of the scan line counter is cleared when the vertical counter reaches the value equal to the contents of R18. Thus Screen 2 in figure 16 starts at address location 0000H. The linear address generator addresses the display buffer sequentially starting at 0000H. Each subsequent row address is determined by the Offset register contents as described earlier under register description.

SAM	CHAIN	MEMOPT	LSB	Comment
0	0	0	A0	
0	0	1	A0	
0	1	0	PGSEL	PGSEL is $\overline{D5}$ of data loaded by $\overline{MODEIOW}$
0	1	1	A14	
0	0	0	A0	
1	0	1	A0	
1	1	0	A16	
1	1	1	A0	

Table 1. LSB Address Select Scheme

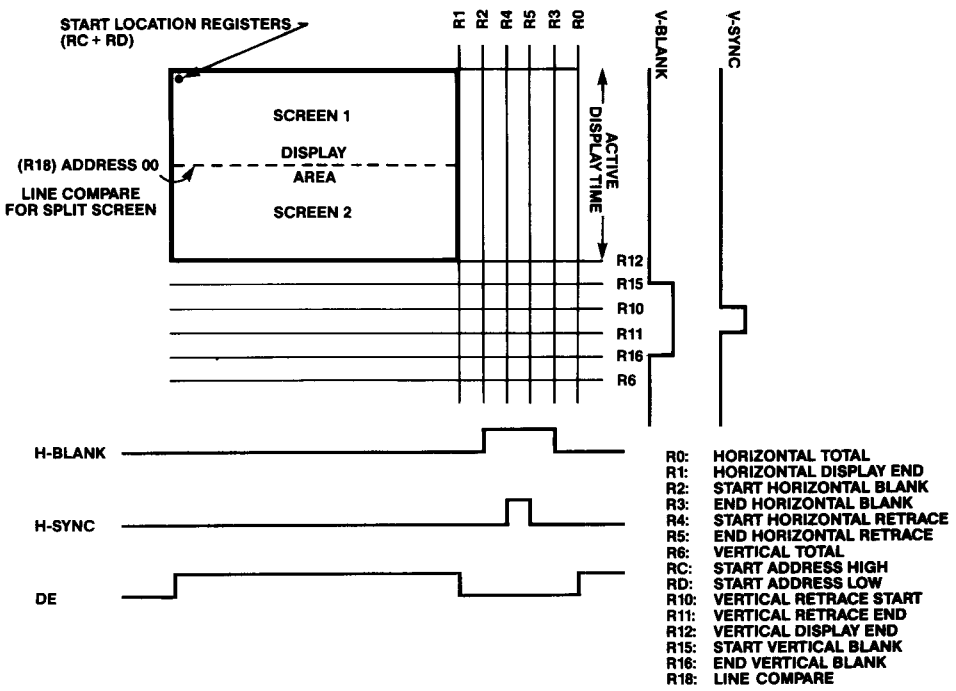


Figure 16. 82C434A Display Timing Sequence

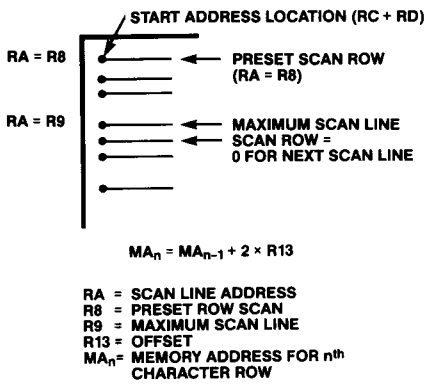


Figure 17. Soft Scroll Using the CRT Controller

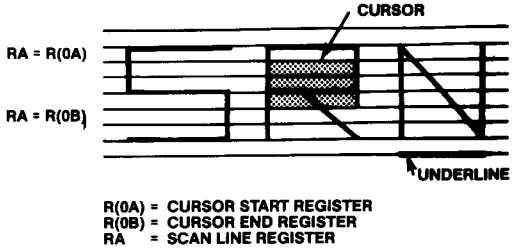


Figure 18. CRT Controller Cursor Control

Soft Scroll

The CRT Controller offers soft scrolling capability by presetting a value in the Preset Scan Register, R8. Figure 17 shows a typical example of how this can be achieved. As described earlier in the graphics display mode, the start address registers RC and RD define the address of the first pixel that is displayed on the screen. In the alphanumeric mode, the start address is the address of the first character which will be displayed in the first row. The Preset Scan Row register defines the starting row scan at which the display is actually started. The start address is latched by the CRT Controller during the vertical retrace period. The Preset Scan register is also loaded into the row scan counter during the same period. By updating the Start Address registers and the Preset Scan register, a smooth vertical scrolling effect can be created at a desired scroll rate. Note that the Preset Scan register should be set to zero for graphics modes. In this case the vertical scrolling can be controlled by updating the Start Address registers only. Figure 17 also illustrates how subsequent addresses are computed for a given raster scan.

Cursor Control

The height of the CURSOR is programmable through registers RA and RB. The memory address of the CURSOR is programmable through registers RE and RF. Figure 18 shows how the CURSOR height is controlled by setting the horizontal scan line equal to the contents of RA and then RB registers. In the same way, the underline is also controlled by setting the scan line counter one less than the contents of the underline register R14.

Vertical Interrupt

The 82C434A CRT Controller generates an interrupt at the end of a vertical display. The Vertical Display End controls the time when the interrupt becomes active. The interrupt can be used by the CPU to update the Enhanced Graphics CHIPSet during the vertical blanking interval. The interrupt output CRTINT is tri-stated when interrupt is in-active.

82C434A Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	V_{DD} + .5	V
Output Voltage	V_O	-0.5	V_{DD} + .5	V
Operating Temperature	T_{op}	-25	85	C
Storage Temperature	T_{stg}	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C434A Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	C

82C434A DC Characterisitcs

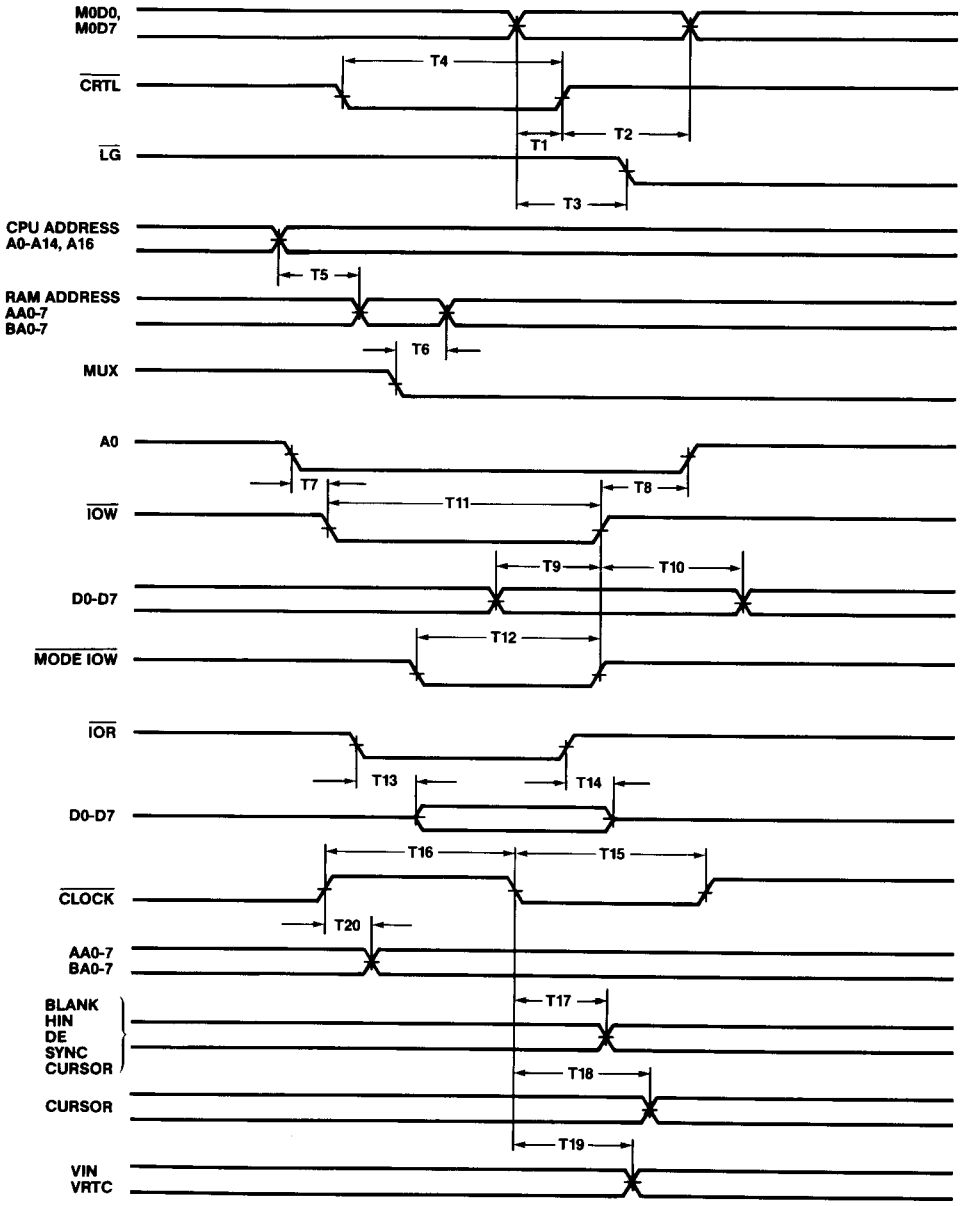
Parameter	Symbol	Min.	Max.	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage (Note 1)	V_{IH}	2.0		V
Output Low Voltage I_{OL1}=2mA (Note 2) I_{OL2}=4mA (Note 3) I_{OL3}=8mA (Note 4)	V_{OL}		0.45	V
Output High Voltage I_{OH}= (Note 5)	V_{OH}	3.5		V
Input Low Current $0 < V_{IN} < V_{CC}$	I_{IL}		±10	μA
Output Short Circuit Current V_O=0V	I_{OS}		20	mA
Power Supply Current @ 4 MHz Clock	I_{CC}		20	mA
Output HI-Z Leak Current $0.45 < V_{OUT} < V_{CC}$	I_{OZ1}		±10	μA

NOTES:
1. The following inputs require V_{IH} = 3.0V (min.) D0-D7, BAV14-15, AAV14-15, MUX, CHAIN, GRAPHICS, CRT/CPU, CLOCK, CRTL. All other inputs require V_{IH} = 2.0 V (min.).
2. For VRTC, SYNC CURSOR and DE only.
3. For CRTINT, BLANK, and VIN only.
4. All other outputs and bidirectional pins.
5. I_{OH} for the pin equal to I_{OL} for that pin.

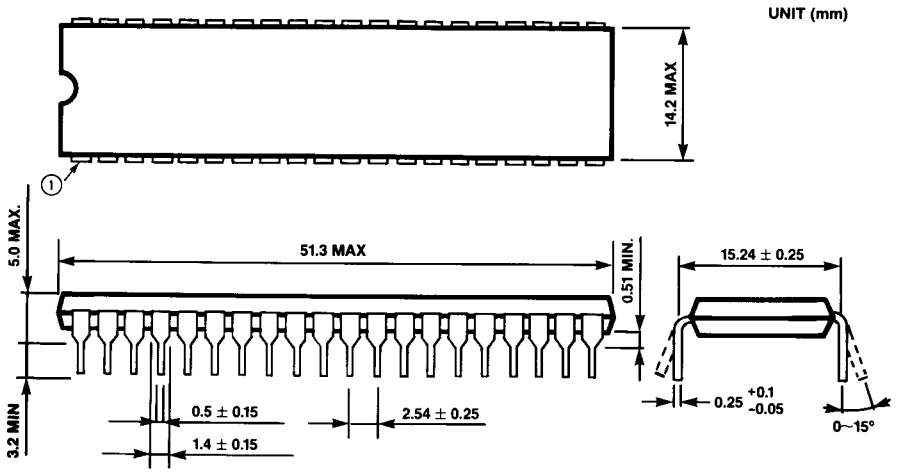
82C434A AC Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

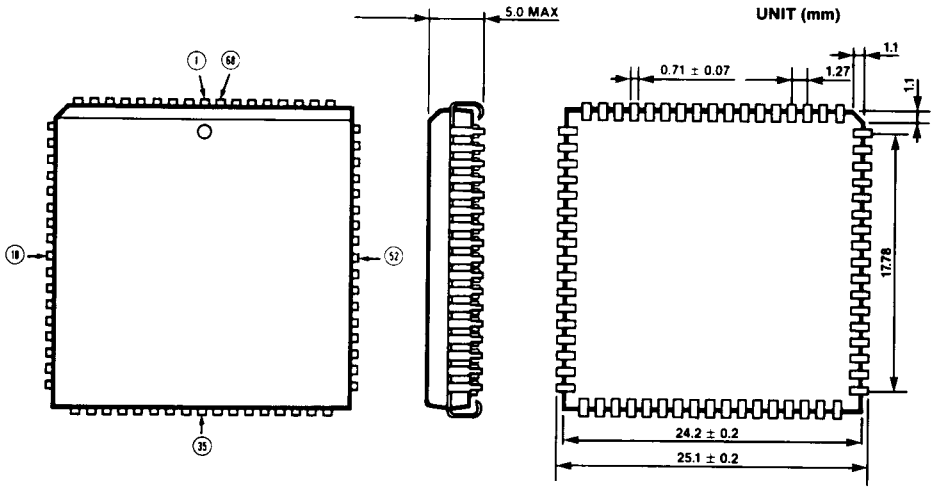
Sym	Description	Min.	Max.	Units
t1	M0D0-D0D7 set-up to CRT Latch ($\overline{CRTL}$) going high	5	—	ns
t2	M0D0-D0D7 hold time after CRT Latch ($\overline{CRTL}$) goes high	25	—	ns
t3	M0D0-D0D7 set-up to Line Graphics (LG) delay	—	36	ns
t4	CRT Latch ($\overline{CRTL}$) low period	50	—	ns
t5	CPU addresses to RAM addresses delay	4	60	ns
t6	MUX to RAM address delay	3	40	ns
t7	Address A0 to transistion to $\overline{IOW}$ low delay	25	—	ns
t8	$\overline{IOW}$ going high to address A0 transition	25	—	ns
t9	Data set-up time to $\overline{IOW}$ or $\overline{MODEIOW}$ high	40	—	ns
t10	Data hold after $\overline{IOW}$ or $\overline{MODEIOW}$ go high	25	—	ns
t11	$\overline{IOW}$ low period	140	—	ns
t12	$\overline{MODEIOW}$ low period	100	—	ns
t13	$\overline{IOR}$ active to data valid	4	40	ns
t14	$\overline{IOR}$ in-active to data bus tri-state	2	30	ns
t15	Clock low period	140	—	ns
t16	Clock high period	110	—	ns
t17	Clock low to BLANK, HIN, DE, SYNC and CURSOR (for cursor) delay	2	60	ns
t18	Clock low to CURSOR for underline delay	—	135	ns
t19	Clock low to VIN and VRTC delay	—	100	ns
t20	Clock high to RAM address delay	3	40	ns


M0D0,
M0D7
T4
CRTL
T2
T1
LG
T3
CPU ADDRESS
A0-A14, A16
T5
RAM ADDRESS
AA0-7
BA0-7
T6
MUX
A0
T7
T8
T11
IOW
T9
T10
D0-D7
T12
MODE IOW
IOR
T13
T14
D0-D7
T16
T15
CLOCK
T20
AA0-7
BA0-7
T17
BLANK
HIN
DE
SYNC
CURSOR
T18
CURSOR
T19
VIN
VRTC

40-Pin Plastic Dual-In-Line Package

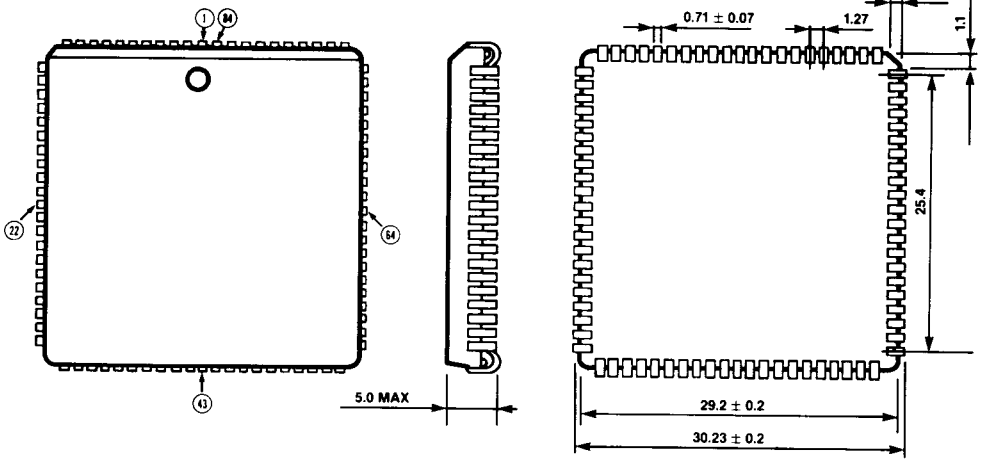


68-Pin Plastic Leaded Chip Carrier



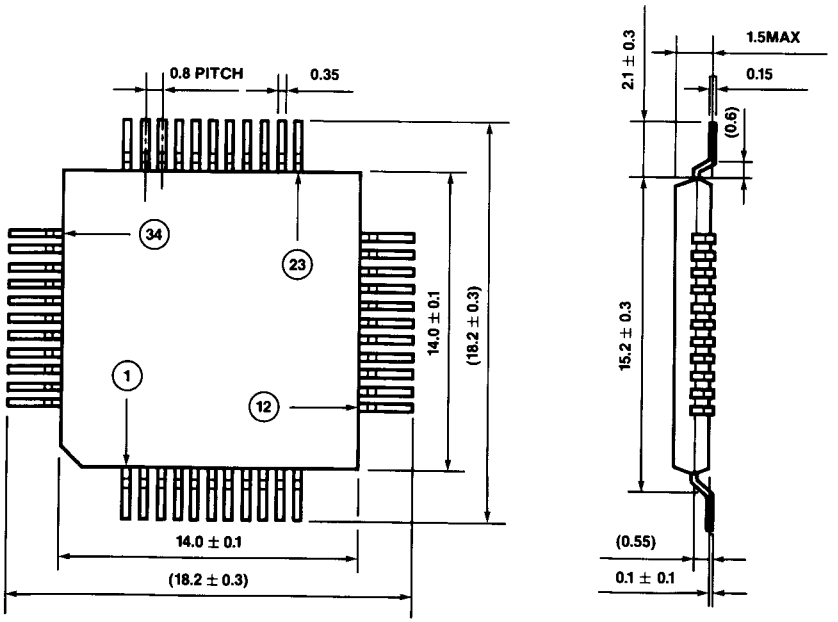
84-Pin Plastic Leaded Chip Carrier

UNIT (mm)



44-Pin Plastic Flat Package

UNIT (mm)



Ordering Information

Order Number	Package Type Note 1	Operating Range Note 2
P82C431	PLCC-68	C
P82C432A	PDIP-40	C
F82C432A	PFP-44	C
F82C432B	PFP-44	C
P82C433	PDIP-40	C
F82C433	PFP-44	C
P82C434A	PLCC-84	C

NOTE 1: PLCC-84 Plastic Lead Chip Carrier in 84 pins
PDIP-40 Plastic Dual-in-Line in 40 pins
PFP-44 Plastic Flat Pack in 44 pins
NOTE 2: Commercial range, 0-70° C, ±5% Supply Voltage
NOTE 3: CHIPSet ordering should be done as follows:
CS8240 = P82C431 + P82C432A + P82C433 + P82C434A
CS8240A = P82C431 + F82C432A + F82C433 + P82C434A
CS8240B = P82C431 + F82C432B + F82C433 + P82C434A

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