# XRT56L85

Low Power
PCM Line Interface

October 2000-1

## FEATURES

- Low Power (Typical 14mA)
- Single +5V Supply
- Up to 2.048 Mbps Operation in Both TX and RX Directions
- Receiver Input can be:
  - Balanced Transformer Coupled
  - Capacitively (Twisted Pair)
  - Single Coaxial Capacitive Coupling

## APPLICATIONS

- T1 and CEPT Interfaces
- CPI
- DMI

## GENERAL DESCRIPTION

The XRT56L85 is a PCM line interface chip. It consists of both transmit and receive circuitry in a DIL 18 pin package. The maximum bit rate the chip can handle is 2.048 Mbps and the signal level to the received can be attenuated by 10dB of cable loss at half the bit rate. Total current consumption is between 12-16mA at +5V.

## ORDERING INFORMATION

| Part No. | Package | Operating Temperature Range |
|---|---|---|
| XRT56L85P | 18 Lead 300 Mil PDIP | -40°C to +85°C |
| XRT56L85D | 18 Lead 300 Mil JEDEC SOIC | -40°C to +85°C |

## BLOCK DIAGRAM

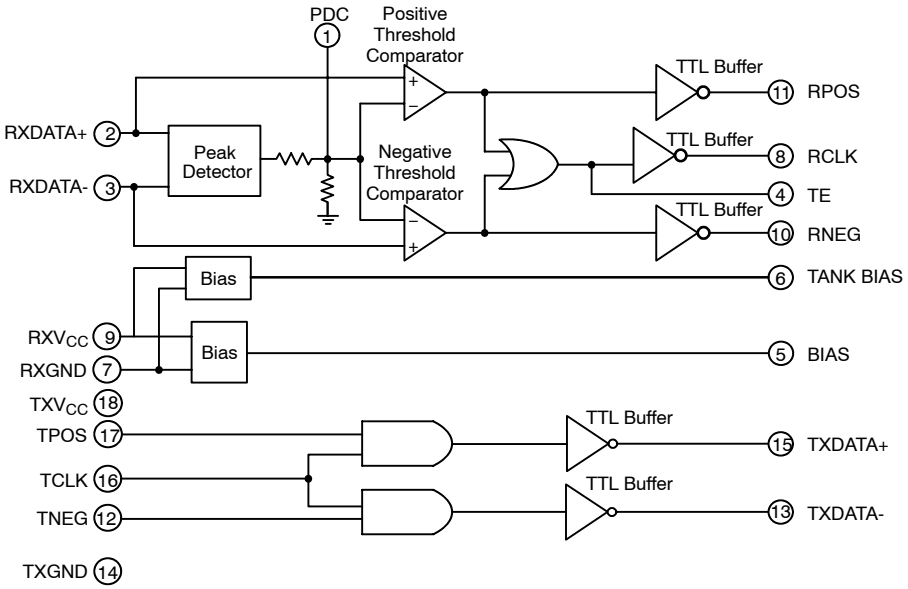


**Figure 1. Block Diagram**




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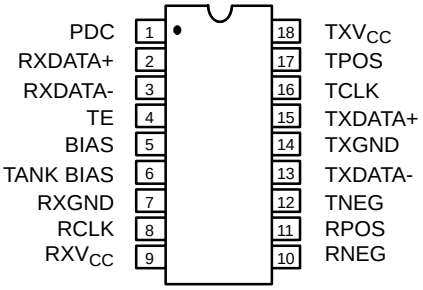
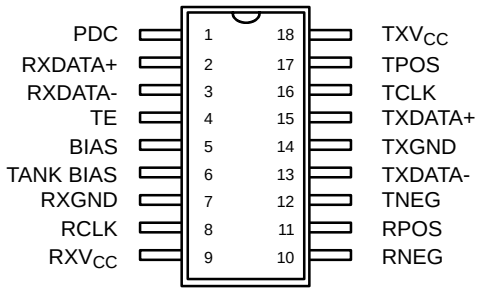
## PIN CONFIGURATION




**18 Lead PDIP (0.300")**




**18 Lead SOIC (Jedec, 0.300")**

## PIN DESCRIPTION

| Pin # | Symbol | Type | Description |
|---|---|---|---|
| 1 | PDC | | **Peak Detector Capacitor.** This pin should be connected to a 0.1μF capacitor |
| 2 | RXDATA+ | I | **Receive Analog Input Positive.** The AMI signal received from the line is applied at this and the RX DATA(-) pin. Data and clock from the signal applied at these two pins recovered and output on the RPOS, RNEG, and RCLK pins, respectively. |
| 3 | RXDATA- | I | **Receive Analog Input Negative.** See the description for RX DATA(+). |
| 4 | TE | O | **LC Tank Excitation Output.** This output connects to one side of the tank circuitry. |
| 5 | BIAS | O | **Bias.** This pin should be tied to ground through a 0.1μF capacitor. |
| 6 | TANK BIAS | | **Tank Reference.** The tank circuitry is biased via this output. |
| 7 | RXGND | | **Receiver Ground.** To minimize ground interference a separate pin is used to ground the receiver section. |
| 8 | RCLK | O | **Recovered Receive Clock.** Recovered clock signal from the AMI signal received at the RX DATA(+) and RX DATA(-) pins. This signal is output to the terminal equipment. |
| 9 | $RXV_{CC}$ | | **Receive Supply Voltage.** 5V supply voltage for the Receive Section. |
| 10 | RNEG | O | **Receive Negative Data Output.** A signal at this pin corresponds to the receipt of a negative pulse on the RX DATA(+)/RX DATA(-) pins. This TTL compatible signal is output to the terminal equipment. |
| 11 | RPOS | O | **Receive Positive Data Output.** A signal at this pin corresponds to the receipt of a positive pulse on the RX DATA(+)/RX DATA pins. This TTL compatible signal is outputed to the terminal equipment. |
| 12 | TNEG | I | **Transmit Negative Data Input.** TTL input for a negative polarity pulse (the negative portion of the AMI pulse train) to be transmitted to the line via the TX DATA(+) and TX DATA pins. |
| 13 | TXDATA- | O | **Transmit Negative Data Output.** This pin, along with the TX DATA(+) pin, forms a differential driver output, this is used to drive AMI data down the line via a transformer. Note: This is an open-collector output. |
| 14 | TXGND | | **Transmit Ground.** |
| 15 | TXDATA+ | O | **Transmit Positive Data Output.** Please see description for TX DATA(-). |
| 16 | TCLK | I | **Transmit Clock.** TPOS and TNEG are sampled on the rising edge of TCLK. |
| 17 | TPOS | I | **Transmit Positive Data Input.** TTL input for a positive polarity pulse (the positive portion of the AMI pulse train) to be transmitted to the line via the TX DATA(+) and TX DATA(-) pins. |
| 18 | TXVcc | | **Transmit Supply Voltage.** 5V supply voltage to the transmit section. |

## ELECTRICAL CHARACTERISTICS

**Test Conditions: $V_{CC}$ = 5V± 5%, $T_A$ = -40°C to +85°C, Unless Otherwise Specified**

| Parameters | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| **DC Electrical Characteristics** | | | | | |
| Supply Voltage | 4.75 | 5 | 5.25 | V | |
| Supply Current | | 14 | 16 | mA | Total Current to Pin 9 & Pin 18 (Transmitter Outputs Open and All Ones Pattern) |
| **Receiver Section** | | | | | |
| Tank Drive Current | 300 | 500 | 700 | µA | Measured at Pin 4, $V_{CC}$= 5V |
| Clock Output Low | | 0.3 | 0.6 | V | Measured at Pin 8, $I_{OL}$ = 1.6mA |
| Clock Output High | 3.0 | 3.6 | | V | Measured at Pin 8, $I_{OH}$ =400µA |
| Data Output Low | | 0.3 | 0.6 | V | Measured at Pin 10 & 11, $I_{OL}$ =1.6mA |
| Data Output High | 3.0 | 3.6 | | V | Measured at Pin 10 & 11, $I_{OH}$ =400µA |
| **Transmitter Section** | | | | | |
| Driver Output Low | 0.6 | 0.9 | 1.2 | V | Measured at Pin 13 & 15, $I_{OL}$ =-40mA |
| Output Leakage Current | | | 100 | µA | Measured in Off State<br>Output Pull-up to +20V |
| Input High Voltage | 2.2 | | | V | Measured at Pin 12, 16 & 17<br>$I_{OL}$ = -40mA, $V_{OL}$ = 1.0V |
| Input Low Voltage | | | 0.8 | V | Measured at Pin 12, 16 & 17<br>Output Off |
| Input Low Current | | | -1.6 | mA | Measured at Pin 12, 16 & 17<br>Input Low Voltage = 0.4V |
| Input High Current | | | 40 | µA | Measured at Pin 12, 16 & 17<br>Input Low Voltage = 0.4V |
| Output Low Current | | | -30 | mA | Measured at Pin 13 & 15<br>$V_{OL}$= 1.0V |
| **AC Electrical Characteristices** | | | | | |
| **Receiver Section** | | | | | |
| Input Level | | 6 | 6.6 | Vpp | Measured Between Pin 2 & 3 |
| Loss Input Signal Alarm Level | | 0.6 | | Vpp | Measured Between Pin 2 & 3<br>Alarm on Pull Data/Clock Output High |
| Input Impedance at 2.048MHz | | 2.5 | | kΩ | Measured Between Pin 2 & 3<br>With Sinewave Input |
| Clock Duty Cycle | 35 | 50 | 65 | % | Measured at Pin 8 at 2.0V DC Level |
| Clock Rise & Fall Time | | 20 | 40 | ns | Measured at Pin 8, CL = 15pF |
| Data Pulse Width | 35 | 50 | 75 | % of clock period | Measured at Pin 10 & 11<br>At 1V DC Level, Cable Loss = 6dB |
| **Transmitter Section** | | | | | |
| Pulse Width at 2.048MHz | 234 | 244 | 264 | ns | Measured at Pin 13 & 15 *Figure 3* |
| Output Rise Time | | 12 | 25 | ns | *Figure 3* |
| Output Fall Time | | 12 | 25 | ns | *Figure 3* |
| Output Fall Imbalance | | 2.5 | | ns | At 50% Output Level |

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . +20V

Storage Temperature . . . . . -65°C to 150°C .

## SYSTEM DESCRIPTION

### The Receiver

The incoming bipolar PCM signal, which is attenuated and distorted by the cable is applied to the receiver input, consisting of the RX DATA(+) and RX DATA(-) pins, either through a balanced transformer, a balanced capacitively coupled terminal or a single-ended coaxial cable (see *Figure 5*). A peak detector following the input generates a DC reference for the positive and negative threshold comparator (to extract the positive and negative data pulses). Information on the positive and negative data pulses is outputed as TTL compatible signals at pins RPOS and RNEG, respectively. More specifically, an output signal present at the RPOS pin indicates that a positive pulse was received at the RX DATA(+)/RX DATA(-) pins, from the incoming bipolar data stream. Likewise an output signal present at the RNEG pin indicates that a negative pulse was received at the RX DATA(+)/RX DATA(-) pins. This conversion from the bipolar signal to TTL compatible signals allows for digital processing of the clock and data signals by the terminal equipment. An example of the waveforms of the TTL compatible recovered clock and data as output by the receiver portion of the chip is presented in *Figure 2*, *Figure 3* and *Figure 5*. A tank circuit tuned to the appropriate frequency is added externally to provide the appropriate frequency-selective filtering of the received clock signal.

### The Transmitter

The transmitter portion of the chip receives TTL compatible signals and transmits a corresponding bipolar data stream down the line (See *Figure 5*). TPOS and TNEG are TTL compatible signals that dictate the polarity of the pulse to be generated and transmitted on the output bipolar data stream. Both TPOS and TNEG inputs are sampled by the rising edge of the transmit clock, TCLK. The TX DATA(+) and TX DATA(-) pins form a differential driver output, this is used to drive AMI data down the line via a transformer. The TX DATA(+) and TX DATA(-) pins are open-collector outputs.

When a logic “high” signal is applied to the TPOS pin, a positive pulse (the positive portion of the bipolar data stream) will be transmitted to the line via the TX DATA(+) O/P and TX DATA(-) O/P pins. Likewise, when a logic “high” signal is applied to the TNEG pin, a negative pulse will be transmitted to the line via the TX DATA(+) and TX DATA(-) pins. An illustration of the key waveforms involved in this TTL to AMI conversion process, in the Transmitter portion of the chip is presented in *Figure 4*.

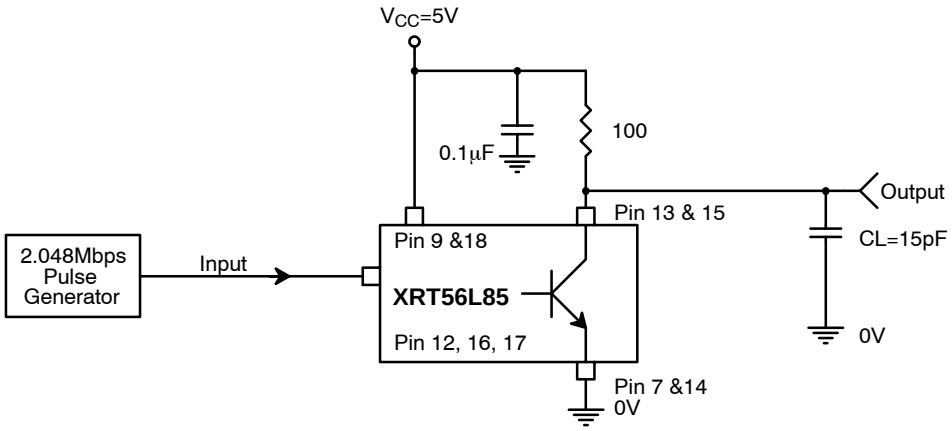



**Figure 2.**

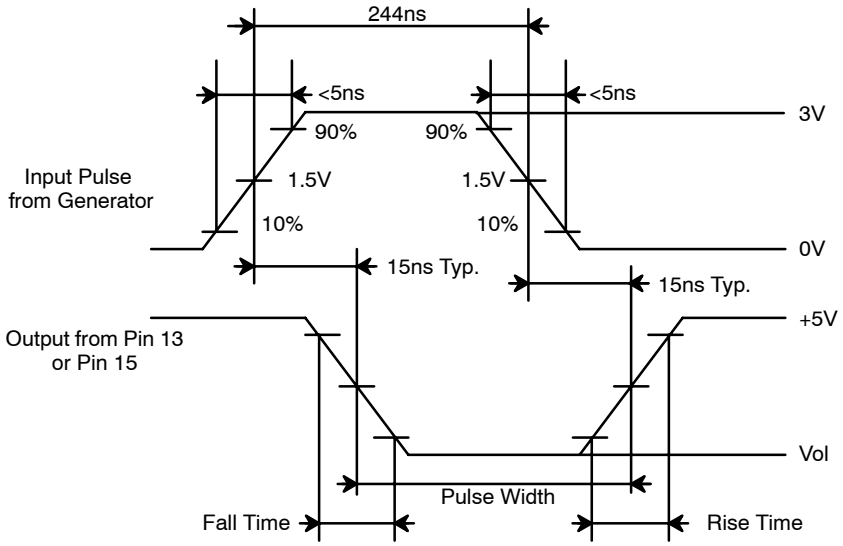



**Figure 3.**

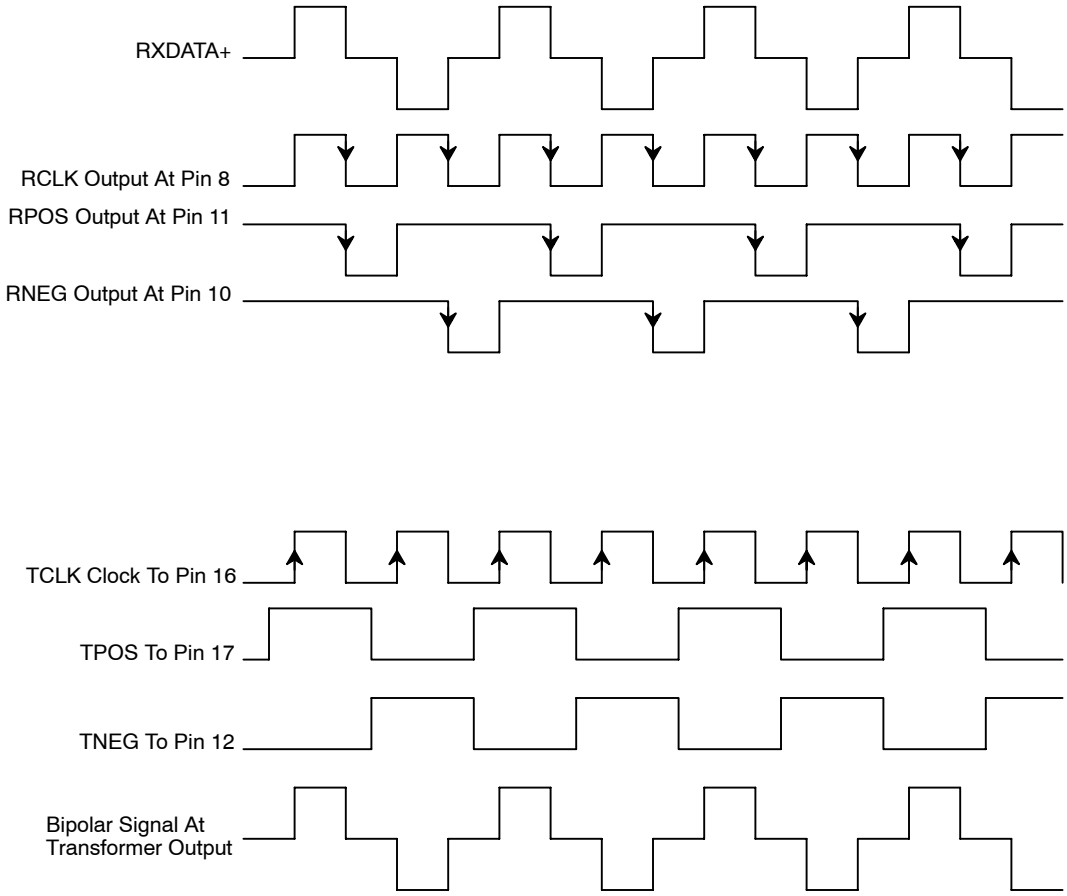
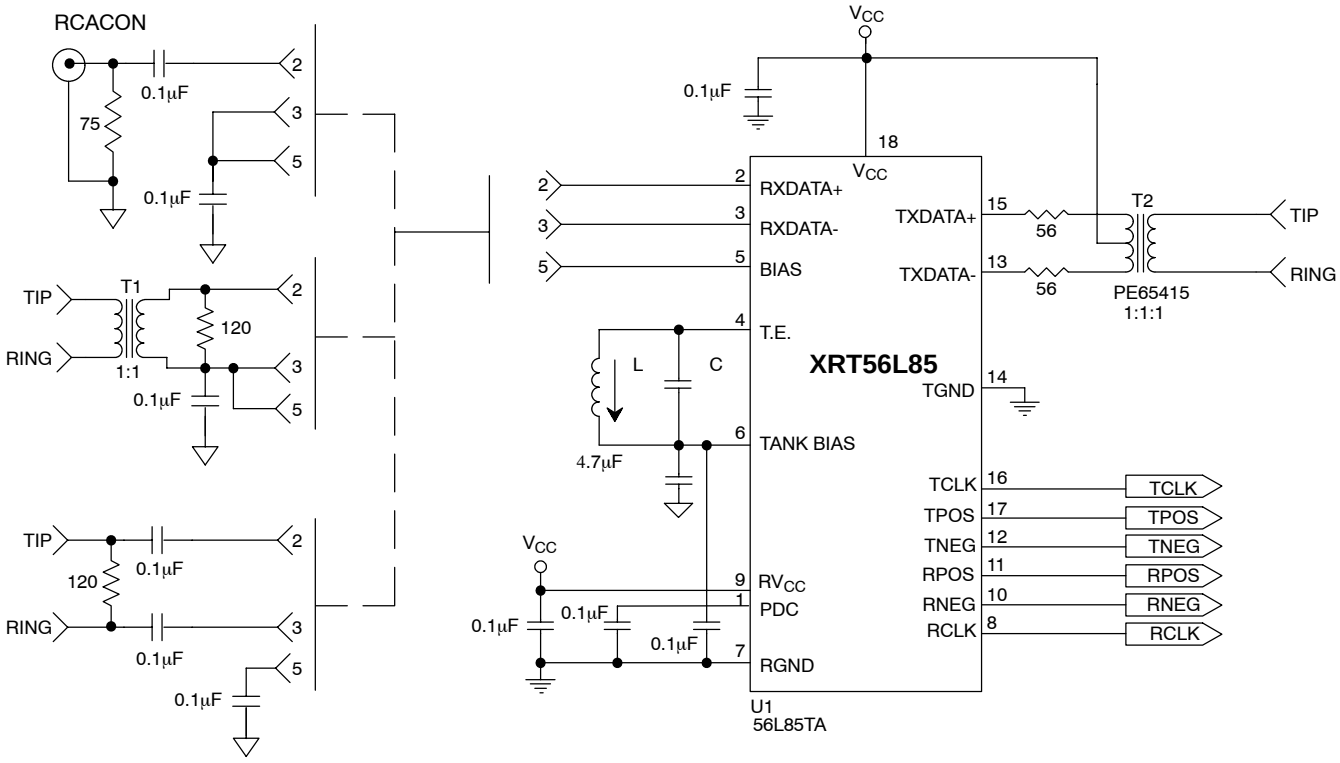



**Figure 4. Receiver Timing Diagram With 1-1-1-1-1-1 Pattern**



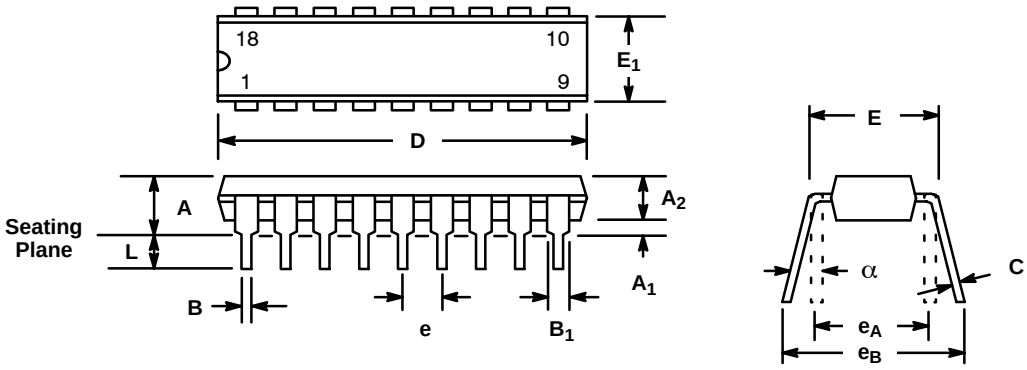

L=Tank Coil AIE 415−0804 (1.544 and 2.048 Mbs)

| Device | 1.544Mbs | 2.048Mbs |
|---|---|---|
| L | 60µH | 60µH |
| C | 175pF | 100pF |

**Figure 5. Application Circuit for XRT56L85**

# 18 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

*Rev. 1.00*

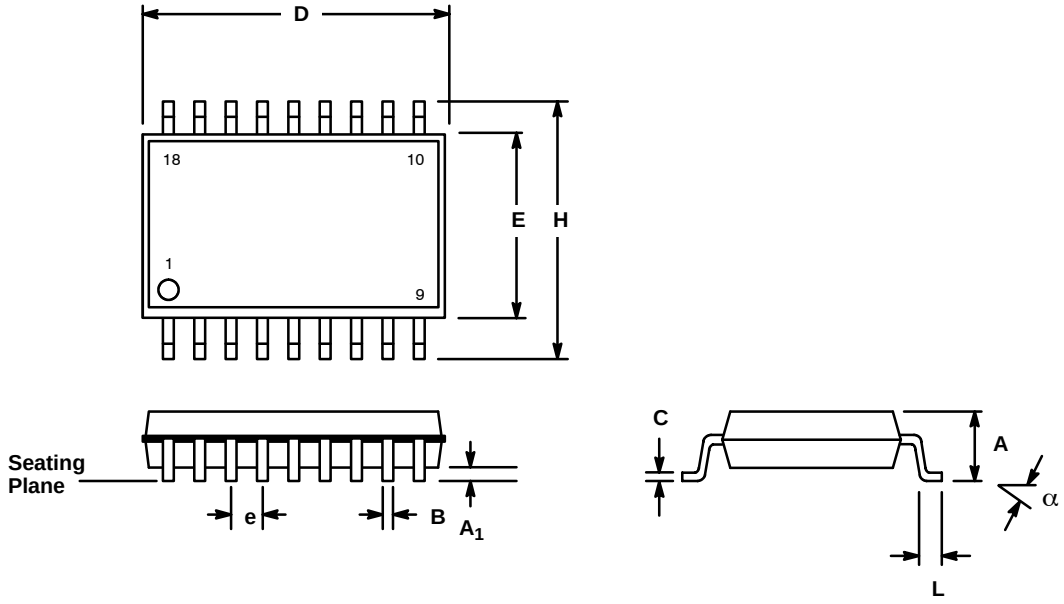



| SYMBOL | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.145 | 0.210 | 3.68 | 5.33 |
| $A_1$ | 0.015 | 0.070 | 0.38 | 1.78 |
| A2 | 0.115 | 0.195 | 2.92 | 4.95 |
| B | 0.014 | 0.024 | 0.36 | 0.56 |
| $B_1$ | 0.030 | 0.070 | 0.76 | 1.78 |
| C | 0.008 | 0.014 | 0.20 | 0.38 |
| D | 0.845 | 0.925 | 21.46 | 23.50 |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| $E_1$ | 0.240 | 0.280 | 6.10 | 7.11 |
| e | 0.100 BSC | | 2.54 BSC | |
| $e_A$ | 0.300 BSC | | 7.62 BSC | |
| $e_B$ | 0.310 | 0.430 | 7.87 | 10.92 |
| L | 0.115 | 0.160 | 2.92 | 4.06 |
| α | 0° | 15° | 0° | 15° |

*Note: The control dimension is the inch column*

# 18 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC)

*Rev. 1.00*




| SYMBOL | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.093 | 0.104 | 2.35 | 2.65 |
| $A_1$ | 0.004 | 0.012 | 0.10 | 0.30 |
| B | 0.013 | 0.020 | 0.33 | 0.51 |
| C | 0.009 | 0.013 | 0.23 | 0.32 |
| D | 0.447 | 0.463 | 11.35 | 11.75 |
| E | 0.291 | 0.299 | 7.40 | 7.60 |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.394 | 0.419 | 10.00 | 10.65 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |
| α | 0° | 8° | 0° | 8° |

*Note: The control dimension is the millimeter column*

# Notes

# Notes

NOTICE

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