

### Features

- 2 Regulated Voltage are provided
  - SYNC Switching Power Internal Reference Voltage (1.25V , 1.5V , 1.8V and 2.05V)
  - ASYNC Switching Power Internal Reference Voltage (1.5V)
- Simple Single-Loop Control Design
  - Voltage-Mode PWM Control
- Excellent Output Voltage Regulation
  - SYNC Output :  $\pm 1\%$  Over Temperature
  - ASYNC Output :  $\pm 3\%$  Over Temperature
- Fast Transient Response
  - High-Bandwidth Error Amplifier
  - Full 0% to 100% Duty Ratio
- Power-Good Output Voltage Monitor
- Over-Voltage and Over-Current Fault Monitors
- Small Converter Size
  - Constant Frequency Operation(200kHz)
  - Programmable Oscillator from 50kHz to 800kHz
  - Reduce External Component Count
- 20Pin , SOIC Package

### Applications

- High Power 5V to 2.5 or 3.3V DC-DC Regulator
- VGA Card Power Regulation

### General Description

The APW7036 provides complete power control and protection for two DC-DC converter optimized in VGA Card applications. It integrates two PWM controllers , as well as the monitoring and protection function into a single package.

The APW7036 provides simple , single feedback loop , voltage mode control with fast transient response. The output voltage of the SYNC converter can be precisely regulated to as low as  $V_{REF}$  (1.25V , 1.5V , 1.8V and 2.05V) , with a maximum tolerance of  $\pm 1.0\%$  over temperature.

The APW7036 can provides in excess of 14A of output current for an on-board DC/DC converter. It can monitors all the output voltage , and a single Power Good signal is issued when the SYNC output is within  $\pm 10\%$  of the  $V_{REF}$  setting and the ASYNC output levels is above under-voltage levels. Additional built-in over-voltage protection for the SYNC output uses the lower MOSFET to prevent output voltage above 115% of the  $V_{REF}$  setting. The PWM controller's over-current function monitor the output current by sensing the voltage drop across the upper MOSFET's  $R_{DS(ON)}$  , eliminating the need for a current sensing resistor .

### Pin Description

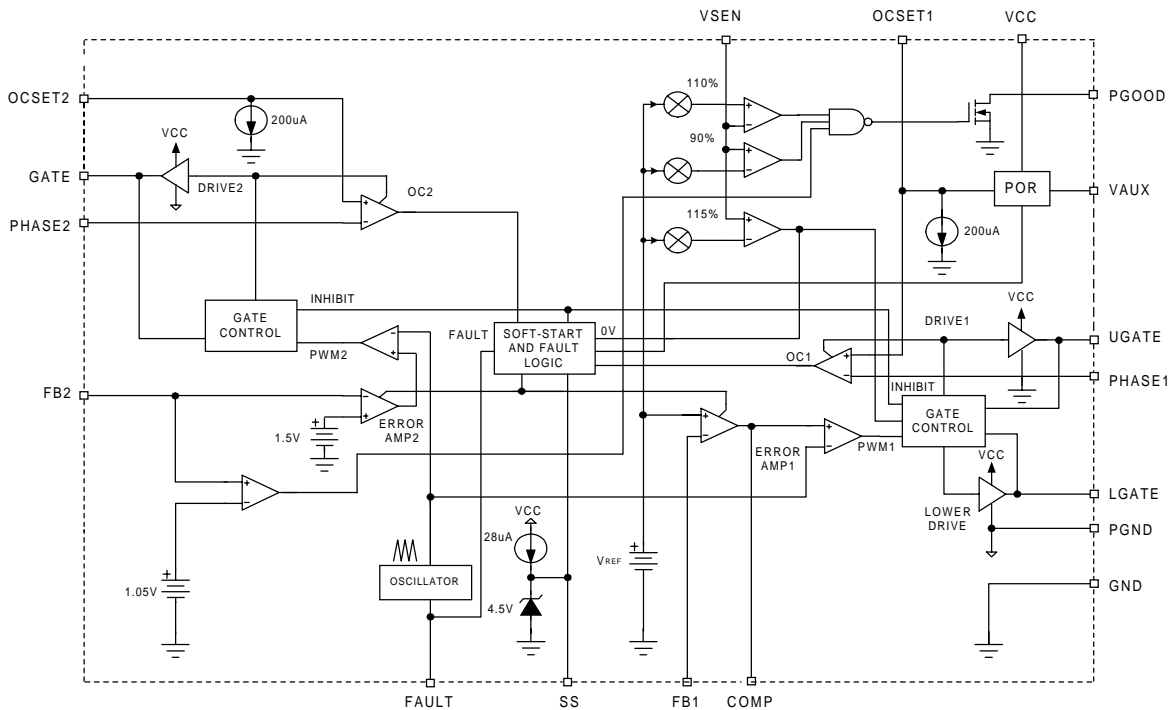
UGATE	□ 1	20 □	PHASE1
VCC	□ 2	19 □	LGATE
GATE	□ 3	18 □	PGND
PHASE2	□ 4	17 □	OCSET1
PGOOD	□ 5	16 □	VSEN
OCSET2	□ 6	15 □	FB1
FB2	□ 7	14 □	COMP
SS	□ 8	13 □	NC
FAULT/RT	□ 9	12 □	GND
NC	□ 10	11 □	VAUX

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

## Ordering Information

APW7036		Voltage Code	12 : 1.25V	15 : 1.50V	18 : 1.80V
		Package Code	K : SOP-20		
		Temp. Range	C : 0 to 70 °C		
		Handling Code	TU : Tube	TR : Tape & Reel	
		Lead Free Code	L : Lead Free Device	Blank : Original Device	

## Block Diagram



## Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VCC	Supply Voltage	15	V
V <sub>I</sub> , V <sub>O</sub>	Input , Output or I/O Voltage	GND -0.3 V to V12 +0.3	V
T <sub>A</sub>	Operating Ambient Temperature Range	0 to 70	°C
T <sub>J</sub>	Junction Temperature Range	0 to 125	°C
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
T <sub>S</sub>	Soldering Temperature	300 ,10 seconds	°C

## Thermal Characteristics

Symbol	Parameter	Value	Unit
R <sub>θJA</sub>	Thermal Resistance in Free Air		
	SOIC	75	°C/W
SOIC (with 3in <sup>2</sup> of Copper)	65		

## Electrical Characteristics

(Recommended operating conditions , Unless otherwise noted) Refer to Block and Simplified Power System Diagrams , and Typical Application Schematic

Symbol	Parameter	Test Conditions	APW7036			Unit
			Min.	Typ.	Max.	
<b>V<sub>CC</sub> Supply Current</b>						
I <sub>CC</sub>	Nominal Supply Current	UGATE , LGATE , GATE , open		9		mA
<b>Power-on Reset</b>						
	Rising VCC Threshold	Vocset=4.5V			10.4	V
	Falling VCC Threshold	Vocset=4.5V	8.2			V
	Rising VAUX Threshold	Vocset=4.5V		2.5		V
	VAUX Threshold Hysteresis	Vocset=4.5V		0.5		V
	Rising V <sub>OCSET</sub> Threshold			1.26		V
<b>Oscillator</b>						
F <sub>OCS</sub>	Free Running Frequency	RT= Open	185	200	215	kHz
ΔV <sub>OSC</sub>	Ramp Amplitude	RT= Open		1.9		V <sub>P-P</sub>
<b>Switching Controller Reference Voltage</b>						
V <sub>REF</sub>	Reference Voltage	APW7036-12 APW7036-15 APW7036-18 APW7036-20		1.25 1.50 1.80 2.05		V
	Reference Voltage accuracy		-1.0		+1.0	%
V <sub>FB2</sub>	Reference Voltage			1.5		V
	Reference Voltage accuracy		-3.0		+3.0	%
<b>Synchronous PWM Controller Error Amplifier</b>						
	DC Gain			88		dB
GBWP	Gain-Bandwidth Product			15		MHz
SR	Slew Rate	COMP=10pF		6		V/μs
<b>PWM Controllers Gate Drivers</b>						
I <sub>UGATE</sub>	UGATE1,GATE Source	V <sub>CC</sub> =12V, V <sub>UGATE1,GATE</sub> =6V		1		A
R <sub>UGATE</sub>	UGATE1,GATE Sink	V <sub>UGATE1,GATE</sub> =1V			3.5	Ω

## Electrical Characteristics Cont.

Symbol	Parameter	Test Conditions	APW7036			Unit
			Min.	Typ.	Max.	
<b>PWM Controllers Gate Drivers</b>						
$I_{LGATE}$	LGATE Source	$V_{CC}=12V, V_{LGATE}=1V$		1		A
$R_{LGATE}$	LGATE Sink	$V_{LGATE}= 1V$			3	$\Omega$
<b>Protection</b>						
	VSEN Over-Voltage ( $V_{SEN}/V_{REF}$ )	VSEN Rising		115	120	%
$I_{OVP}$	FAULT Sourcing Current	$V_{FAULT/RT}=2.0V$		8.5		mA
$I_{OCSET}$	OCSET1,2 Current Source	$V_{OCSET}= 4.5V_{DC}$	170	200	230	$\mu A$
$I_{SS}$	Soft Start Current			28		$\mu A$
<b>Power Good</b>						
	VSEN Upper Threshold ( $V_{SEN}/V_{REF}$ )	VSEN1 Rising		110		%
	VSEN Under Voltage ( $V_{SEN}/V_{REF}$ )	VSEN1 Rising		94		%
	VSEN Hysteresis ( $V_{SEN}/V_{REF}$ )	Upper /Lower Threshold		2		%
$V_{PGOOD}$	PGOOD Voltage Low	$I_{PGOOD}= -4mA$			0.8	V

## Functional Pin Description

### UGATE (Pin 1)

Connect UGATE pin to the synchronous PWM converter's upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.

### VCC (Pin 2)

Provide a 12V bias supply for the IC to this pin. This pin also provides the gate bias charge for all the MOSFETs controlled by the IC. The voltage at this pin is monitored for Power-On Reset purposes.

### GATE (Pin 3)

Connect GATE pin to the standard BUCK PWM converter's MOSFET gate. This pin provides the gate drive for the MOSFET.

### PHASE2 (Pin 4)

Connect the PHASE2 pin to the standard BUCK PWM

converter's MOSFET source. This pin is used to monitor the voltage drop across the MOSFET for over-current protection.

### PGOOD (Pin 5)

PGOOD is an open collector output used to indicate the status of the output voltages. This pin is pulled low when the synchronous regulator output is not within 10% of the reference voltage or the other output is below under-voltage thresholds.

### NC (Pin 10, 13)

No Connection.

### OCSET1 , 2 (Pin 17 , 6)

Connect a resistor ( $R_{OCSET}$ ) from this pin to the drain of the PWM converter's MOSFET.  $R_{OCSET}$ , an internal 200 $\mu A$  current source ( $I_{OCSET}$ ), and the MOSFET's on-resistance( $r_{DS(ON)}$ ) set the converter over-current

## Functional Pin Description Cont.

(OC) trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} * R_{OCSET}}{r_{DS(ON)}}$$

An over-current trip cycles the soft-start function.

### FB2 (Pin 7)

This pin provides the feedback for the non-synchronous switching regulator. A resistor divider is connected from this pin to regulator output and GND that sets the output voltage. The value of the resistor connected from regulator output to FB2 must be less than 150Ω.

### SS (Pin 8)

Connect a capacitor from this pin to ground. This capacitor, along with an internal 28μA current source, sets the soft-start interval of the converter.

### FAULT / RT (Pin 9)

This pin provides oscillator switching frequency adjustment. By placing a resistor ( $R_T$ ) from this pin to GND, the nominal 200kHz switching frequency is increased. Conversely, connecting a pull-up resistor ( $R_T$ ) from this pin to VCC reduces the switching frequency.

Nominally, the voltage at this pin is 1.26V. In the event of an over-voltage or over-current condition, this pin is internally pulled to VCC.

### VAUX (Pin 11)

The +3.3V input voltage at this pin is monitored for power-on reset (POR) purposes.

### GND (Pin 12)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

### COMP and FB1 (Pins 14, and 15)

COMP and FB1 are the available external pins of the

synchronous PWM regulator error amplifier. The FB1 pin is the inverting input of the error amplifier. Similarly, the COMP pin is the error amplifier output. These pins are used to compensate the voltage-mode control feedback loop of the synchronous PWM converter.

### VSEN (Pin 16)

This pin is connected to the synchronous PWM converter's output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for over-voltage protection.

### PGND (Pin 18)

This is the power ground connection. Tie the synchronous PWM converter's lower MOSFET source to this pin.

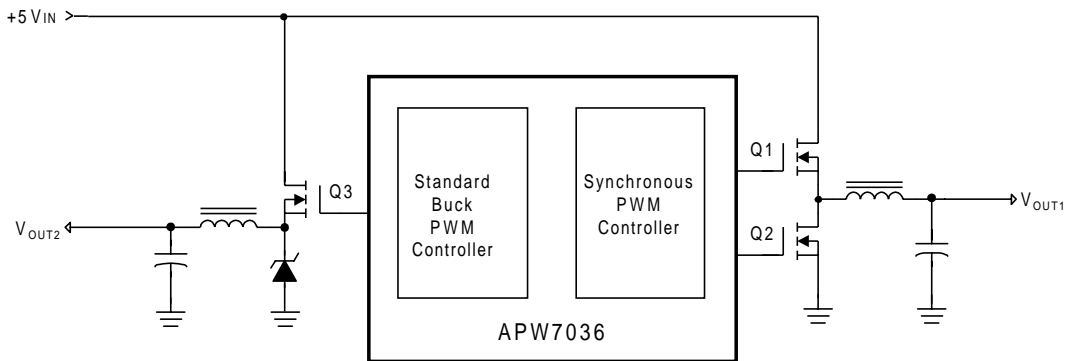
### LGATE (Pin 19)

Connect LGATE to the synchronous PWM converter's lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.

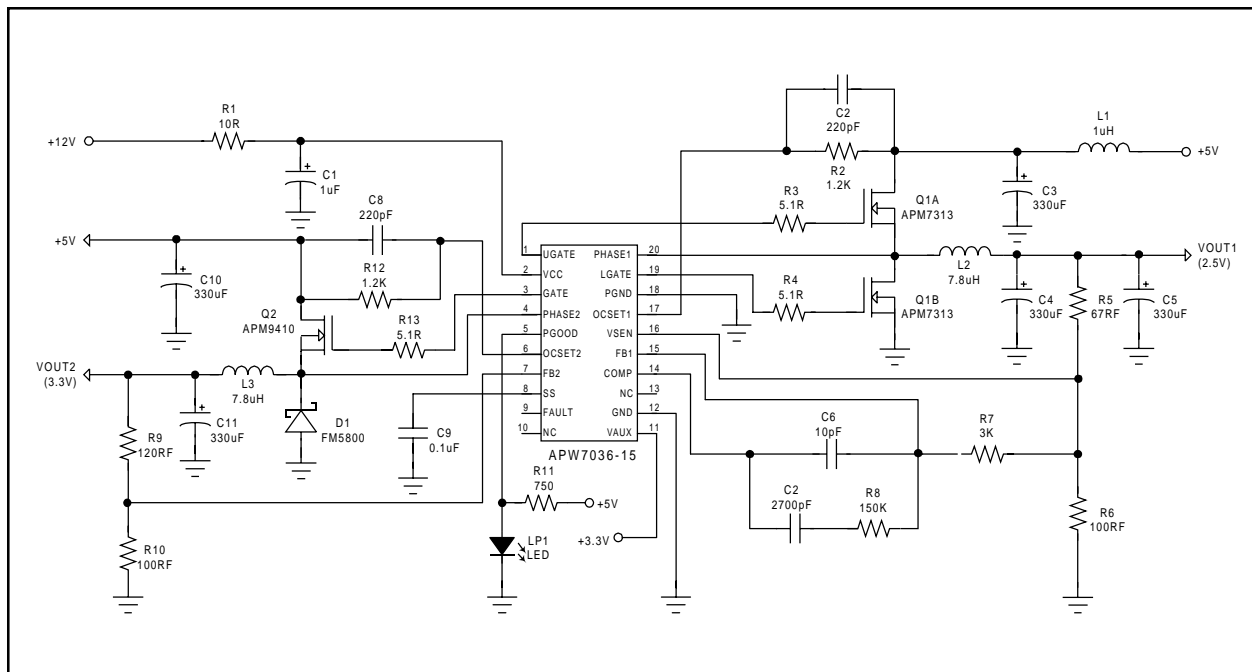
### PHASE1 (Pin 20)

Connect the PHASE1 pin to the synchronous PWM converter's upper MOSFET source. This pin is used to monitor the voltage drop across the upper MOSFET for over-current protection.

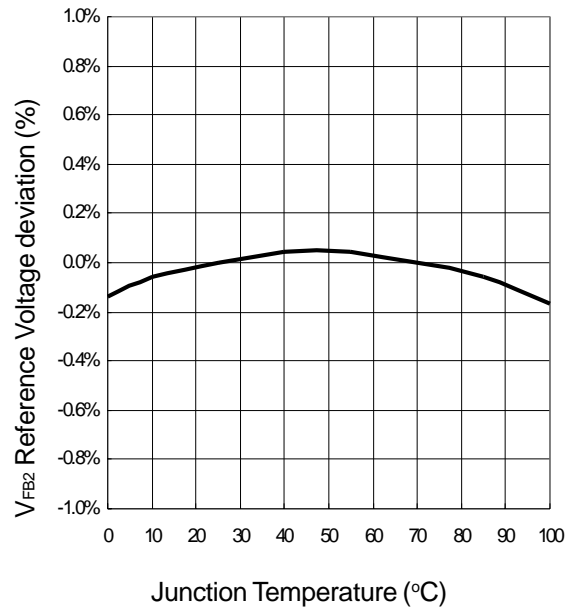
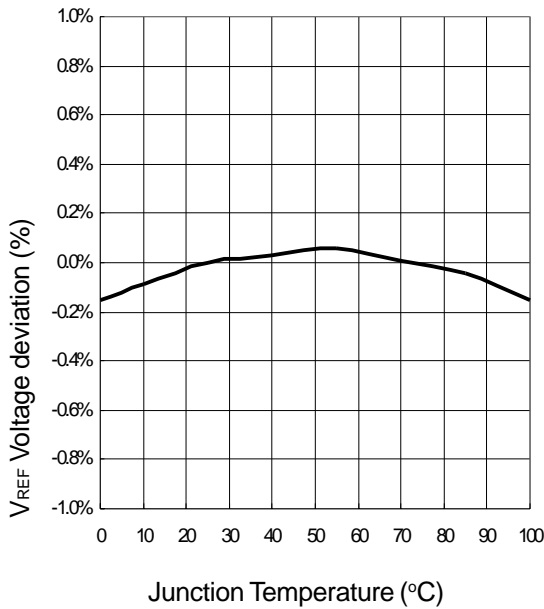
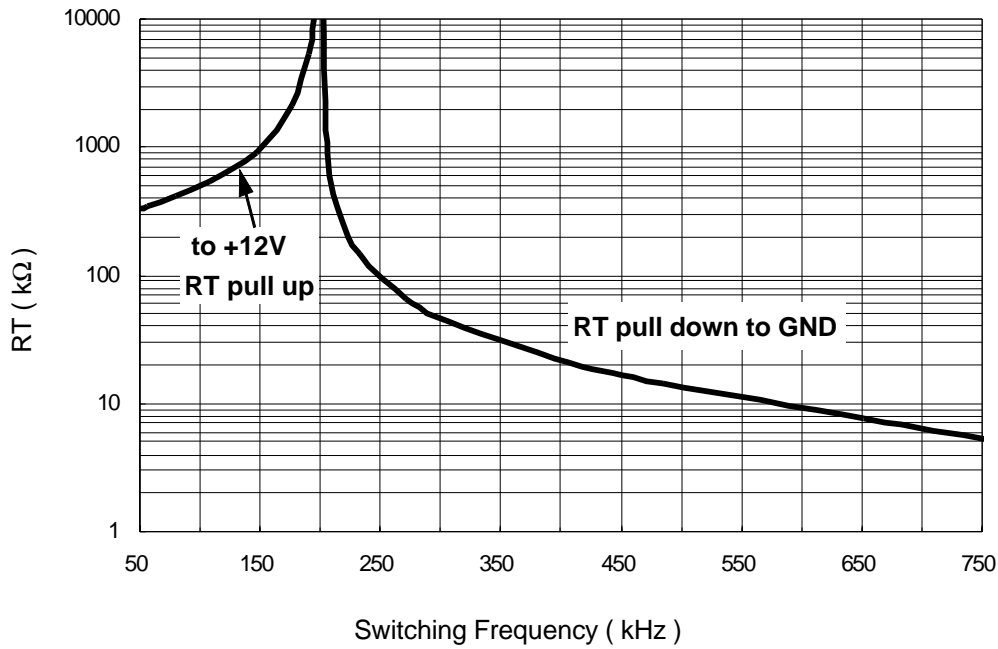
## Simplified Power System Diagram



## Typical Characteristics



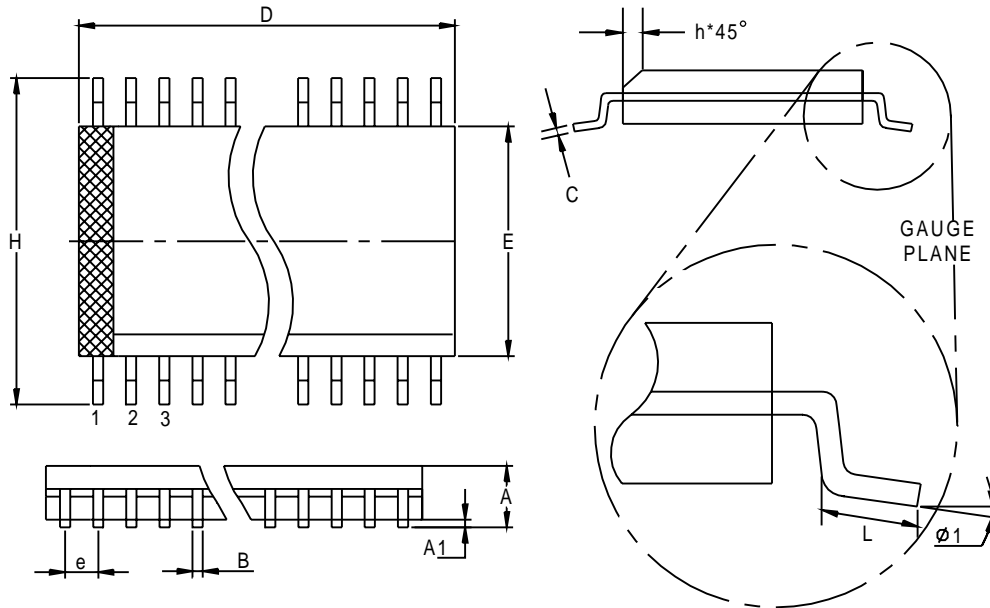
## Typical Characteristics



Note : The Reference Voltage ( $V_{REF}$ ) Deviation is  $\frac{V_{REF}(T_J) - V_{REF}(25^\circ C)}{V_{REF}(25^\circ C)} \times 100\%$

## Package Information

SO – 300mil ( Reference JEDEC Registration MS-013)



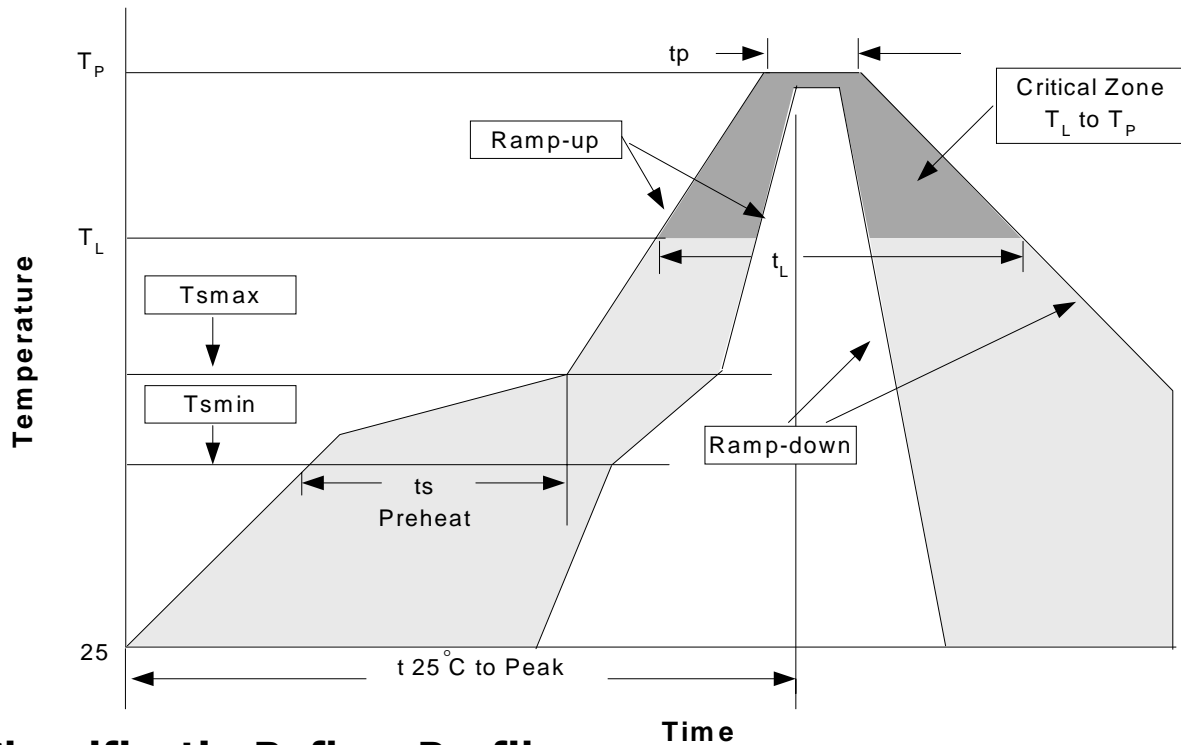
Dim	Millimeters		Variations			Dim	Inches		Variations		
	Min.	Max.	Variations	Min.	Max.		Min.	Max.	Variations	Min.	Max.
A	2.35	2.65	SO-20	12.60	13.0	A	0.093	0.1043	SO-20	0.496	0.512
A1	0.10	0.30	SO-24	15.20	15.60	A1	0.004	0.0120	SO-24	0.599	0.614
B	0.33	0.51	SO-28	17.70	18.11	B	0.013	0.020	SO-28	0.697	0.713
C	0.23	0.32				C	0.0091	0.0125			
D	See variations					D	See variations				
E	7.40	7.60				E	0.2914	0.2992			
e	1.27BSC					e	0.050BSC				
H	10	10.65				H	0.394	0.419			
h	0.25	0.75				h	0.010	0.029			
L	0.40	1.27				L	0.016	0.050			
φ 1	0°	8°				φ 1	0°	8°			



## Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb)
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.
Packaging	1000 devices per reel

### Reflow Condition (IR/Convection or VPR Reflow)



### Classification Reflow Profiles

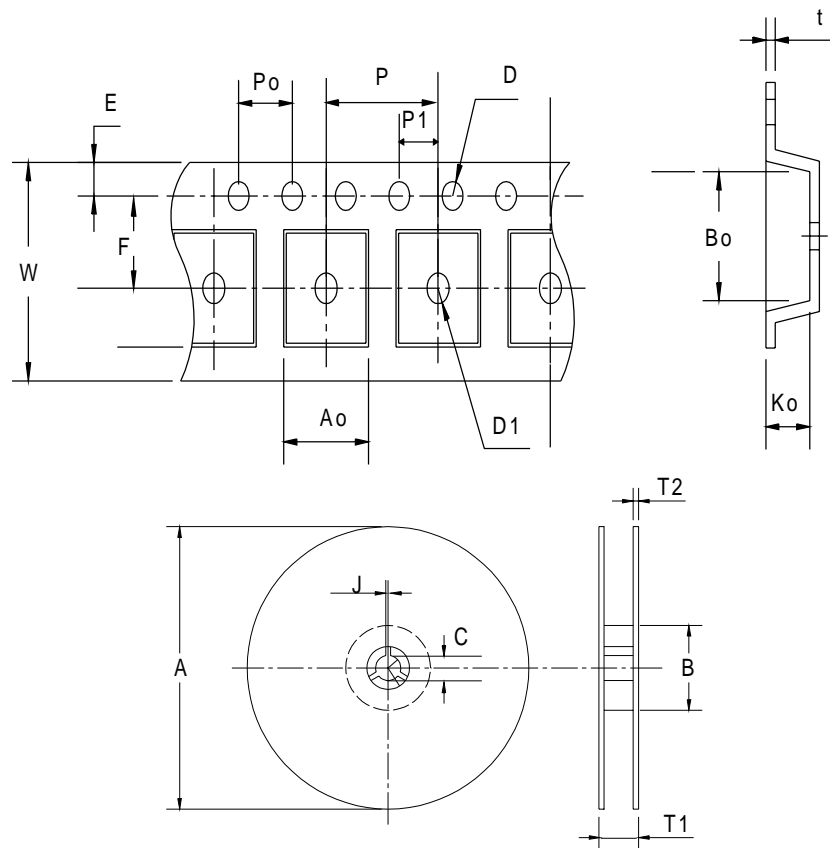
Profile Feature	Sn-Pb Eutectic Assembly		Pb-Free Assembly	
	Large Body	Small Body	Large Body	Small Body
Average ramp-up rate ( $T_L$ to $T_P$ )	3°C/second max.		3°C/second max.	
Preheat				
- Temperature Min ( $T_{smin}$ )	100°C		150°C	
- Temperature Mix ( $T_{smax}$ )	150°C		200°C	
- Time (min to max)( $t_s$ )	60-120 seconds		60-180 seconds	
$T_{smax}$ to $T_L$				
- Ramp-up Rate			3°C/second max	
$T_{smax}$ to $T_L$				
- Temperature( $T_L$ )	183°C		217°C	
- Time ( $t_L$ )	60-150 seconds		60-150 seconds	
Peak Temperature( $T_p$ )	225 +0/-5°C	240 +0/-5°C	245 +0/-5°C	250 +0/-5°C
Time within 5°C of actual Peak Temperature( $t_p$ )	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.		6°C/second max.	
Time 25°C to Peak Temperature	6 minutes max.		8 minutes max.	

Note: All temperatures refer to topside of the package. Measured on the body surface.

## Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I <sub>tr</sub> > 100mA

## Tape & Reel Dimensions



<b>Application</b>	A	B	C	J	T1	T2	W	P	E
<b>SOP-20</b>	330±1	62 ± 1.5	12.75 ±0.15	2 + 0.6	24.4 +0.2	2± 0.2	24 + 0.3 - 0.1	12± 0.1	1.75± 0.1
<b>Application</b>	F	D	D1	Po	P1	Ao	Bo	Ko	t
<b>SOP-20</b>	11.5 ± 0.1	1.5+0.1	1.5+0.25	4.0 ± 0.1	2.0 ± 0.1	8.2 ± 0.1	13± 0.1	2.5± 0.1	0.35±0.013

(mm)

**Cover Tape Dimensions**

<b>Application</b>	<b>Carrier Width</b>	<b>Cover Tape Width</b>	<b>Devices Per Reel</b>
<b>SOP- 20</b>	24	21.3	1000

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