



**CMLDM7003  
CMLDM7003J**

**SURFACE MOUNT PICOmini™  
DUAL N-CHANNEL  
ENHANCEMENT-MODE  
SILICON MOSFET**

**PICOmini™**



**SOT-563 CASE**

**Central™  
Semiconductor Corp.**

**DESCRIPTION:**

The CENTRAL SEMICONDUCTOR CMLDM7003 and CMLDM7003J are Enhancement-mode N-Channel Field Effect Transistors, manufactured by the N-Channel DMOS Process, designed for high speed pulsed amplifier and driver applications. The CMLDM7003 utilizes the USA pinout configuration, while the CMLDM7003J utilizes the Japanese pinout configuration. These special Dual Transistor devices offer low drain-source on state resistance ( $r_{DS(ON)}$ ).

**MARKING CODE: CMLDM7003: C30  
CMLDM7003J: C3J**

**MAXIMUM RATINGS** ( $T_A=25^\circ\text{C}$ )

	SYMBOL		UNITS
Drain-Source Voltage	$V_{DS}$	50	V
Drain-Gate Voltage	$V_{DG}$	50	V
Gate-Source Voltage	$V_{GS}$	40	V
Continuous Drain Current	$I_D$	300	mA
Maximum Pulsed Drain Current	$I_{DM}$	1.2	A
Power Dissipation	$P_D$	350	mW (Note 1)
Power Dissipation	$P_D$	300	mW (Note 2)
Power Dissipation	$P_D$	150	mW (Note 3)
Operating and Storage			
Junction Temperature	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$
Thermal Resistance	$\theta_{JA}$	357	$^\circ\text{C/W}$

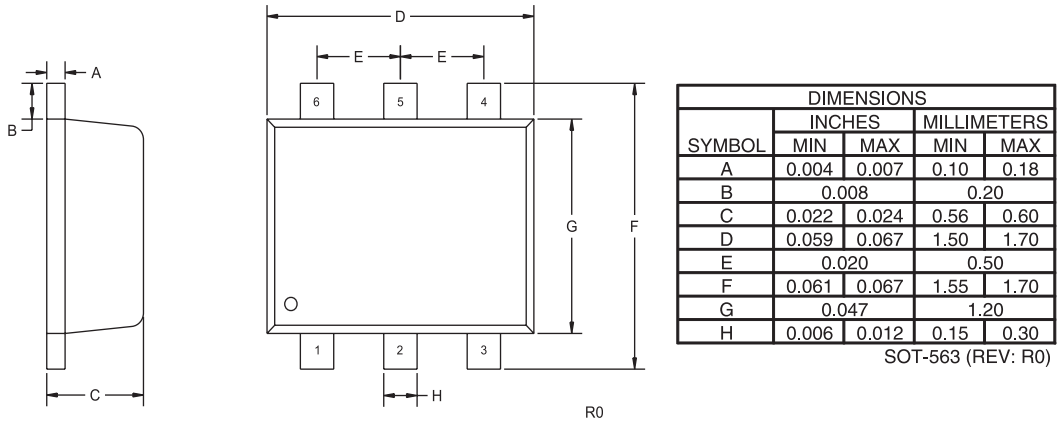
**ELECTRICAL CHARACTERISTICS PER TRANSISTOR** ( $T_A=25^\circ\text{C}$  unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{GSSF}, I_{GSSR}$	$V_{GS}=5V$			50	nA
$I_{GSSF}, I_{GSSR}$	$V_{GS}=10V$			500	nA
$I_{GSSF}, I_{GSSR}$	$V_{GS}=12V$			1.0	$\mu\text{A}$
$I_{DSS}$	$V_{DS}=50V, V_{GS}=0V$			50	nA
$BV_{DSS}$	$V_{GS}=0V, I_D=10\mu\text{A}$	50			V
$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.5		1.2	V
$r_{DS(ON)}$	$V_{GS}=1.8V, I_D=50\text{mA}$		1.6	2.3	$\Omega$
$r_{DS(ON)}$	$V_{GS}=2.5V, I_D=50\text{mA}$		1.3	1.9	$\Omega$
$r_{DS(ON)}$	$V_{GS}=5.0V, I_D=50\text{mA}$		1.1	1.5	$\Omega$
gFS	$V_{DS}=10V, I_D=200\text{mA}$	200			mmhos
$C_{rss}$	$V_{DS}=25V, V_{GS}=0, f=1.0\text{MHz}$			TBD	pF
$C_{iss}$	$V_{DS}=25V, V_{GS}=0, f=1.0\text{MHz}$			TBD	pF
$C_{oss}$	$V_{DS}=25V, V_{GS}=0, f=1.0\text{MHz}$			TBD	pF
$V_{SD}$	$V_{GS}=0V, I_S=115\text{mA}$			1.4	V

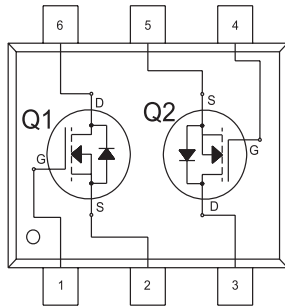
- Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0 mm<sup>2</sup>  
 (2) FR-4 Epoxy PC Board with copper mounting pad area of 4.0 mm<sup>2</sup>  
 (3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4 mm<sup>2</sup>

R0 (26-June 2006)

**SOT-563 CASE - MECHANICAL OUTLINE**



**CMLDM7003 (USA Pinout)**

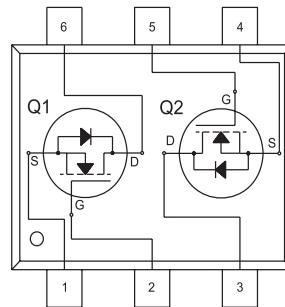


**LEAD CODE:**

- 1) GATE Q1
- 2) SOURCE Q1
- 3) DRAIN Q2
- 4) GATE Q2
- 5) SOURCE Q2
- 6) DRAIN Q1

**MARKING CODE: C30**

**CMLDM7003J (Japanese Pinout)**



**LEAD CODE:**

- 1) SOURCE Q1
- 2) GATE Q1
- 3) DRAIN Q2
- 4) SOURCE Q2
- 5) GATE Q2
- 6) DRAIN Q1

**MARKING CODE: C3J**