PROCESS CP192

Small Signal Transistor

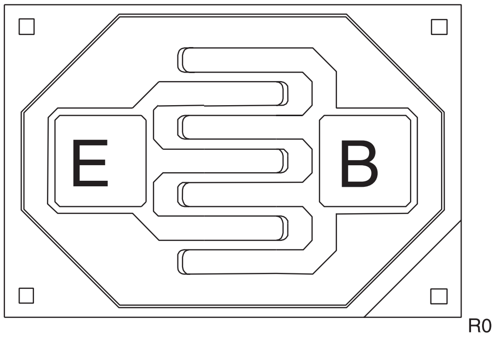
NPN - Amp/Switch Transistor Chip

Central™
Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	13 x 17 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	3.0 X 3.0 MILS
Emitter Bonding Pad Area	3.0 X 3.0 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



BACKSIDE COLLECTOR

GROSS DIE PER 4 INCH WAFER

52,240

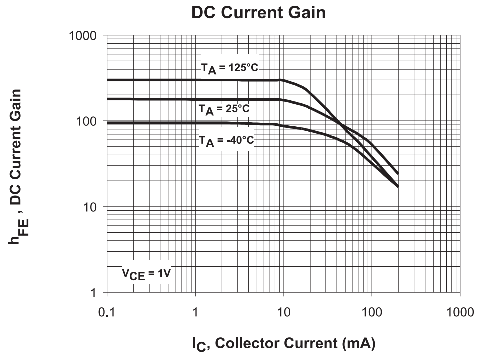
PRINCIPAL DEVICE TYPES

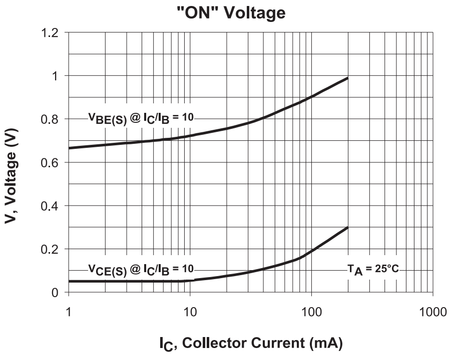
2N3904
CMPT3904
CMST3904
CXT3904
CZT3904

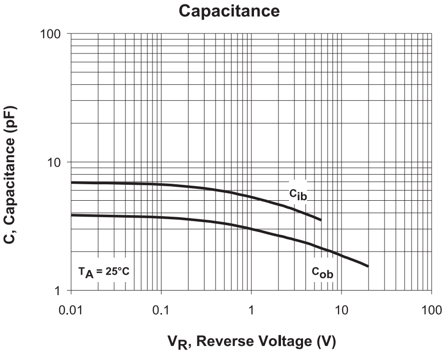
145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

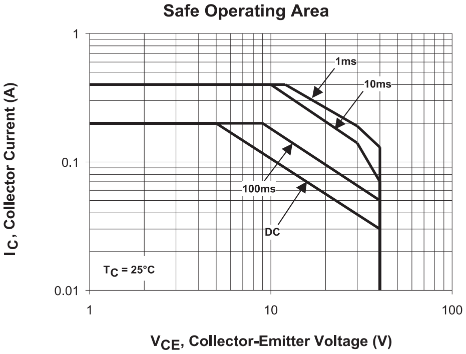
R2 (1 -August 2002)

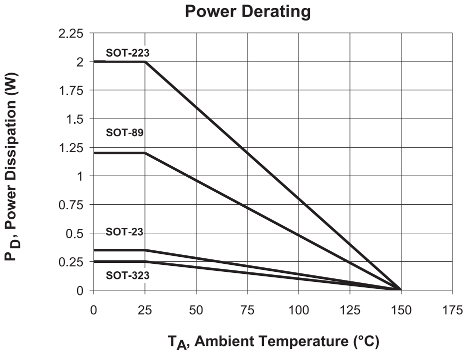
Typical Electrical Characteristics

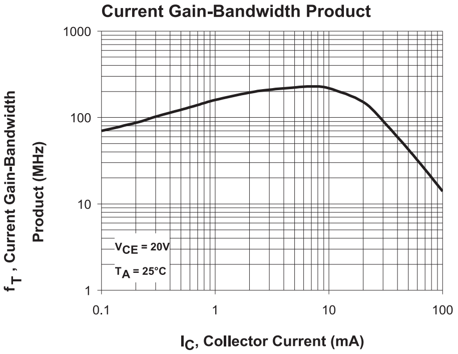

DC Current Gain


"ON" Voltage


Capacitance


Safe Operating Area


Power Derating


Current Gain-Bandwidth Product

145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

R2 (1 -August 2002)