32Mbyte(8Mx32) 72-pin F/P Mode 2K Ref. SIMM Design 5V

Part No. HMD8M32M16, HMD8M32M16G

GENERAL DESCRIPTION

The HMD8M32M16 is a 8M x 32 bit dynamic RAM high density memory module. The module consists of sixteen CMOS 4M x 4bit DRAMs in 24-pin SOJ packages mounted on a 72-pin, double-sided, FR-4-printed circuit board. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM components. The module is a single In-line Memory Module with edge connections and is intended for mounting in to 72-pin edge connector sockets. All module components may be powered from a single 5V DC power supply and all inputs and outputs are TTL-compatible.

FEATURES

- Part Identification
  - HMD8M32M16--2048 Cycles/32ms Ref, Solder
  - HMD8M32M16G--2048 Cycles/32ms Ref, Gold
- Access times : 50, 60ns
- High-density 32MByte design
- Single + 5V ±0.5V power supply
- JEDEC standard pinout
- FP(Fast Page) mode operation
- TTL compatible inputs and outputs
- FR4-PCB design

OPTIONS MARKING

- Timing
  - 50ns access -5
  - 60ns access -6
- Packages
  - 72-pin SIMM M

PERFORMANCE RANGE

SPEED	tRAC	tCAC	tRC	tPC
-5	50ns	13ns	90ns	35ns
-6	60ns	15ns	110ns	40ns

PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	19	A10	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	Vss	57	DQ12
4	DQ1	22	DQ5	40	/CAS0	58	DQ28
5	DQ17	23	DQ21	41	/CAS2	59	Vcc
6	DQ2	24	DQ6	42	/CAS3	60	DQ29
7	DQ18	25	DQ22	43	/CAS1	61	DQ13
8	DQ3	26	DQ7	44	/RAS0	62	DQ30
9	DQ19	27	DQ23	45	/RAS1	63	DQ14
10	Vcc	28	A7	46	NC	64	DQ31
11	NC	29	NC(A11)	47	/W	65	DQ15
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	/RAS1	51	DQ9	69	PD3
16	A4	34	/RAS0	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	Vss

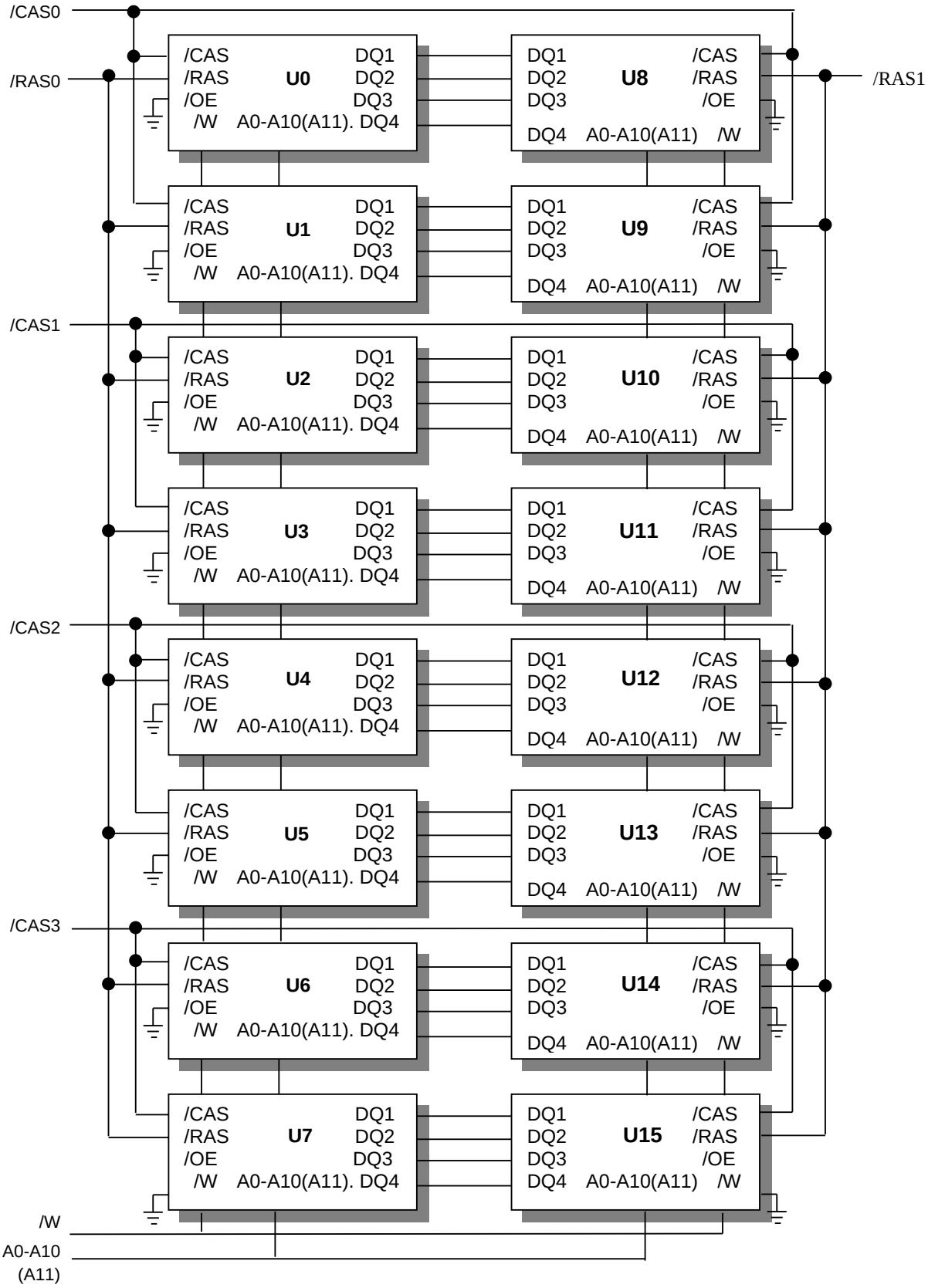
SIMM TOP VIEW

Note: A11 is not used for HMD8M32M16

PIN NAMES

Pin Name	Function	Pin Name	Function	Pin Name	Function
A0-A10	Address Input(2K Ref)	/RAS0, /RAS1	Row Address Strobe	Vss	Ground
A0-A11	Address Input(4K Ref)	/CAS0 - /CAS3	Column Address Strobe	NC	No Connection
DQ0-DQ31	Data In/Out	PD1 - PD4	Presence Detect	Vcc	Power(+5V)
/W	Read/Write Input				

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	-1V to 7.0V
Voltage on Vcc Supply Relative to Vss	Vcc	-1V to 7.0V
Power Dissipation	P_D	16W
Storage Temperature	T_{STG}	-55°C to 150°C
Short Circuit Output Current	I_{OS}	50mA

w Permanent device damage may occur if " Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(Voltage reference to V_{SS}, T_A=0 to 70 °C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	Vcc+1	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS

SYMBOL	SPEED	MIN	MAX	UNITS
I_{CC1}	-5	-	1760	mA
	-6	-	1600	mA
I_{CC2}		-	32	mA
I_{CC3}	-5	-	1760	mA
	-6	-	1600	mA
I_{CC4}	-5	-	1440	mA
	-6	-	1280	mA
I_{CC5}		-	16	mA
I_{CC6}	-5	-	1760	mA
	-6	-	1600	mA
$I_{I(L)}$		-80	80	µA
$I_{O(L)}$		-80	80	µA
V_{OH}		2.4	-	V
V_{OL}		-	0.4	V

I_{CC1} : Operating Current * (/RAS , /CAS , Address cycling @t_{RC}=min.)

I_{CC2} : Standby Current (/RAS=/CAS=V_{IH})

I_{CC3} : /RAS Only Refresh Current * (/CAS=V_{IH}, /RAS, Address cycling @t_{RC}=min)

I_{CC4} : Fast Page Mode Current * (/RAS=V_{IL}, /CAS, Address cycling @t_{PC}=min)

I_{CC5} : Standby Current (/RAS=/CAS=Vcc-0.2V)

I_{CC6} : /CAS-Before-/RAS Refresh Current * (/RAS and /CAS cycling @t_{RC}=min)

I_{IL} : Input Leakage Current (Any input 0V ≤ V_{IN} ≤ 6.5V, all other pins not under test = 0V)

I_{OL} : Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V

V_{OH} : Output High Voltage Level (I_{OH}= -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address cad be changed maximum once while /RAS=V_{IL}. In I_{CC4}, address can be changed maximum once within one page mode cycle.

CAPACITANCE (T_A=25°C, Vcc = 5V, f = 1Mz)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Input Capacitance (A0-A10)	C_{IN1}	-	80	pF
Input Capacitance (/W)	C_{IN2}	-	112	pF
Input Capacitance (/RAS0)	C_{IN3}	-	112	pF
Input Capacitance (/CAS0-/CAS3)	C_{IN4}	-	112	pF
Input/Output Capacitance (DQ0-31)	C_{DQ1}	-	112	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C , Vcc = 5V±10%, See notes 1,2.)

PARAMETER	SYMBOL	-5		-6		UNIT
		MIN	MAX	MIN	MAX	
Random read or write cycle time	t_{RC}	90		110		ns
Access time from /RAS	t_{RAC}		50		60	ns
Access time from /CAS	t_{CAC}		13		15	ns
Access time from column address	t_{AA}		25		30	ns
/CAS to output in Low-Z	t_{CLZ}	3		3		ns
Output buffer turn-off delay	t_{OFF}	3	13	3	15	ns
Transition time (rise and fall)	t_T	2	50	2	50	ns
/RAS precharge time	t_{RP}	30		30		ns
/RAS pulse width	t_{RAS}	50	10K	60	10K	ns
/RAS hold time	t_{RSH}	13		15		ns
/CAS hold time	t_{CSH}	60		70		ns
/CAS pulse width	t_{CAS}	15	10K	20	10K	ns
/RAS to /CAS delay time	t_{RCD}	20	45	20	50	ns
/RAS to column address delay time	t_{RAD}	15	30	15	35	ns
/CAS to /RAS precharge time	t_{CRP}	5		5		ns

Row address set-up time	t_{ASR}	0		0		ns
Row address hold time	t_{RAH}	10		10		ns
Column address set-up time	t_{ASC}	0		0		ns
Column address hold time	t_{CAH}	15		15		ns
Column address hold referenced to /RAS	t_{AR}	50		55		ns
Column Address to /RAS lead time	t_{RAL}	30		35		ns
Read command set-up time	t_{RCS}	0		0		ns
Read command hold referenced to /CAS	t_{RCH}	0		0		ns
Read command hold referenced to /RAS	t_{RRH}	0		0		ns
Write command hold time	t_{WCH}	15		15		ns
Write command hold referenced to /RAS	t_{WCR}	50		55		ns
Write command pulse width	t_{WP}	15		15		ns
Write command to /RAS lead time	t_{RWL}	15		20		ns
Write command to /CAS lead time	t_{CWL}	15		20		ns
Data-in set-up time	t_{DS}	0		0		ns
Data-in hold time	t_{DH}	15		15		ns
Data-in hold referenced to /RAS	t_{DHR}	50		55		ns
Refresh period	t_{REF}		16		16	ns
Write command set-up time	t_{WCS}	0		0		ns
/CAS setup time (C-B-R refresh)	t_{CSR}	10		10		ns
/CAS hold time (C-B-R refresh)	t_{CHR}	15		15		ns
/RAS precharge to /CAS hold time	t_{RPC}	5		5		ns
Access time from /CAS precharge	t_{CPA}		35		40	ns
Fast page mode cycle time	t_{PC}	40		45		ns
/CAS precharge time (Fast page)	t_{CP}	10		10		ns
/RAS pulse width (Fast page)	t_{RASP}	60	100K	70	100K	ns
/W to /RAS precharge time (C-B-R refresh)	t_{WRP}	10		10		ns
/W to /RAS hold time (C-B-R refresh)	t_{WRH}	10		10		ns
/CAS precharge(C-B-R counter test)	t_{CPT}	20		30		ns

NOTES

1.An initial pause of 200μs is required after power-up followed by any 8 /RAS-only or /CAS-before-/RAS refresh cycles before proper device operation is achieved.

2.$V_{IH\ (min)}$ and $V_{IL\ (max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$ and are assumed to be 5ns for all inputs.

3.Measured with a load equivalent to 1TTL loads and 100pF

4.Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.

5.Assumes that $t_{RCD} \geq t_{RCD(max)}$

6. t_{AR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$

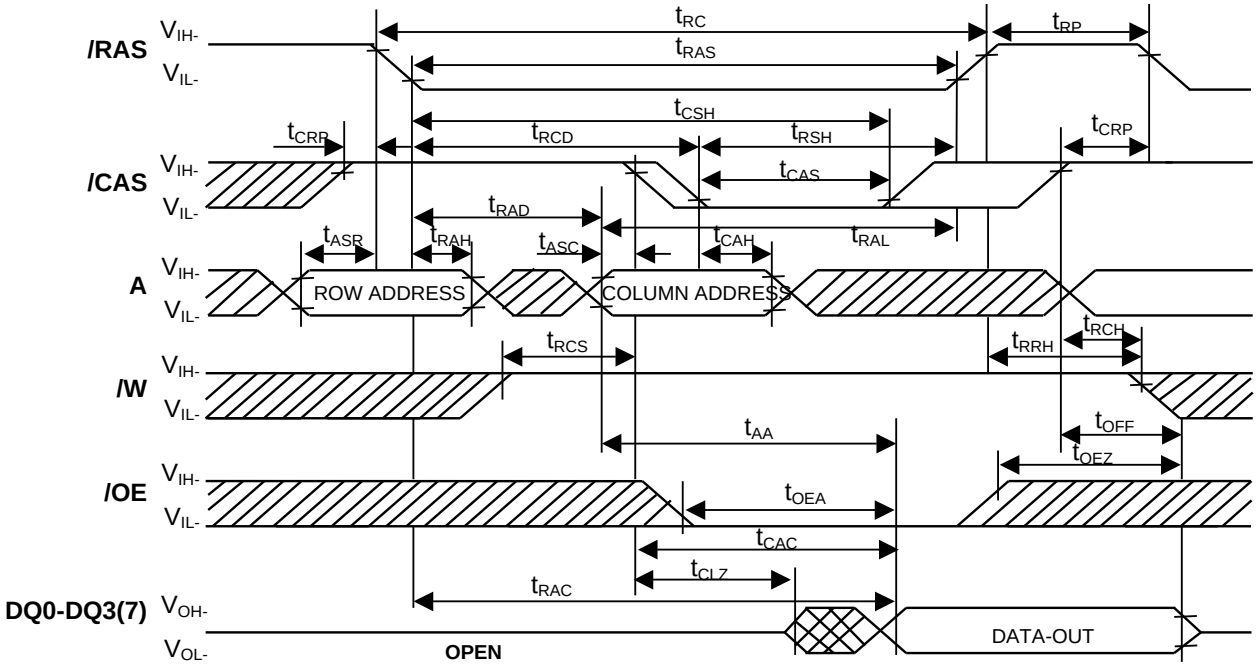
7.This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH}

or V_{OL}.

8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameter.
   They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the /CAS leading edge in early write cycles and to the /W leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit. then access time is controlled by t_{AA}.

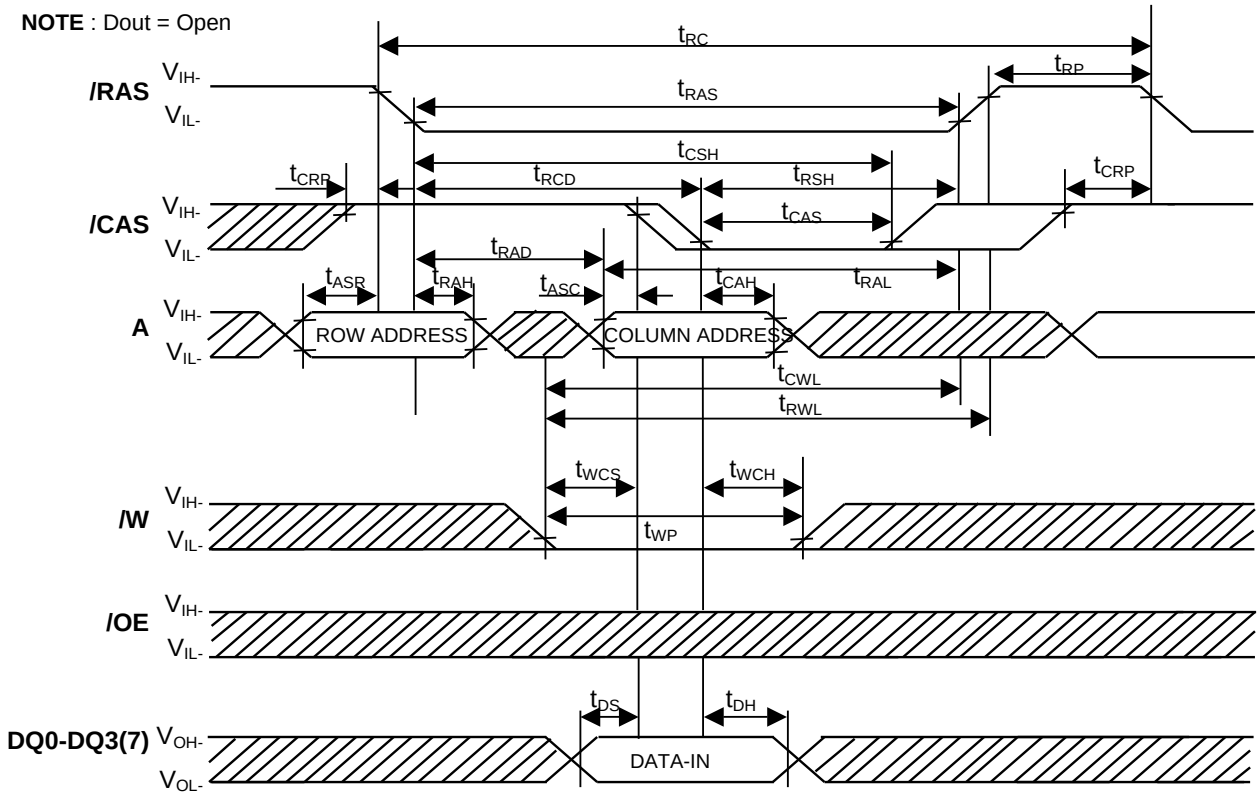
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE

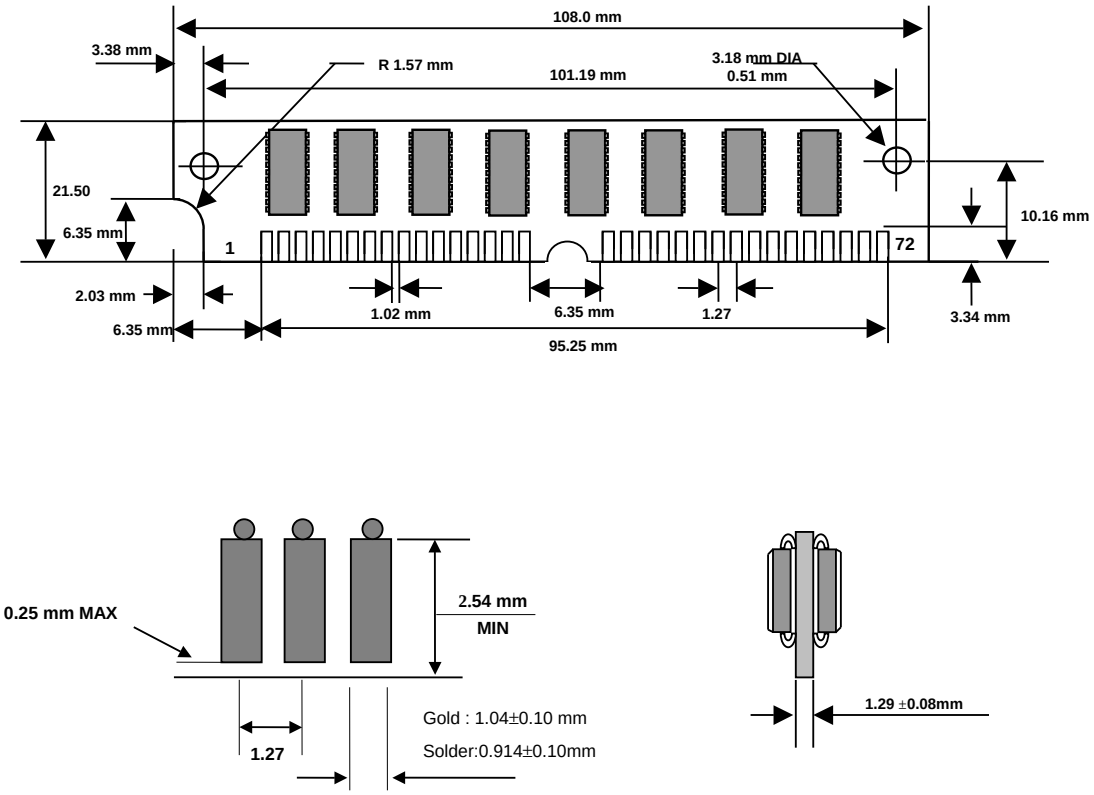


TIMING WAVEFORM OF WRITE CYCLE (EARLY WRITE)

NOTE : Dout = Open



PACKAGING INFORMATION



ORDERING INFORMATION

Part Number	Density	Org.	Package	Vcc	SPEED
HMD8M32M16G-5	32MByte	8MX 32bit	72 Pin-SIMM	5.0V	50ns
HMD8M32M16G-6	32MByte	8MX 32bit	72 Pin-SIMM	5.0V	60ns