

# PWRLITE LU1010DA

## High Performance N-Channel *POWERJFET™* with PN Diode



### Features

- ❖ Superior gate charge x R<sub>ds(on)</sub> product (FOM)
- ❖ Trench Power JFET with low threshold voltage V<sub>th</sub>.
- ❖ Device fully “ON” with V<sub>gs</sub> = 0.7V
- ❖ Optimum for “Low Side” Buck Converters
- ❖ Excellent for high frequency dc/dc converters
- ❖ Optimized for Secondary Rectification in isolated DC-DC
- ❖ Low R<sub>g</sub> and low C<sub>ds</sub> for high speed switching

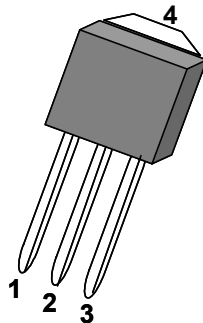
### Applications

- ❖ DC-DC Converters
- ❖ Synchronous Rectifiers
- ❖ PC Motherboard Converters
- ❖ Step-down power supplies
- ❖ VRM Modules

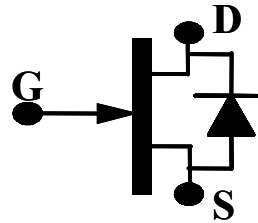
### Description

The Power JFET transistor from Lovoltech is a device that presents a Low R<sub>ds(on)</sub> allowing for improved efficiencies in DC-DC switching applications. The device is designed with a low threshold such that drivers can operate at 5V, which reduces the driver power dissipation and increases the overall efficiency. Lower threshold produces faster turn-on/turn-off, which minimizes the required dead time. A PN Diode is added for applications where a freewheeling diode is required. This product has tin plated leads.

### IPAK Lead-free Pin Assignments



Case TO251 (IPAK)



N – Channel PowerJFET  
with PN Diode

### Pin Definitions

Pin Number	Pin Name	Pin Function Description	Product Summary		
			V <sub>DS</sub> (V)	R <sub>ds(on)</sub> (Ω)	I <sub>D</sub> (A)
1	Gate	<b>Gate.</b> Transistor Gate	24V	0.0045	50 <sup>l</sup>
2, 4	Drain	<b>Drain.</b> Transistor Drain			
3	Source	<b>Source.</b> Transistor Source			

### Absolute Maximum Ratings

Parameter	Symbol	Ratings	Units
Drain-Source Voltage	V <sub>DS</sub>	24	V
Gate-Source Voltage	V <sub>GS</sub>	-12	V
Gate-Drain Voltage	V <sub>GD</sub>	-28	V
Continuous Drain Current	I <sub>D</sub>	50 <sup>l</sup>	A
Pulsed Drain Current	I <sub>D</sub>	100	A
Single Pulse Drain-to-Source Avalanche Energy at 25°C (V <sub>DD</sub> = 6V <sub>DC</sub> , I <sub>L</sub> =60A <sub>PK</sub> , L=0.3mH, R <sub>G</sub> =100 Ω)	E <sub>AS</sub>	220	mJ
Junction Temperature	T <sub>J</sub>	-55 to 150°C	°C
Storage Temperature	T <sub>STG</sub>	-65 to 150°C	°C
Lead Soldering Temperature, 10 seconds	T	260°C	°C
Power Dissipation (Derated at 25°C)	P <sub>D</sub>	80	W

## Thermal Resistance

Symbol	Parameter		DPAK Ratings	Units
$R\theta_{JA}$	Thermal Resistance Junction-to-Ambient		80	°C/W
$R\theta_{JC}$	Thermal Resistance Junction-to-Case		1.56	°C/W

## Electrical Specifications

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

The  $\phi$  denotes a specification which apply over the full operating temperature range.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>Static</b>						
$BV_{DSX}$	Breakdown Voltage Drain to Source	$I_D = 0.5 \text{ mA}$ $V_{GS} = -4 \text{ V}$	24	28		V
$BV_{GDO}$	Breakdown Voltage Gate to Drain	$I_G = -50 \mu\text{A}$		-32	-28	V
$BV_{GSO}$	Breakdown Voltage Gate to Source	$I_G = -50 \mu\text{A}$		-14	-12	V
$R_{DS(ON)}$	Drain to Source On Resistance <sup>2</sup>	$I_G = 40 \text{ mA}, I_D = 10 \text{ A}$ $I_G = 10 \text{ mA}, I_D = 10 \text{ A}$ $I_G = 5 \text{ mA}, I_D = 10 \text{ A}$		3.7 3.8 3.9	4.5 5.0	m $\Omega$ m $\Omega$
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = 0.1 \text{ V}, I_D = 250 \mu\text{A}$		-1		V
$TCV_{GSTH}$	Temperature Coefficient of Gate Threshold Voltage	$V_{DS} = 0.1 \text{ V}, I_D = 250 \mu\text{A}$		-2.8		mV/°C
<b>Dynamic</b>						
$Q_{Gsync}$	Total Gate Charge Sync JFET	$\Delta V_{Drive} = 5 \text{ V}, V_{DS} = 0.1 \text{ V}$		12.6		nC
$Q_G$	Total Gate Charge	$\Delta V_{Drive} = 5 \text{ V}, I_D = 10 \text{ A}, V_{DS} = 15 \text{ V}$		15		nC
$Q_{GD}$	Gate to Drain Charge	$V_{DS} = 13.5 \text{ V to } V_{DS} = 1.5 \text{ V}$		10.5		nC
$Q_{GS}$	Gate to Source Charge	$V_{GS} = -4.5 \text{ V to } V_{DS} = 13.5 \text{ V}$		4.5		nC
$Q_{SW}$	Switching Charge	$V_{GS} = -2 \text{ V to } V_{DS} = 1.5 \text{ V}$		11.4		nC
$R_G$	Gate Resistance			0.4		$\Omega$
$T_{D(ON)}$	Turn-on Delay Time	$V_{DD} = 15 \text{ V}, I_D = 10 \text{ A}$ $V_{Drive} = 5 \text{ V}$ Resistive Load		6.7		ns
$T_R$	Rise Time			12.4		
$T_{D(OFF)}$	Turn-off Delay			9		
$T_F$	Fall Time			4.6		
$C_{ISS}$	Input Capacitance	$V_{DS} = 10 \text{ V}, V_{GS} = -5 \text{ V}, 1 \text{ MHz.}$		1465		pF
$C_{OSS}$	Output Capacitance			611		
$C_{GS}$	Gate-Source Capacitance			972		
$C_{GD}$	Gate-Drain Capacitance			493		
$C_{DS}$	Drain-Source Capacitance			118		
<b>PN Diode</b>						
$I_R$	Reverse Leakage	$V_R = 20 \text{ V}, V_{GS} = -4 \text{ V}$			0.3	mA
$V_F$	Forward Voltage	$I_F = 1 \text{ A}$		800		mV
$V_F$	Forward Voltage	$I_F = 10 \text{ A}$		900		mV
$V_F$	Forward Voltage	$I_F = 20 \text{ A}$		960		mV
$Q_{rr}$	Reverse Recovery Charge	$I_s = 10 \text{ A di/dt} = 100 \text{ A/us,}$		9.5		nC
$T_{rr}$	Reverse Recovery Time	$I_s = 10 \text{ A di/dt} = 100 \text{ A/us,}$		14.6		ns

### Notes:

- Current is limited by bondwire; with an  $R_{thjc} = 1.56 \text{ }^\circ\text{C/W}$  the chip is able to carry 102A.
- Pulse width  $\leq 500 \mu\text{s}$ , duty cycle  $\leq 2\%$

## Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

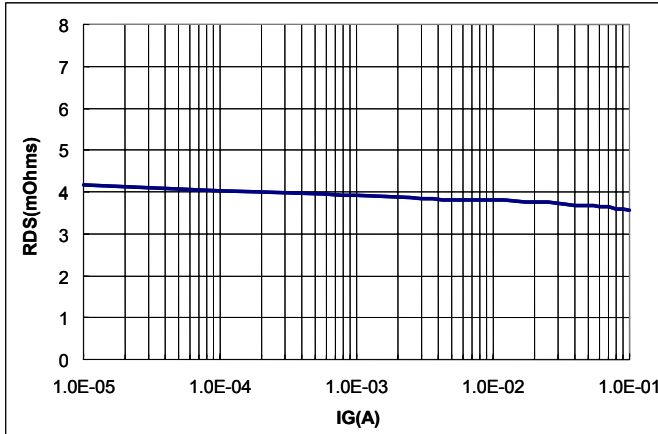


Figure 1 –  $R_{DS(on)}$  vs Gate Current at  $I_D = 10A$

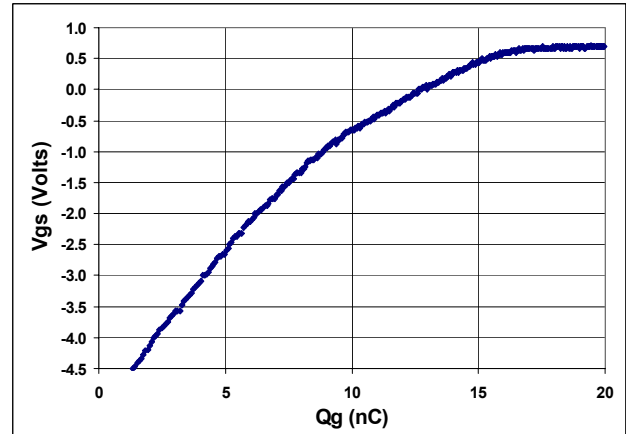


Figure 2 – Gate Charge for  $V_{DS} = 0.1V$

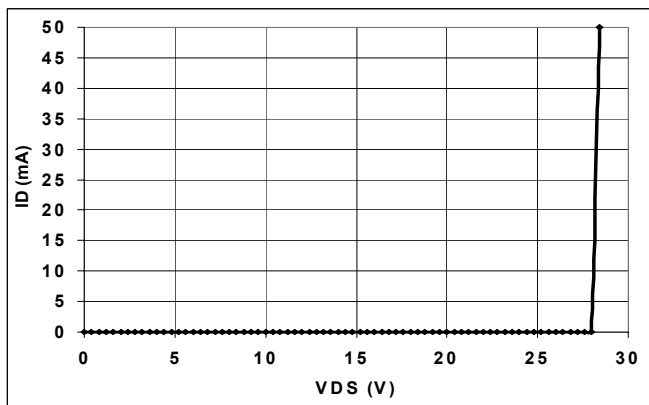


Figure 3 – Breakdown Voltage  $V_{DS}$  vs  $I_D$

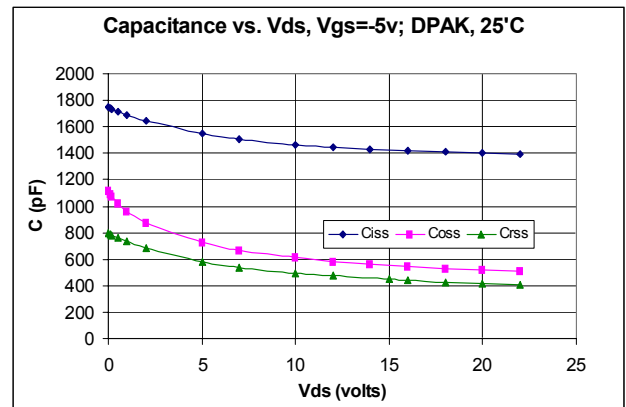


Figure 4 – Capacitance vs Drain Voltage  $V_{DS}$

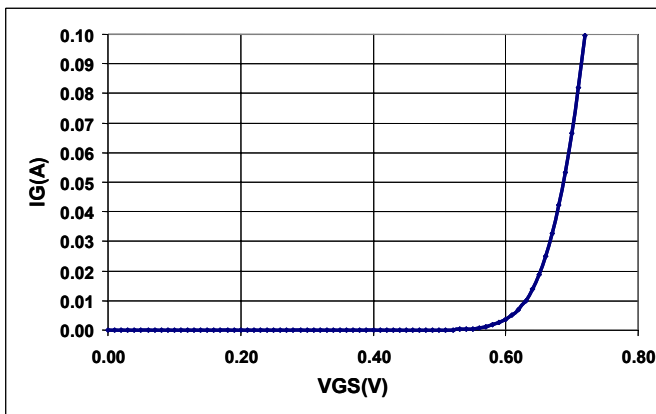


Figure 5 –  $I_G$  vs Gate Voltage  $V_{GS}$

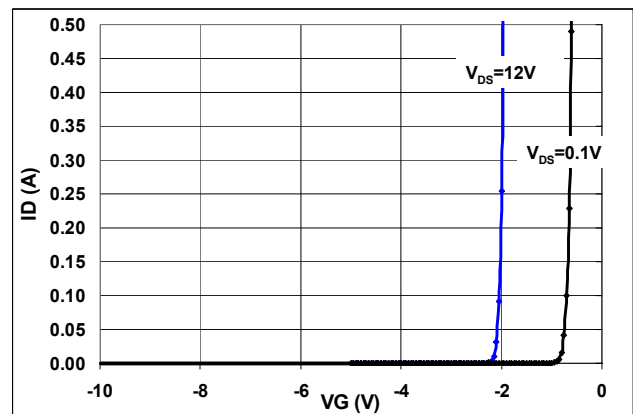


Figure 6 – Transfer Characteristic

## Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

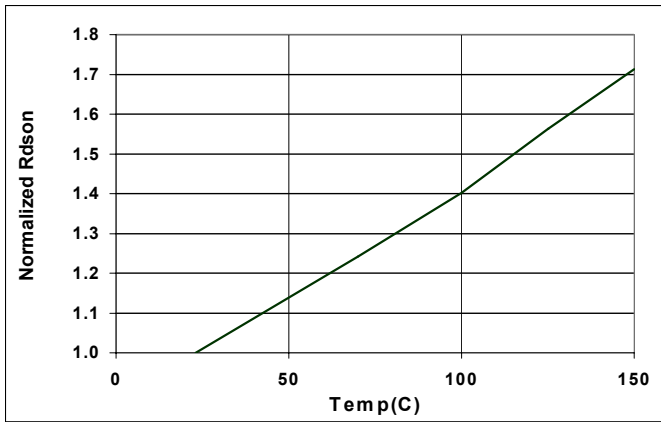


Figure 7 –  $R_{DS(on)} = f(T)$ ;  $I_D = -10\text{A}$ ;  $I_G = 50\text{mA}$

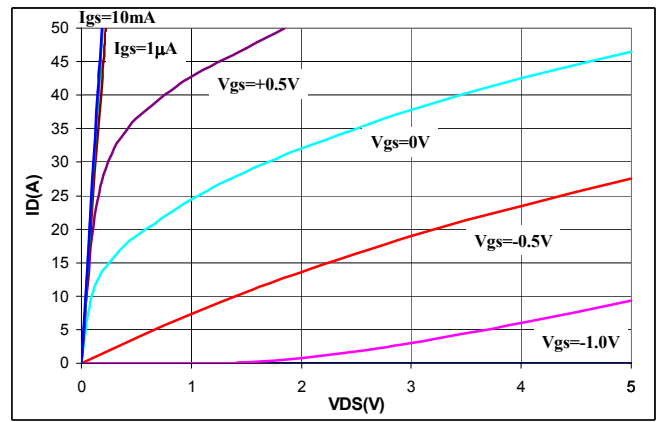


Figure 8 –  $I_D$  vs  $V_{DS}$  Characteristics

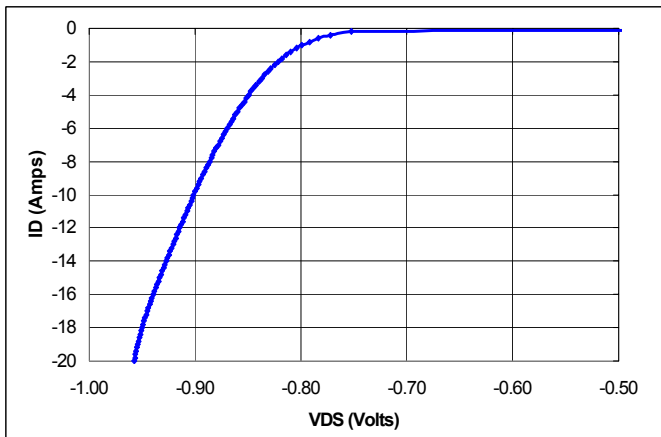


Figure 9 – PN Diode Voltage vs Current

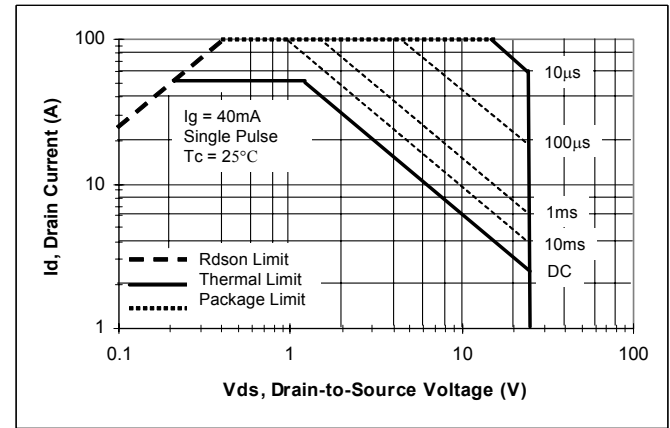


Figure 10 – Safe Operating Area

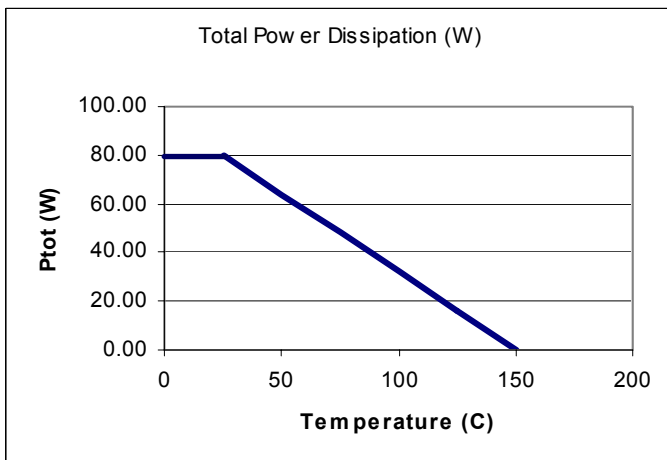


Figure 11 – Total Power Dissipation

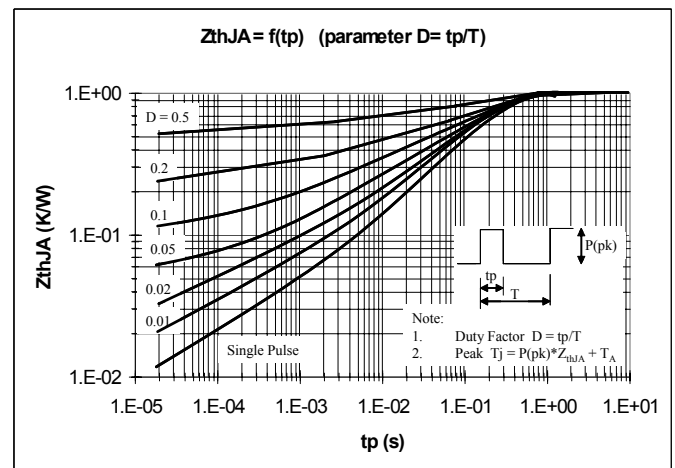


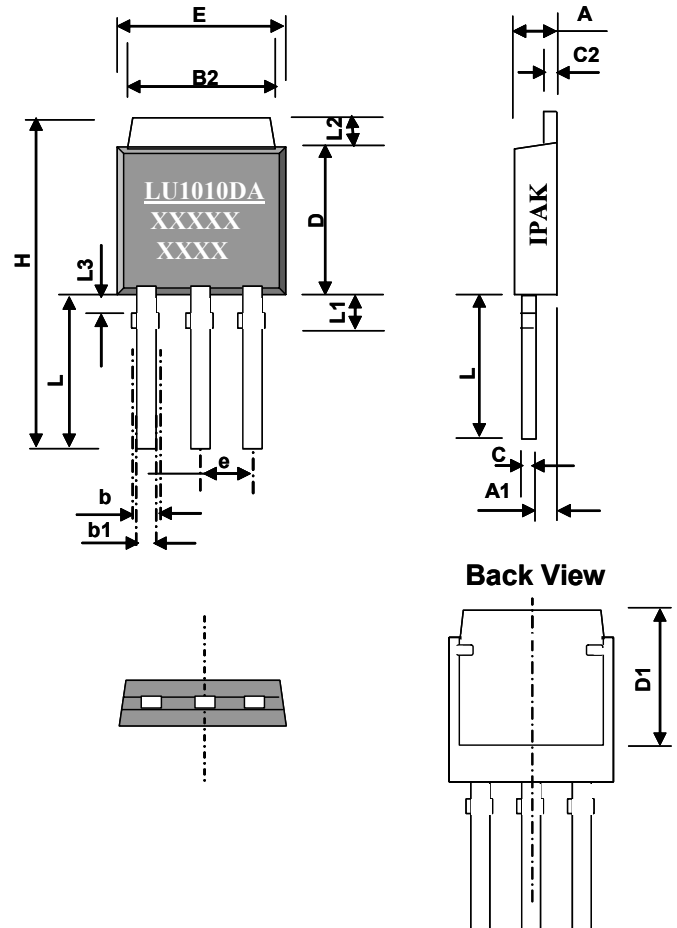
Figure 12 – Normalized Thermal Response

**Ordering Information**

Product Number	PN Marking	Package	Notes:
LU1010DA	LU1010DA	TO251 (IPAK)	<b>This product is Pb-Free and has Tin Plated leads</b>

**Package and Marking Information**

DIMENSIONS						
DIM.	mm.			inch		
	TYP.	MIN.	MAX.	TYP.	MIN.	MAX.
A		2.19	2.40	0.086	0.094	
A1		0.89	1.14	0.035	0.045	
b		0.76	1.14	0.030	0.045	
b1		0.64	0.90	0.025	0.035	
B2		5.20	5.46	0.205	0.215	
C		0.45	0.60	0.017	0.023	
C2		0.45	0.60	0.017	0.023	
D		5.97	6.22	0.235	0.244	
D1	5.64			0.222		
E		6.35	6.73	0.250	0.265	
e	2.28			0.090		
H	13.19	13.06	13.32	0.514	0.525	
L		5.95	7.6	0.234	0.300	
L1		2.03	2.29	0.079	0.090	
L3		0.63	1.14	0.025	0.045	


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- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Datasheet Identification	Product Status	Definition
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No Identification Needed	In Production	This datasheet contains final specifications. Lovoltech reserves the right to make changes at any time without notice in order to improve the design.