High Efficiency Boost Charge Pump Regulator

FEATURES

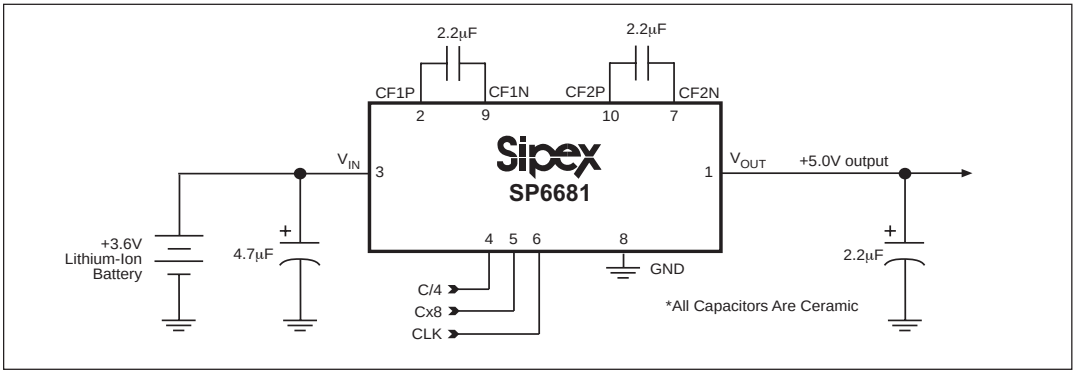
- Ideal for Li Ion or 3V to 5V Conversion
- Low Profile, Inductorless Regulator
- Up To 96% Power Efficiency
- +2.7V to +5.5V Input Voltage Range
- 5.0V, 50mA Output, 4% Accuracy
- Low EMI Design
- Low Quiescent Current: 175μA
- Low Shutdown Current: 4μA
- Optional External Clock: 32.768kHz
- Thermal Shutdown Protection
- Programmable Frequencies: 8.192kHz, 32.768kHz, or 262.14kHz
- Internal Oscillator: 16kHz or 130kHz, when CLK Pin Is Held High
- Ultra small 10-Pin MSOP Package

APPLICATIONS

- GSM SIM Card Power Supplies
- 3V to 5V Boost Applications
- Li Ion to 5.0V Boost Applications
- White LED Driver
- Smart Card Readers

DESCRIPTION

The SP6681 is a charge pump ideal for converting a +3.6V Li-Ion battery input to a +5.0V regulated output. An input voltage range of +2.7V to +5.5V is converted to a regulated output of 5.0V. The SP6681 device will operate at three different switching frequencies corresponding to three different output resistances and load current ranges. An external 32.768kHz nominal clock signal is used to produce three synchronized pump frequencies through the use an internal phase lock loop to drive the charge pump. Two control inputs can adjust the internal pump frequency on the fly to 8.192kHz (f_{INPUT} / 4), 32.768kHz (f_{INPUT} x 1), or 262.14kHz (f_{INPUT} x 8). The charge pump configuration dynamically changes to optimize power efficiency. At low input voltages the charge pump doubles the input while at higher inputs the output is 1.5 times the input. The SP6681 can deliver high power efficiencies up to 96% with low quiescent currents from 175μA to 800μA. The SP6681 is offered in a 10-Pin μSOIC package.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{IN}.....-0.3V to +6.0V
V_{OUT}.....-0.3V to +6.0V
I_{OUT}.....100mA
Storage Temperature.....-65˚C to +150˚C

Power Dissipation Per Package
10-pin mSOIC
(derate 8.84mW/^{O}C above +70^{O}C).....720mW
Junction Temperature.....125˚C

SPECIFICATIONS

V_{IN} = +2.75 to +5.5V, f_{CLK} = 32.768kHz, C_{IN} = 4.7µF (ceramic), CF1 = CF2 = C_{OUT} = 2.2µF, (ESR = 0.03 Ω) and T_{AMB} = -40°C to +85°C unless otherwise noted.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage, V_{IN}		2.75	3.6	5.5	V
Quiescent Current, I_Q	$f_{PUMP} = f_{CLK}/4$ $f_{CLK}=f_{PUMP}$ $f_{PUMP} = f_{CLK}/8$		175 230 580	250 300 1500	µA
In-Rush Current into V_{IN}, IN_{RUSH}	2.7V V_{IN} 5.5V, NOTE 1		500		mA
Off Current, I_{OFF}	clock not present		8	15	µA
Input Clock Freq., f_{CLK}	Operational (supplied externally)		32.768		kHz
Pump Frequency, f_{PUMP}	f_{CLK} C/4pin input Cx8pin input no input X X Present Low Low Present High Low Present X High High Low Low High Low High High High Low		0 32.768 8.192 262.140 16 130 0		kHz
Input Threshold Voltage V_{IL} V_{IH}	Digital inputs = f_{CLK}, $f_{CLK}/4$, f_{CLK} x 8	 1.3		0.4	V
Input Current $I_{IN(low)}$ $I_{IN(high)}$	Digital inputs = f_{CLK}, $f_{CLK}/4$, f_{CLK} x 8		0.1 1.0	10 10	µA
Mode Transition Voltage,	X1.5 to X2, V_{IN} falling $f_{pump} = f_{CLK}/4$, I_{LOAD} = 1mA f_{pump}, f_{CLK}, I_{LOAD} = 5mA	3.55 3.55	3.70 3.70	3.85 3.85	V
Hysteresis for Mode Transition Voltage	V_{IN} rising to V_{IN} falling		50		mVpp
Transient Response:	Max. Transient Amplitude; t=5µs I_{LOAD} f_{PUMP} 100µA to 2mA 8.192kHz 2mA to 20mA 32.768kHz 20mA to 50mA 262.14kHz		 1.5 1.5 1.5		%

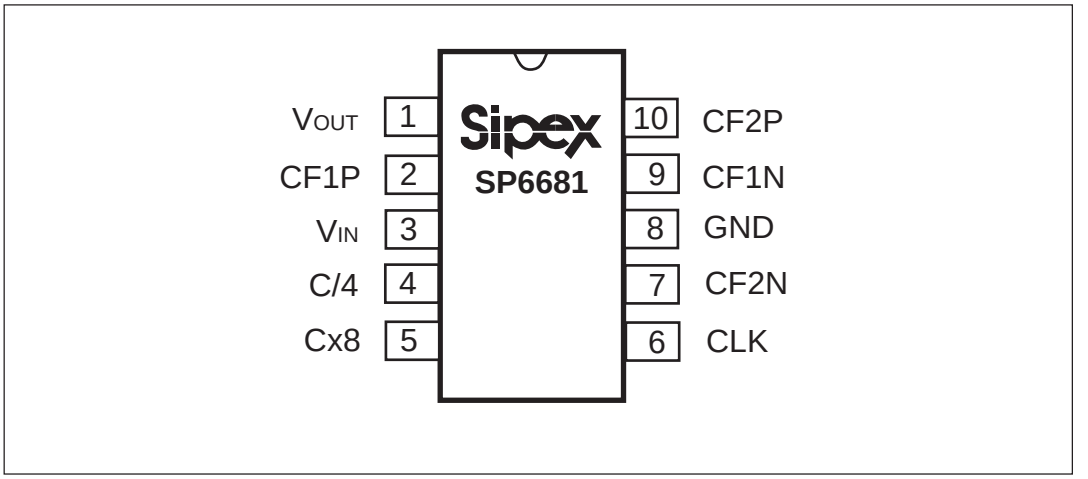
SPECIFICATIONS (CONT)

V_{IN} = +2.75 to +5.5V, f_{CLK} = 32.768kHz, C_{IN} = 4.7µF (ceramic), CF1 = CF2 = C_{OUT} = 2.2µF, (ESR = 0.03 Ω) and T_{AMB} = -40°C to +85°C unless otherwise noted.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Resistance, R_{OUT}	Mode: X2, V_{IN}=3.85V				
	I_{LOAD}=2mA f_{PUMP}=8.192kHz		60		
	10mA 32.768kHz		20		
	50mA 262.14kHz		12.5		
Average Output Voltage: Ave V_{OUT}	f_{PUMP}=8.192kHz; I_{LOAD}=2mA				
	V_{IN} Mode				
	3.0V X2	4.8	5.0	5.2	V
	3.55V X2	4.8	5.0	5.2	
	3.85V X1.5	4.8	5.0	5.2	
	3.5V X1.5	4.8	5.0	5.2	
	f_{PUMP}=32.768kHz; I_{LOAD}=10mA				
	V_{IN} Mode				
	3.0V X2	4.8	5.0	5.2	V
	3.55V X2	4.8	5.0	5.2	
	3.85V X1.5	4.8	5.0	5.2	
	3.5V X1.5	4.8	5.0	5.2	
	f_{PUMP}=262.14kHz; I_{LOAD}=50mA				
	V_{IN} Mode				
	3.0V X2	4.8	5.0	5.2	V
	3.55V X2	4.8	5.0	5.2	
	3.85V X1.5	4.8	5.0	5.2	
	3.5V X1.5	4.8	5.0	5.2	
Power Efficiency P_{EFF}	f_{PUMP}=8.192kHz; I_{LOAD}=2mA				
	V_{IN} Mode				
	3.0V X2		93		%
	3.55V X2		80		
	3.85V X1.5		92		
	3.5V X1.5		54		
	f_{PUMP}=32.768kHz; I_{LOAD}=10mA				
	V_{IN} Mode				
	3.0V X2		96		%
	3.55V X2		80		
	3.85V X1.5		92		
	3.5V X1.5		57		
	f_{PUMP}=262.14kHz; I_{LOAD}=50mA				
	V_{IN} Mode				
	3.0V X2		92		%
	3.55V X2		81		
	3.85V X1.5		91		
	3.5V X1.5		60		

NOTE 1: F_{CLK} applied 10ms after V_{IN} is present.

PINOUT



PIN ASSIGNMENTS

Pin 1— V_{OUT} — 5.0V regulated charge pump.

Pin 2 — CF1P — Positive terminal to the charge pump flying capacitor, CF1.

Pin 3 — V_{IN} — Input pin for the +2.7V to +5.5V supply voltage.

Pin 4 — C/4 — This is a control line for the internal charge pump frequency. When this control line is forced to a logic high, the internal charge pump frequency is set to $^1/_4$ of the CLK frequency, provided that Cx8 is low.

Pin 5 — Cx8 — This is a control line for the internal charge pump frequency. When this control line is forced to a logic high, the internal charge pump frequency is set to x8 of the CLK frequency.

Pin 6 — CLK — 32.768kHz Clock. Connect this input pin to an external 32.768kHz clock to drive the frequency of the charge pump. Logic low inputs on the C/4 and Cx8 pins sets the internal charge pump frequency according to *Table 1*. Shutdown mode for the device is set when there is no clock signal present on this input pin, or when it is pulled to ground.

Pin 7 — CF2N — Negative terminal to the charge pump flying capacitor, CF2.

Pin 8 — GND — Ground reference.

Pin 9 — CF2P — Positive terminal to the charge pump flying capacitor, CF2.

Pin 10 — CF1N — Negative terminal to the charge pump flying capacitor, CF2.

DESCRIPTION

The SP6681 device is a regulated CMOS charge pump voltage converter that can be used to convert a +2.7V to +5.5V input voltage to a nominal +5.0V output. These devices are ideal for cellular phone designs involving battery-powered and/or board level voltage conversion applications.

An external clock signal with a frequency of 32.768kHz nominal is required for device operation. A designer can set the SP6681 device to operate at 3 different charge pump frequencies: 8.192kHz (f_{INPUT} / 4), 32.768kHz (f_{INPUT} x 1), and 262.14kHz (f_{INPUT} x 8). The three frequencies correspond to three nominal load current ranges: 2mA, 20mA, and 50mA, respectively. The SP6681 device optimizes for high power efficiency with a low quiescent current of 175µA at 8.198kHz, 230µA at 32.768kHz, and 800µA at 262.14kHz. When there is no external clock signal input, the device is in a low-power shutdown mode drawing 4.4µA (typical) current.

The SP6681 device is ideal for designs using +3.6V lithium ion batteries such as cell phones, PDAs, medical instruments, and other portable equipment. For designs involving power sources above +2.7V up to +5.5V, the internal charge pump switch architecture dynamically selects an operational mode that optimizes efficiency. The SP6681 device regulates the maximum output voltage to +5.0V.

THEORY OF OPERATION

There are seven major circuit blocks for the SP6681 device. Refer to *Figure 1*.

1) The Voltage Reference contains a band gap and other circuits that provide the proper current biases and voltage references used in the other blocks.

2) The Clock Manager accepts the digital input voltage levels (including the input clock) and translates them to V_{CC} and 0V. It also determines if a clock is present in which case the device is powered up. If the CLK input is left floating or pulled near ground, the device shuts down and V_{IN} is shorted to V_{OUT}. The worst case digital low is 0.4V and the worst case digital high is 1.3V. This block contains a synthesizer that generates the internal pump clock which runs at the frequency controlled with the C/4 and Cx8 logic pins.

3) The Charge Pump Switch Configuration Control determines the pump configuration depending upon V_{IN} as described earlier and programs the Clock Phase Control. For an input supply voltage from +2.7V to +3.7V, an X2 doubling architecture is enabled. This mode requires one flying capacitor and one output capacitor. For an input supply voltage greater than +3.7V up to +5.5V, an X1.5 multiplier architecture is enabled. This mode requires two flying capacitors and one output capacitor.

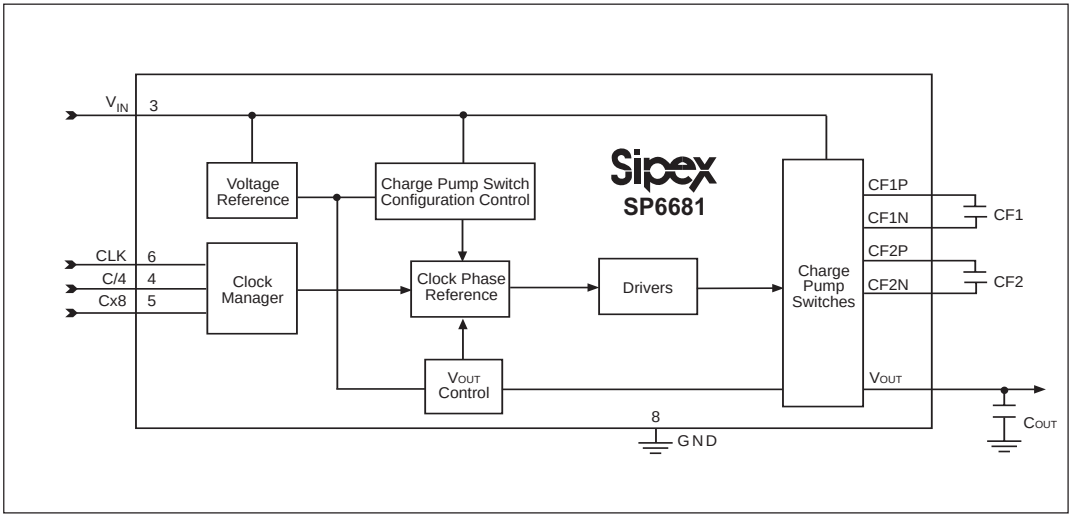


Figure 1. Internal Block Diagram of the SP6681

4) The Clock Phase Control accepts the clock and mode control generated by the Clock Manager and the Charge Pump Switch Configuration Control. This block then provides several clock phases going to the Drivers block.

5) The V_{OUT} Control regulates the Clock Phase Control to ensure V_{OUT} is regulated to 5.0V.

6) The Drivers block drives the clock phase information to the gates of the large pump transistors.

7) The Charge Pump Switch block contains the large transistors that transfer charge to the fly and load capacitors.

In normal operation of the device V_{IN} is connected between +2.7 and 5.5V. Refer to Figure 2 for a typical application circuit. When no clock is present (CLK is floating or near ground) the device is in shutdown and the output is connected to the input. This shutdown feature will work either in start up or after the device is pumping. Once a clock is present, the band gap is activated, but only if V_{IN} > 2.3V. Otherwise the device remains in shutdown mode. Once the reference voltage is stable, the device begins the pumping operation.

If V_{IN} < 3.70V, the device is configured as a doubler. However, as the output reaches 5.0V, the doubler action is truncated.

If V_{IN} is above 3.70V, the device is reconfigured and multiplies the input by a factor of 1.5. This mode reduces the current drawn from the supply and hence increases the power efficiency. As the output reaches 5.0V, the charge transfer to the load capacitor is truncated.

APPLICATION INFORMATION

Refer to Figure 3 for a typical SIM card application circuit with the SP6681.

Oscillator Control

The external clock frequency required to drive the internal charge pump oscillator is 32.768kHz (nominal) at the CLK pin. When there is no clock signal present at the CLK pin, the SP6681 device is in a low-power shutdown mode.

C/4 and Cx8 are two control lines for the internal charge pump oscillator. When the C/4 control line is forced to a logic high and the Cx8 control line is at a low, the internal charge pump oscillator is set to 8.192kHz. When both the C/4 and Cx8 control lines are at a logic low, the internal charge pump oscillator is set to the input clock signal, 32.768kHz. When the C/4 control line is forced to a logic high, the internal charge pump oscillator is set to 262.14kHz.

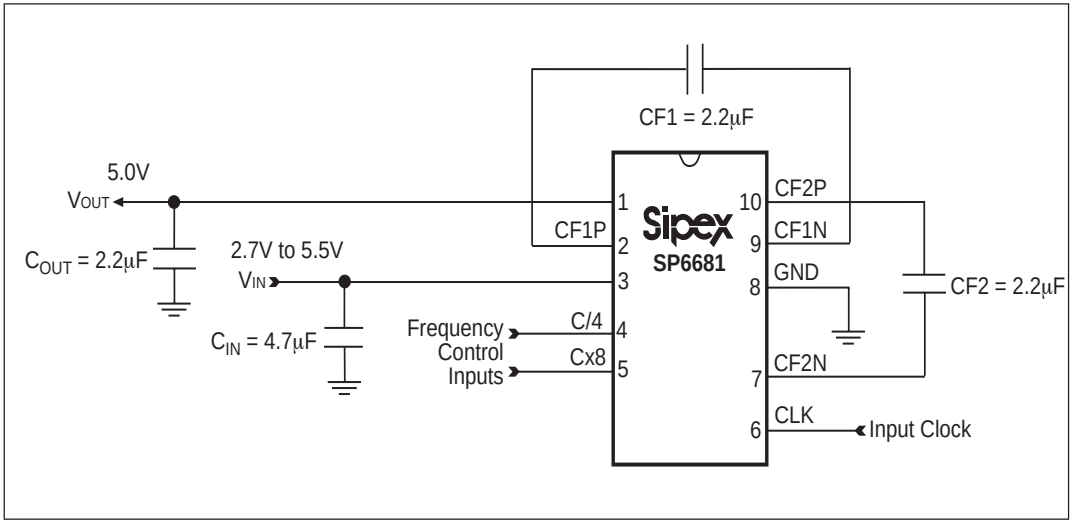


Figure 2. Typical Application for the SP6681

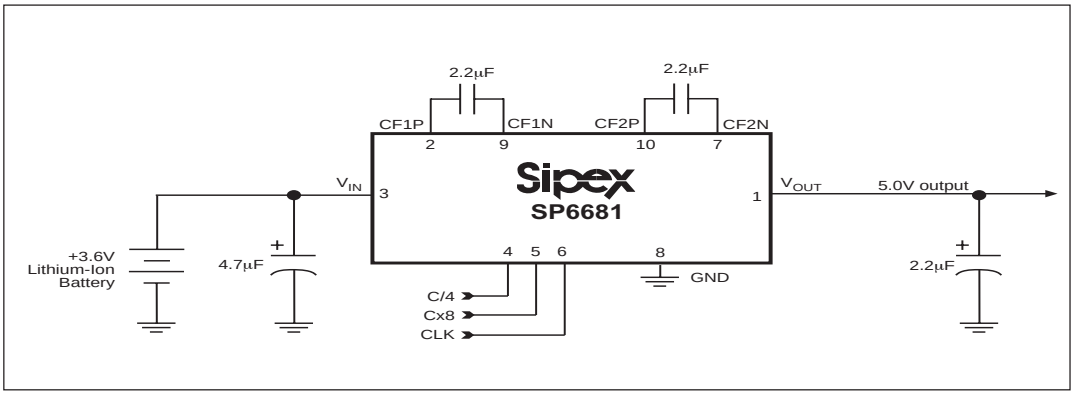


Figure 3. Typical SIM Card Application Circuit for the SP6681

Any standard CMOS logic output is suitable for driving the C/4 or Cx8 control lines as long as logic low is less than 0.4V and logic high is greater than 1.3V.

CLK pin	C/4 pin	Cx8 pin	f_{PUMP}
not present	X	X	0
32.768kHz	low	low	32.768kHz
32.768kHz	low	high	262.14kHz
32.768kHz	high	low	8.192kHz
32.768kHz	high	high	262.14kHz

Table 1. Control Line Logic for the Internal Charge Pump Oscillator

Efficiency

Power efficiency with the SP6681 charge pump regulator is improved over standard charge pumps doubler circuits by the inclusion of an 1.5X output mode, as described in the Theory of Operation section. The net result is an increase in efficiency at battery inputs greater than 3.7 to 3.8V where the SP6681 switches to the 1.5X mode.

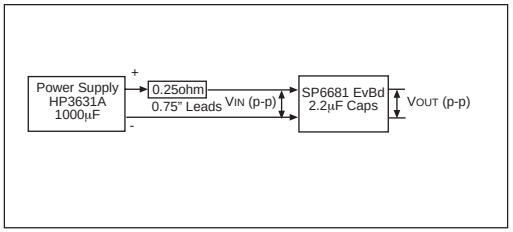


Figure 4. Capacitor Selection Test Circuit

Capacitor Selection

In order to maintain the lowest output resistance, input ripple voltage and output ripple voltage, multi-layer ceramic capacitors with inherently low ESR are recommended. Refer to Table 2 for some suggested low ESR capacitors. Tables of output resistance and ripple voltages for a variety of input, output and pump capacitors are included here to use as a guide in capacitor selection. Measured conditions are with CLK = 32kHz, 5mA output load and all capacitors are 2.2uF except when stated otherwise. A DC power supply with added 0.25ohm output ESR was used to simulate a Lithium Ion Battery as shown in figure 4.

Board Layout

PC board layout is an important design consideration to mitigate switching current effects. High frequency operation makes PC layout important for minimizing ground bounc and noise. Components should be place as close to the IC as possible with connections made through short, low impedance traces. To maximize output ripple voltage, use a ground plane and solder the IC's GND pin directly to the ground plane.

MANUFACTURER / TELEPHONE #	PART NUMBER	CAPACITANCE / VOLTAGE	MAX ESR @ 100kHz	CAPACITOR SIZE / TYPE
TDK / 847-803-6100	C2012X5R1A225K	2.2µF / 10V	0.030Ω	0805 / X5R
TDK / 847-803-6100	C3216X5R1C475K	4.7µF / 10V	0.020Ω	1206 / X5R
AVX / 843-448-9411	1206ZC225K	2.2µF / 10V	0.030Ω	1206 / X7R
Taiyo Yuden / 847-925-0888	LMK212BJ225MG	2.2µF / 10V	0.030Ω	0805 / X5R
Taiyo Yuden / 847-925-0888	LMK316BJ475ML	4.7µF / 10V	0.020Ω	1206 / X7R

Table 2. Suggested Low ESR Cermic Surface Mount Capacitors.

The SP6681 circuit shown in figure 5 acts as a 3.3V in to 5V out for biasing the two 5V Logic Level N-channel MOSFETs used in a step-down DC/DC converter. The high current switching path is from the +3.3V bus through the N-channel MOSFETs and inductor L1 to the output capacitors. To fully enhance Logic-Level N-channel MOSFETs, +5V is needed from the SP6681 output to the SP6120 VCC pin, which supplies the low-side MOSFET MN1 with a 0V to 5V gate pulse through the GL pin.

For the top-side MOSFET MN2 (which has a floating gate driver biased at the BST pin), the boost pin BST is charge pumped up from the 0 to 3.3V switching at the switch node pin SWN, with an additional 5V from SP6681 output, through the DBST diode to a total of 8.3V when the SWN is at 3.3V, or a total of 5V from gate to source to fully enhance the MOSFET MN2. For a more detailed schematic of a step-down DC/DC converter, see the SP6120 datasheet.

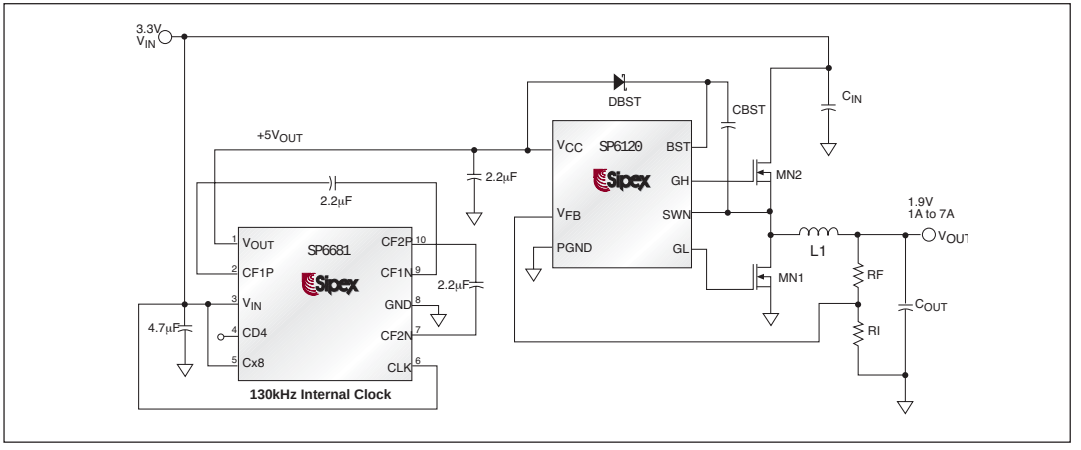
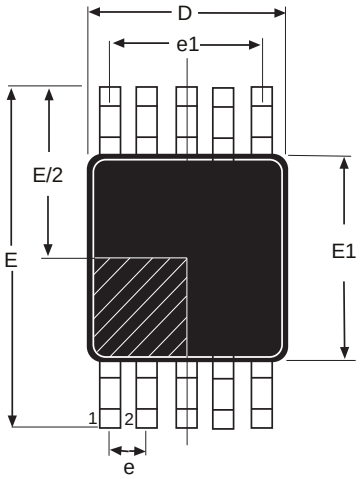
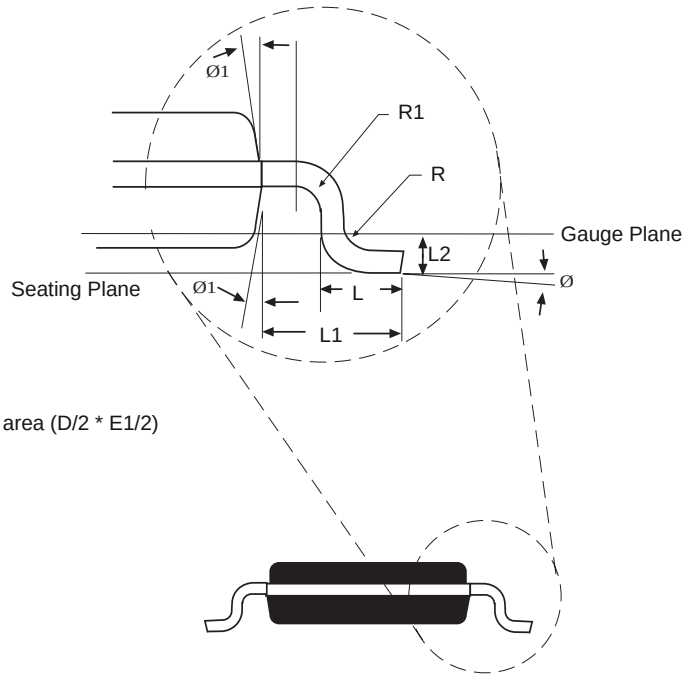


Figure 5. SP6681 Circuit as a 3.3V to 5.0V Boost for 5V N-Channel MOSFETs in Buck DC/DC Converter Circuit.

PACKAGE: 10-PIN MSOP

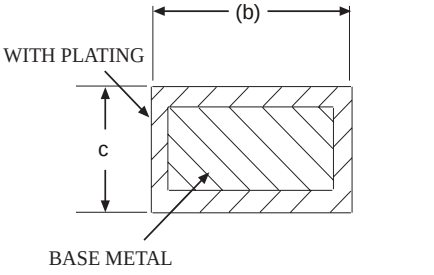
(ALL DIMENSIONS IN MILLIMETERS)

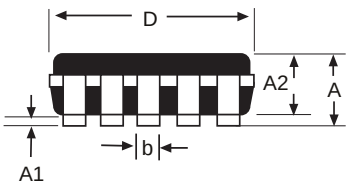




Pin #1 indentifier must be indicated within this shaded area (D/2 * E1/2)

Dimensions in (mm)	10-PIN MSOP JEDEC MO-187 (BA) Variation		
	MIN	NOM	MAX
A	-	-	1.1
A1	0	-	0.15
A2	0.75	0.85	0.95
b	0.17	-	0.27
c	0.08	-	0.23
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
e	0.50 BSC		
e1	2.00 BSC		
L	0.4	0.60	0.80
L1	-	0.95	-
L2	-	0.25	-
N	-	10	-
R	0.07	-	-
R1	0.07	-	-
Ø	0º		8º
Ø1	0º	-	15º





ORDERING INFORMATION

Model	Temperature Range	Package Type
SP6681EU	-40˚C to +85˚C	10-pin MSOP
SP6681EU/TR	-40˚C to +85˚C	(tape and reel) 10-pin MSOP

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