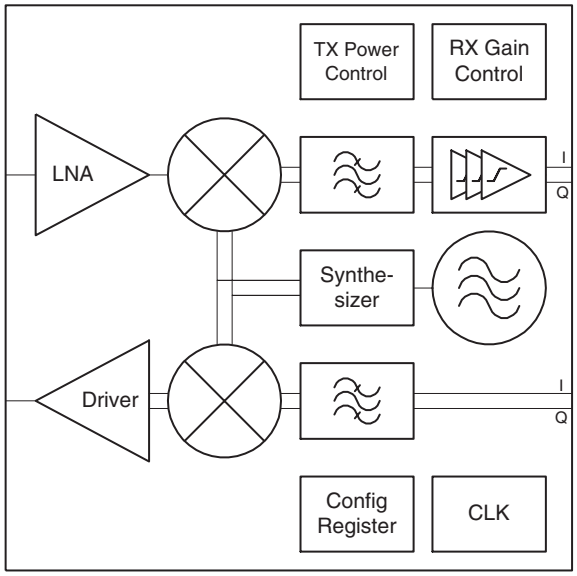
Features

- **Single-chip WiMax Transceiver @ 3.5GHz**
- **Fully Differential Design**
- **Low-IF Receiver Architecture; Requires No External Filters**
- **Self Calibration Mode for RX / TX Filters**
- **Supports Channel Bandwidths of 1.75, 3.5, and 7MHz**
- **Modulation up to 64QAM**
- **Ultra-fast Fractional-N Synthesizer**
- **Sensitivity < -68dBm @ 64-QAM, CR=¾, 7MHz BW**
- **Phase Noise Synthesizer: 0.8° (-37dBc)**
- **Low Supply Voltage: 2.7V**
- **TX Output PRF: -12 dBm**
- **RX/TX Operating Current: 200/320mA Typical**
- **Low Power Off Current: < 20µA Typical**
- **56-lead QFN Package**
- **Low External Component Count of only a few Passives**

Applications

- **3.5 GHz Band Wireless Communication Devices**
- **IEEE® 802.16-2004 Radios**
- **Supports OFDM up to 64QAM**

Figure 1. AT86RF535A Block Diagram



WiMax Transceiver 802.16-2004

AT86RF535A

Preliminary

5108B–WiMax–2/06

Description

Atmel's AT86RF535A is a fully integrated, low cost RF 3.5GHz Low-IF conversion transceiver for WiMax applications. It combines excellent RF performance with low current consumption at the smallest die size. The AT86RF535A chip is fabricated on the advanced AT46000 SiGe BiCMOS process. The transceiver combines LNA, PA driver, RX/TX mixer, RX/TX filters, VCO, Synthesizer, RX Gain control, and TX Power control, all fully digital controlled. The number of external components is limited to only a few devices.

Quick Reference Data

Table 1. Quick Reference Data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{RF}	Input Center Frequency		3.4	3.55	3.7	GHz
DFRS	Frequency Resolution				39.2	Hz
V_{DD}	Supply Voltage	Applied to VDD pins	3.0	3.3	3.6	V
I_{DDRX}	Supply Current	Receive mode		200		mA
I_{DDTX}	Supply Current	Transmit mode, -5 dBm includes Balun		320		mA
I_{DDPOFF}	Supply Current	Power-off mode, only in "External CLK oscillator" mode		20		µA
SENS	Sensitivity QPSK Sensitivity 64QAM	BW=1.75MHz, CR=½, S/N=9.4dB BW=7MHz, CR=¾, S/N=24.4dB			−89 −68	dBm
P_{RF}	TX Output Power	FRF= 3.5 GHz, 15dB back off for 64QAM, EVM=-34dB, includes Balun		−12		dBm
PN	Integrated Phase Noise of Synthesizer	Integrated over Frequency Range 50kHz …1MHz		0.8		deg rms
T_{AMB}	Operating Ambient Temperature		−30	27	+70	°C

Note: All voltages are referenced to GND. VDD=3.0V TAMB=27°C, unless otherwise noted.

Electrical Characteristics

Table 2. Receiver Characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
System						
F_{RF}	Input Center Frequency		3.4	3.55	3.7	GHz
Z_{IN}	Differential Impedance at LNA Input	Includes a matching inductor and two series capacitors		50		Ω diff.
SENS	Sensitivity QPSK 1/2 Sensitivity 64QAM 3/4	BW=1.75MHz, S/N=9.4dB BW=7MHz, S/N=24.4dB			–90 –69	dBm
$P_{IN,MAX}$	Maximum Input Power	BW=7MHz, EVM=24.4dB	-20			dBm
NF_{SSB}	Noise Figure Single Side Band	High gain mode, includes Balun w/o Frontend loss		4	5	dB
$G_{RX,STEP}$	RX Chain: Gain Steps			0.76		dB
$G_{RX,RANGE}$	RX Chain: Gain Range			95.5		dB
$t_{RX/TX}$	RX to TX Switching Time				5	µs
L_{LO-ANT}	LO Leakage to Antenna	All gain modes, includes Balun			tbd	dBm
ACR±1	Adjacent Ch. Rejection	16QAM 3/4 64QAM 3/4			–11 -4	dB
ACR±2	Nonadjacent Ch. Rejection	16QAM 3/4 64QAM 3/4			–30 –23	dB
Baseband filters, DC cancellation, RSSI, IQ outputs						
R_{OUT}	Output load resistance	Pin to GND	1			MΩ
C_{OUT}	Output load capacitance	Pin to GND			10	pF
V_{OMAX}	Maximum Output Voltage	Differential	1			V
V_{OUT}	Nominal I or Q output Voltage	Differential at the load specified Output buffer gain offset = 0dB Backoff –15dB relative to I or Q		0.141		Vrms
$G_{B,OFFSTEP}$	I, Q output buffer: Gain Offset Steps			0.76		dB
$G_{B,RANGE}$	I, Q output buffer: Gain Range		–9		+2.25	dB
BW_{3dB}	3-dB Bandwidth of Filter	Low-IF Center Frequency: 1MHz 2MHz 4MHz Note 2		 1.75 3.5 7		MHz
IMRR	Image Rejection Ratio	Note 3		–42	–36	dB
FIF	Low-IF Frequency	Note 2		1.0 2.0 4.0		MHz
CMD	Common Mode IQ Voltage		0.9	1.0	1.1	V DC

Note: 1. VDD=3.0V, TAMB=27°C, FRF=3.55 GHz, specific application circuit TBD, unless otherwise noted
2. Internally adjusted by built-in self test
3. Calibration vector access able over SPI Register

Table 3. Transmitter Characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
System						
F_{RF}	Output Center Frequency		3.4	3.55	3.7	GHz
Z_{OUT}	Differential Impedance at Driver Output			50		Ω diff
P_{OUT}	TX Output Power	For 64QAM modulated signals		-12		dBm
$t_{TX/RX}$	TX to RX Switching Time				tbd	µs
$G_{PA,RANGE}$	TX Chain Gain Control Range		50	71.9		dB
$G_{LSB,STEP}$	TX Chain Gain Control LSB Step Size			0.76		dB
BW_{3dB}	3-dB Bandwidth of Filter	Low-IF Center Frequency: 1MHz 2MHz 4MHz Note 2		 1.75 3.5 7		MHz
L_{Carr}	Carrier Leakage	Note 3		-43		dBc
EVM	Error Vector Magnitude	64QAM 3/4			–34	dB
Z_{IN}	IQ Input Impedance	Differential		10		kΩ diff
V_{IN}	IQ Input Voltage	Peak, Differential		1		Vp,diff
$V_{IN, DC}$	DC Input Voltage			1.05		V

Note: 1. VDD=3.0V, TAMB=27°C, FRF=3.55 GHz, specific application circuit TBD, unless otherwise noted
2. Internally adjusted by built-in self test
3. Calibration vector access able over SPI Register.

Functional Description

The AT86RF535A is a fully integrated, low-cost Low-IF conversion transceiver for WiMax applications and is based on the IEEE 802.16-2004 standard. This product will provide transmit, receive, and frequency synthesis functions OFDM modulation schemes, as defined in the above specifications. It combines excellent RF performance at low current consumption. The transceiver combines LNA, PA driver, RX/TX mixer, RX/TX filters, VCO, Synthesizer, RX gain control, and TX power control, all fully digital controlled. The number of external components is limited to only a few devices. The AT86RF535A consists of a frequency-agile RF transceiver intended for use in 3.5-GHz licensed bands at data rates up to 26Mbps. Configuration and control registers and a bi-directional data communications interface to existing baseband devices from different vendors will be included. The AT86RF535A addresses the requirements of base station (BS) as well as subscriber station (SS) equipment. The device will operate down to 3.0V. The AT86RF535A is fabricated in Atmel's AT46000 advanced SiGe BiCMOS process technology and is assembled in a 8mm x 8mm 56-lead QFN package.

RX Path

The differential low noise amplifier (DLNA) makes use of a differential bipolar stage with resistive emitter linearization. For digital gain control operation, the DLNA supports the four gain modes

0, 6, 12, and 18dB. The linearity improves as the gain is reduced. The differential inphase quadraturephase mixer (IQMIX) utilizes a differential bipolar stage with emitter degeneration for the best linearity performance. A complex driving LO source was chosen for optimal LO leakage cancellation. The IQMIX has 4, 10, 16, and 22dB switchable gain.

The receive poly phase filter (RXPPF) is designed as a frequency shifted leapfrog structure. The filter provides three different bandwidths at three different center frequencies. The bandwidth of this filter is tuned by built-in self test (BIST). The tuning process adjusts the cap values within the filter after power-up. The tuning can be determined via SPI. Image rejection is calibrated via SPI.

Three digital controlled gain amplifiers (DGA1-3) are used to make necessary amplification available. Each stage supports the four gain modes 0, 6, 12, and 18dB. An additional fine gain stage DGB enables gain tuning of approximately ± 6dB in 0.76 dB steps. An output buffer gain offset matches the voltage swing to the respective BB input stage.

The gain control is completely digital and affects LNA, MIX, and the three DGAs by using the same granularity for each stage. The BB/MAC provides the gain vector at a separate serial interface. A fast TX/RX switching is possible via TX/RX switch input pins controlled by the BB/MAC.

The Low-IF conversion receiver does not have to amplify DC signals. But the gain setting produces different offsets in gain stages related to the output. To prevent signal saturation effects contribution, an offset correction takes place after each gain step. For dynamic range reasons, every stage has its individual offset correction stage. The DC feedback (DCFB) works as output offset compensation network which depends on actual gain setting. The internal gain control operation is optimized for fixed target amplitude. To adapt to different application requirements, the IQ output buffer DGB has a programmable gain offset from –1.5dB to 6dB in increments of 0.76dB. So, the nominal output voltage can be set between 180mVp and 650mVp. The gain is controllable via the register. The IQOB is able to drive a capacitive load on all four-output ports (RXI1, RXI2, RXQ1, RXQ2). The external pin CMD is an output pin, which delivers the common mode output voltage of the DGB.

TX Path

The transmit low pass filter (TXLP) filter is band limited concerning emission regulation and OFDM signals. So the input signal at the four-input ports (TXI1, TXI2, TXQ1, TXQ2) driving the TXLP could be a digital one but with defined levels. The complex filtered BB signal is upconverted with IQ Low-IF Upconverter IQUC. A complex driving LO source is chosen for optimal LO leakage cancellation. The output currents of the two mixer stages are added together. The resulting signal drives the power amplifier control (PAC) block. PAC is a Gilbert cell based current domain amplifier. Gain is controlled by DC voltage across the mixer core. In that way linear to dB gain control is achieved. The BB/MAC provides the gain setting vector at a separate serial interface.

Synthesizer

Voltage controlled oscillator (VCO) works at doubled LO frequency. This enables building complex LO phases for IQMIX and IQUC easily by using a divide by two and reduces load-pulling effects regarding DC current swing of the integrated PA. The VCO utilizes a differential double-grounded bipolar stage as core and tank; the latter is made up of an inductive and a capacitive part in parallel. No external devices are necessary. The capacitive part consists of a digital controlled switch cap tuning array and analog controlled varactor. The main reason to use a

combined analog and digital – hybrid – operating phase locked loop (Hybrid PLL) is to overcome tolerance, noise and integration problems in the VCO.

Because of the course digital tuning, the analog tuning gain could be reduced so that the characteristic impedance of the loop filter increases and the charge pump current is reduced. That helps to integrate the whole active loop filter (APLL).

Use of two (proportional and integral component) charge pumps and programming their currents permit changing of filter parameters.

The phase interpolation divider (PDIV) is an alternate of a conventional modulus divider. It has the speed and power advantages of an asynchron divider and is programmable in a restricted range.

Calibration Support

Calibration of transceiver imbalances has to be performed by appendant BB/MAC processor. This processor generates corresponding control signals. The AT86RF535A contains additional analog calibration modules detecting for excellent calibration support:

1. LO signal leakage,
2. IQ signal imbalances in the TX Path, and
3. IQ signal imbalances in the RX Path.

The control values will be given as analog control voltage.

SPI Interface

Serial peripheral interface (SPI) controls the transceiver. This 4-wire bus contains the ports SDE, SCL, SDI and SDO. The SPI has an 8-bit organization. Each transmission starts with a command byte with following structure:

Table 4. SPI Interface Structure

MSB							**LSB**
CMD	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0

The command bit CMD is set to “1“ for WRITE operation and “0” for READ operation.

The transmission continues with the data bytes. The number of data bytes depends on the register. The MSB of each data byte is sent first.

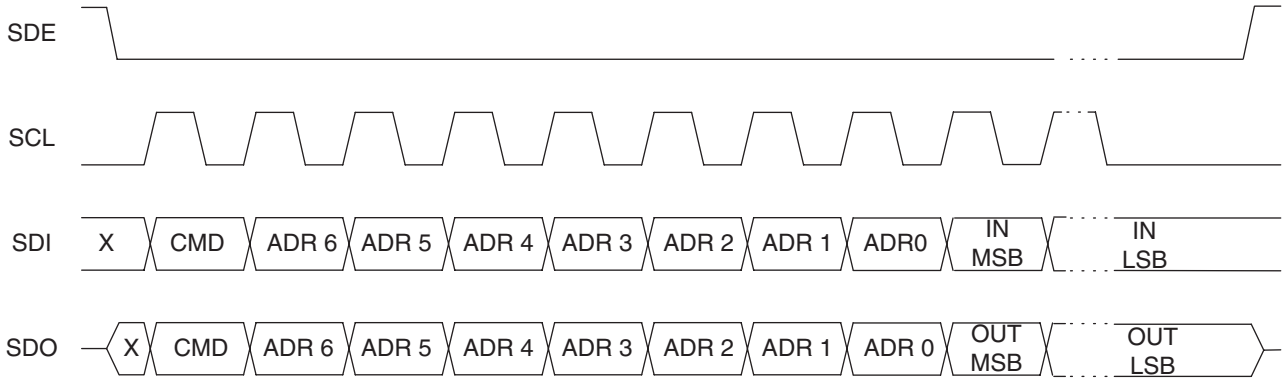
Table 5. For an 8 Bit Register

MSB							**LSB**
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Table 6. For a 16 Bit Register

MSB							**LSB**
DATA15	DATA14	DATA13	DATA12	DATA11	DATA10	DATA9	DATA8
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Figure 2. SPI Transmission for Multiple Bytes



Pin Description & Package Drawing

Table 7. Pin Description

PIN	PIN No.	DESCRIPTION
NIER	1	Interface Enable RX Gain Control Low active, input enable of the serial RX gain control interface
NIET	2	Interface Enable TX Level Control Low active, input enable of the serial TX level control interface
PRX	3	Power Switch of Receive Path High active, digital CMOS input levels
PTX	4	Power Switch Transmit Path High active, digital CMOS input levels
RFRX1	5	RF Receive Input 1 Low noise amplifier input. The 50Ω matching is, in part, the bond/package inductance and an external component (tbd).
RFRX2	6	RF Receive Input 2 Complementary signal to RFRX1
VSSRFRX	7	Ground Supply of Radio Frequency Receive Circuit Modules
VDDRFRX	8	Voltage Supply of Radio Frequency Receive Circuit Modules
RFTX1	9	RF Transmit Output 1 P1dB up to +10dBm @ 50Ω differential 3.5GHz. The 50Ω matching is, in part, the bond/package inductance and an external component (tbd).
RFTX2	10	RF Transmit Output 2 Complementary signal to RFTX1
VDDPA	11	Voltage Supply of Power Amplifier Driving Module
VDDRFTX2	12	Voltage Supply of Radio Frequency Transmit Circuit Modules
DTB	13	Digital Test Bus Input/Output Digital DTB input/output signal for testing purposes, connection and direction is configurable over SPI.
NRES	14	Power On Reset Low active, open drain output with internal 10kΩ pull up resistor
SDO	15	SPI Data Digital Output
NSDE	16	SPI Enable Digital Input The rising edge of SCL and a low SDE indicate the start of a data transmission to the SPI slave
SDI	17	SPI Data Digital Input Serial SPI data input stream is initiated with SDE and begins with an address byte. Input is MSB first. The MSB of the address byte is the R/W control bit. A number of data bytes follows after the address byte. The actual number of data bytes depends on the address.
SCL	18	SPI Clock Digital Input At every rising edge, the SDI data is latched into the internal SPI register. SDO data change also on the rising edge.
VDDSPI	19	Voltage Supply of SPI Interface Pads
VDDDIG1	20	Voltage Supply of Digital Circuit Modules
VSSDIG1	21	Ground Supply SPI Interface Pads and of Digital Circuit Modules

Table 7. Pin Description (Continued)

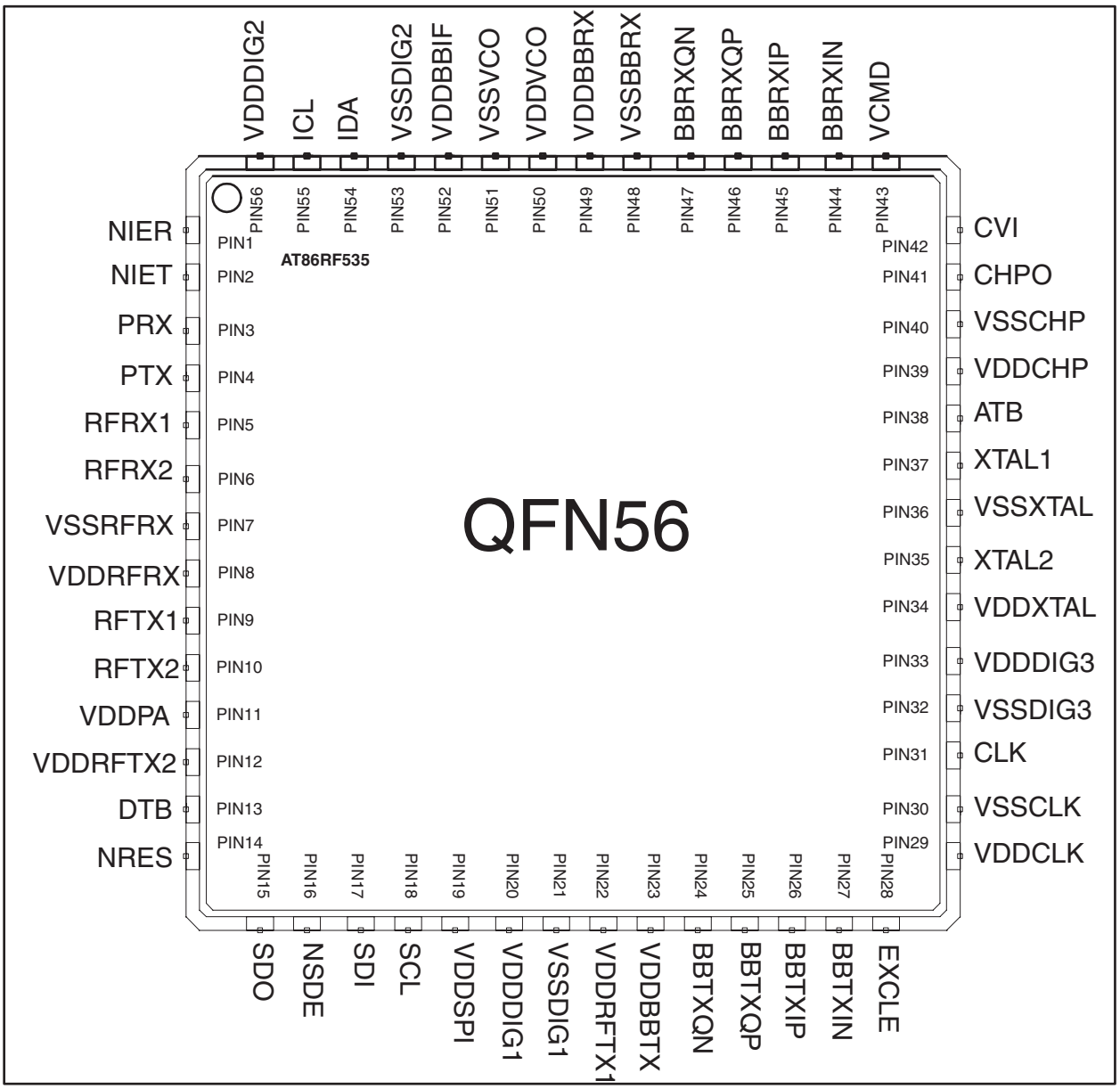
PIN	PIN No.	DESCRIPTION
VDDRFTX1	22	Voltage Supply of Radio Frequency Transmit Circuit Modules
VDDBBTX	23	Voltage Supply of BB TX circuit modules
BBTXQN	24	Base Band Transmit Input Q Negative Base Band transmit input signal Quad Phase
BBTXQP	25	Base Band Transmit Input P Positive Complementary signal to BBTXQN
BBTXIP	26	Base Band Transmit Input I Positive Base band transmit input signal In Phase
BBTXIN	27	Base Band Transmit Input I Negative Complementary signal to BBTXIP
EXCLE	28	External Clock Enable High active, digital CMOS input levels
VDDCLK	29	Voltage Supply of CMOS Clock I/O Modules
VSSCLK	30	Ground Supply of CMOS Clock I/O Modules
CLK	31	32/40MHz CMOS Clock digital I/O Direction depend on XTALE
VSSDIG3	32	Ground Supply of Synthesizer Divider Modules and Digital Modules
VDDDIG3	33	Voltage Supply of Synthesizer Divider Modules and Digital Modules
VDDXTAL	34	Voltage Supply of Crystal Circuit Modules
XTAL2	35	Crystal connection 32/40MHz Analog IO
VSSXTAL	36	Ground Supply of Crystal Circuit Modules
XTAL1	37	Crystal connection 32/40MHz Analog IO
ATB	38	Analog Test Bus Analog IO Analog output/input signal for testing purposes, connection configurable over SPI
VDDCHP	39	Voltage Supply of Phase Frequency Detector and Charge Pump Modules
VSSCHP	40	Ground Supply of Phase Frequency Detector and Charge Pump Modules
CHPO	41	Charge Pump Current Output For external filter mode, configurable by SPI
CVI	42	Control Voltage Input for external Loop Filter Configurable over SPI register
VCMD	43	Common Mode Voltage Bias Output RX Elements DC output voltage 1.0V, only active if PRX=High
BBRXIN	44	Base Band Receive Output I Negative In Phase output negative. The base band-processed signal is level voltage programmable to adapt to different base band ADCs. The capacitive load should be less than 10pF asymmetric
BBRXIP	45	Base Band Receive Output I Positive Complementary signal to BBRXIN

Table 7. Pin Description (Continued)

PIN	PIN No.	DESCRIPTION
BBRXQP	46	Base Band Receive Output Q Positive Quad Phase output positive. The base band-processed signal is voltage level programmable to adapt to different base band ADCs. The capacitive load should be less than 10pF asymmetric.
BBRXQN	47	Base Band Receive Output Q Negative Complementary signal to BBRXQP
VSSBBRX	48	Voltage Supply of BB Receive circuit modules
VDDBBRX	49	Voltage Supply of BB Receive circuit modules
VDDVCO	50	Voltage Supply of Synthesizer modules VCO and APLF
VSSVCO	51	Ground Supply of Synthesizer modules VCO and APLF
VDDBBIF	52	Voltage Supply of BB Interface Pads
VSSDIG2	53	Ground Supply of BB Interface Pads and of Digital Circuit Modules
IDA	54	Interface Data Data input of the serial gain, level and frequency control interface
ICL	55	Interface Clock Clock input of the serial gain, level and frequency control interface
VDDDIG2	56	Voltage Supply of Digital Circuit Modules

Note: Additional ground supplies are generated by down bonds to the exposed paddle.

Figure 3. Pinning Information



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5108B–WiMax–2/06